MOTOROLA

Professional Radio
GM Series

UHF (403-470MHz)

Service Information

Issue: August 2002

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Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 GM140/GM160 Model Chart

GM Series UHF 403-470 MHz					
Model					Description
MDM25RKC9AN1_E					GM140, 403-470 MHz, 25-40W, 4 Ch
	MDM25RKF9AN5_E				GM160, 403-470 MHz, 25-40W, 128 Ch
		MDM25RHC9AA1_E			GM140, 403-470 MHz, 1-25W, 4 Ch
			MDM25RHF9AA5_E		GM160, 403-470 MHz, 1-25W, 128 Ch
				Item	**Description**
X		X		GCN6112_	Control Head GM140
	X		X	GCN6120_	Control Head GM160
X				IMUE6012_	Tanapa, GM140
	X			IMUE6012_	Tanapa, GM160
		X		IMUE6021_	Tanapa, GM140
			X	IMUE6021_	Tanapa, GM160
X	X	X	X	ENBN4056_	Packaging, Waris Mobile Radio
X	X	X	X	GLN7324_	Low Profile Mounting Trunion
X	X			HKN9402_	12V Power Cable, 25-45W
		X	X	HKN4137_	12V Power Cable, 1-25W
X	X	X	X	MDRMN4025_	Enhanced Compact Microphone
X		X		6864110B86_	User Guide, GM140
	X		X	6864110B87_	User Guide, GM160

X = Indicates one of each is required

2.0 GM340/GM360/GM380 Model Chart

GM Series UHF 403-470 MHz					
Model					Description
MDM25RHC9AN1_E					GM340, 403-470 MHz, 1-25W, 6 Ch
	MDM25RHF9AN5_E				GM360, 403-470 MHz, 1-25W, 255 Ch
		MDM25RHC9AN8_E			GM380, 403-470 MHz, 1-25W, 255 Ch
			MDM25RHA9AN0_E		Databox, 403-470 MHz, 1-25W, 16 Ch
				Item	Description
X				GCN6112_	Control Head GM340
	X			GCN6120_	Control Head GM360
		X		GCN6121_	Control Head GM380
			X	GCN6116_	Databox Radio Blank Head
X				IMUE6015_S	Field Replaceable Unit (Main Board) GM340
	X			IMUE6015_S	Field Replaceable Unit (Main Board) GM360
		X		IMUE6038_S	Field Replaceable Unit (Main Board) GM380
			X	IMUE6015_A	S/T 403-470MHz 1-25 SEL5
X	X	X	X	ENBN4056_	Packaging, Waris Mobile
X	X	X	X	GLN7324_	Low Profile Mounting Trunnion
X	X	X	X	HKN4137_	12V Power Cable 1-25W
X	X	X		MDRMN4025_	Enhanced Compact Microphone
X				6864110B80	User Guide GM340
	X			6864110B81	User Guide, GM360
		X		6864110B82	User Guide, GM380

X = Indicates one of each is required

3.0 GM640/GM660/GM1280 Model Chart

	GM Series UHF 403-470 MHz				
	Model				Description
MDM25RHC9CK1_E					GM640, 403-470 MHz, 1-25W, 6 Ch
	MDM25RHF9CK5_E				GM660, 403-470 MHz, 1-25W, 255 Ch
		MDM25RHN9CK8_E			GM1280, 403-470 MHz, 1-25W, 255 Ch
			MDM25RHA9CK7_E		Databox, 403-470 MHz, 1-25W, 16 Ch
				Item	Description
X				GCN6112_	Control Head GM640
	X			GCN6120_	Control Head GM660
		X		GCN6121_	Control Head GM1280
			X	GCN6116_	Databox Radio Blank Head
			X	IMUE6009_A	S/T 403-470MHz 1-25 SEL5
X				IMUE6009_S	Field Replaceable Unit (Main Board) GM640
	X			IMUE6009_S	Field Replaceable Unit (Main Board) GM660
		X		IMUE6009_S	Field Replaceable Unit (Main Board) GM1280
X	X	X	X	ENBN4056_	Packaging, Waris Mobile Radio
X	X	X	X	GLN7324_	Low Profile Mounting Trunnion
X	X	X	X	HKN4137_	12V Power Cable, 1-25W
X	X	X		MDRMN4025_	Enhanced Compact Microphone
X				6864110B83_	User Guide, GM640
	X			6864110B84_	User Guide, GM660
		X		6864110B85_	User Guide, GM1280

X = Indicates one of each is required

4.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General Specifications	
Channel Capacity **GM140** **GM160** **GM340** **GM360** **GM380** **GM640** **GM660** **GM1280** **Databox**	 4 128 6 255 255 6 255 255 16
Power Supply	13.2Vdc (10.8 - 15.6Vdc)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM140/340/640** 56mm x 176mm x 177mm (1 - 25W) 56mm x 176mm x 189mm (25 - 40W) (add 8mm for Volume Knob)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM160/360/660** 59mm x 179mm x 186mm (1 - 25W) 59mm x 179mm x 198mm (25 - 40W) (add 9mm for Volume Knob)
Dimensions: H x W x D (mm) Depth excluding knobs	**GM380/1280** 72mm x 185mm x 188mm (add 8mm for Volume Knob)
Dimensions: H x W x D (mm) Depth excluding knobs	**Databox** 44mm x 168mm x 161mm
Weight **GM140/340/640**	1400gr
Weight **GM160/360/660**	1400gr
Weight **GM380/1280**	1500gr
Weight **Databox**	1220gr
Sealing:	Withstands rain testing per MIL STD 810 C/D /E and IP54
Shock and Vibration:	Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603
Dust and Humidity:	Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603

Transmitter	UHF
*Frequencies - Full Bandsplit	UHF 403-470 MHz
Channel Spacing	12.5/20/25 kHz
Frequency Stability (-30°C to +60°C, +25° Ref.)	±2.0 ppm
Power	1-25W/25-40W
Modulation Limiting	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz
FM Hum & Noise	-40 dB @ 12.5kHz -45 dB @ 20/25kHz
Conducted/Radiated Emission (ETS)	-36 dBm <1 GHz -30 dBm >1 GHz
Adjacent Channel Power	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB
Audio Distortion @1000Hz, 60% Rated Maximum Deviation	<3% typical

Receiver	UHF
*Frequencies - Full Bandsplit	UHF 403-470 MHz
Channel Spacing	12.5/20/25 kHz
Sensitivity (12 dB SINAD)	0.30 µV (0.22 µV typical)
Intermodulation (ETS)	>65 dB Base Mode: >70dB (1-25W model only)
Adjacent Channel Selectivity (ETS)	65 dB @ 12.5 kHz 70 dB @ 20 kHz 75 dB @ 25 kHz
Spurious Rejection (ETS)	70 dB @ 12.5 kHz 75 dB @ 20/25 kHz
Rated Audio	3W Internal 13W External
Audio Distortion @ Rated Audio	<3% typical
Hum & Noise	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz
Audio Response (300 - 3000Hz @ 20/25kHz) (300 - 2550Hz @12.5kHz)	+1 to -3 dB
Conducted Spurious Emission (ETS)	-57 dBm <1 GHz -47 dBm >1 GHz

*Availability subject to the laws and regulations of individual countries.

Chapter 2

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the UHF circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

2.0 UHF (403-470MHz) Receiver

2.1 Receiver Front-End

The receiver is able to cover the UHF range from 403 to 470 MHz. It consists of four major blocks: front-end bandpass filters and pre-amplifier, first mixer, high-IF, low-IF and receiver back-end . Two varactor-tuned bandpass filters perform antenna signal pre-selection. A cross over quad diode mixer converts the signal to the first IF of 44.85 MHz. Low-side first injection is used.

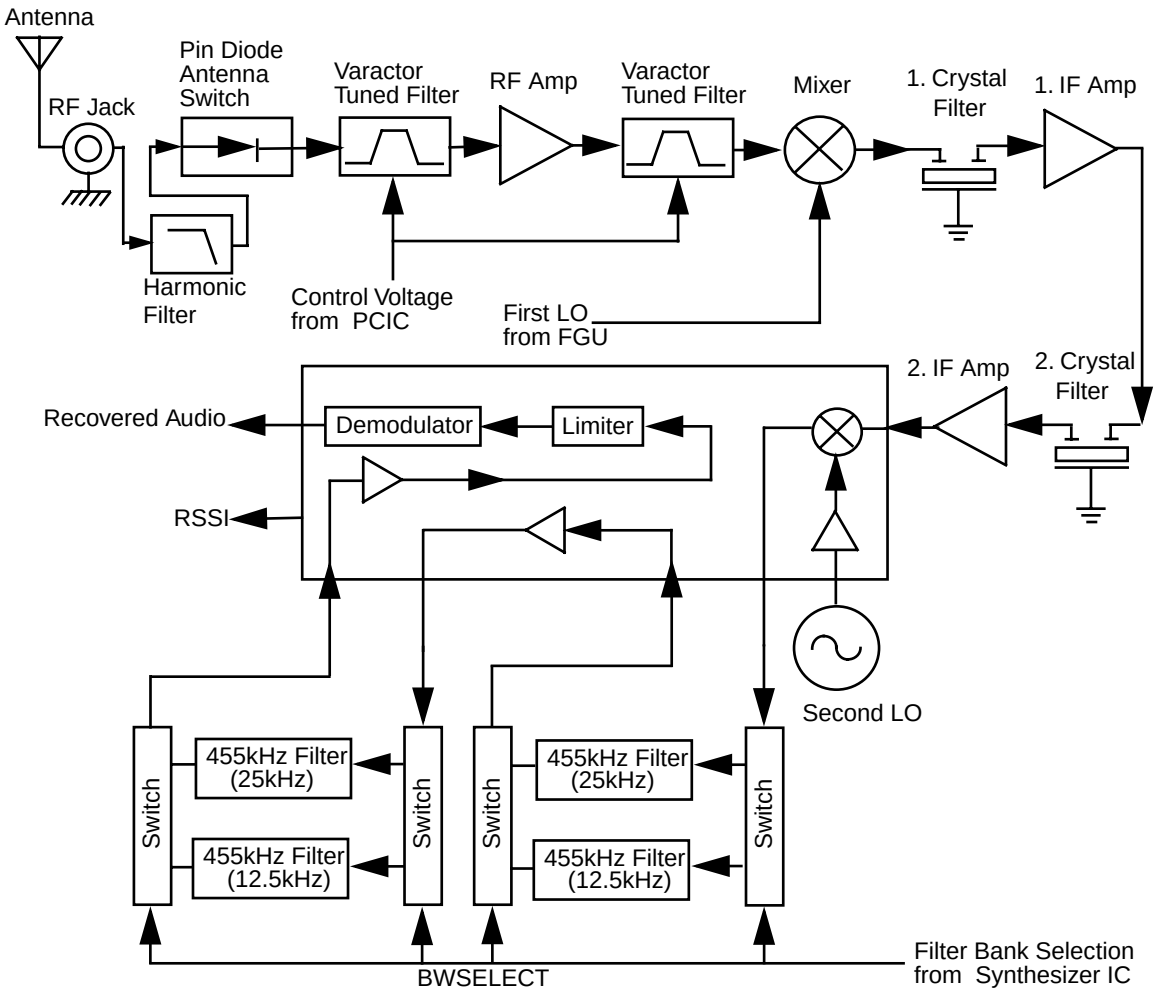


Figure 2-1 UHF Receiver Block Diagram

There are two 2-pole 44.85 MHz crystal filters in the high-IF section and 2 pairs of 455 kHz ceramic filters in the low-IF section to provide the required adjacent channel selectivity .The correct pair of ceramic filters for 12.5 or 25KHz channel spacing is selected via control line BWSELECT. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

2.2 Front-End Band-Pass Filters & Pre-Amplifier

The received signal from the radio's antenna connector is first routed through the harmonic filter and antenna switch, which are part of the RF power amplifier circuitry, before being applied to the receiver pre-selector filter (C4001, C4002, D4001 and associated components). The 2-pole pre-selector filter tuned by the varactor diodes D4001 and D4002 pre-selects the incoming signal (RXIN) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FECTRL_1) ranging from 2 volts to 8 volts is controlled by pin 20 of PCIC (U4501) in the Transmitter section. A dual hot carrier diode (D4003) limits any inband signal to 0 dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q4003) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA is drawn from the voltage 9V3 via L4003 and R4002. A switchable 3dB pad (R4066,R4007,R4063, R4064 and R4070), controlled via line FECTRL_2 and Q4004 stabilizes the output impedance and intermodulation performance.

A second 2-pole varactor tuned bandpass filter provides additional filtering of the amplified signal. The varactor diodes D4004 and D4005 are controlled by the same signal FECTRL_1, which controls the pre-selector filter. A following 1 dB pad (R4013 - R4015) stabilizes the output impedance and intermodulation performance.

2.3 First Mixer and High Intermediate Frequency (IF)

The signal coming from the front-end is converted to the first IF (44.85 MHz) using a cross over quad diode mixer (D4051). Its ports are matched for incoming RF signal conversion to the 44.85 MHz IF using low side injection via matching transformers T4051 and T4052. The injection signal (RXINJ) coming from the RX VCO buffer (Q4332) is filtered by the lowpass filter consisting of (L4053, L4054, C4053 - C4055) followed by a matching transformer T4052 and has a level of approximately 15dBm.

The mixer IF output signal (IF) from transformer T4501pin 2 is fed to the first two pole crystal filter FL3101. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q3101 is actively biased by a collector base feedback (R3101, R3106) to a current drain of approximately 5 mA drawn from the voltage 5V. Its output impedance is matched to the second two pole crystal filter FL3102. The signal is further amplified by a preamplifier (Q3102) before going into pin 1 of IFIC (U3101).

A dual hot carrier diode (D3101) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

2.4 Low Intermediate Frequency (IF) and Receiver Back End

The 44.85 high IF signal from the second IF amplifier feeds the IF IC (U3101) at pin1. Within the IF IC the 44.85 MHz high IF signal mixes with the 44.395 MHz second local oscillator (2nd LO) to

produce the low IF signal at 455 kHz. The 2nd LO frequency is determined by crystal Y3101. The low IF signal is amplified and filtered by an external pair of 455 kHz ceramic filters FL3112, FL3114 for 20/25 kHz channel spacing or FL3111,FL3113/F3115 for 12.5 kHz channel spacing. These pairs are selectable via BWSELECT. The filtered output from the ceramic filters is applied to the limiter input pin of the IF IC (pin 14).

The IF IC contains a quadrature detector using a ceramic phase-shift element (Y3102) to provide audio detection. Internal amplification provides an audio output level of 120 mV rms (at 60% deviation) from U3103 pin 8 (DISCAUDIO) which is fed to the ASFIC_CMP (U0221) pin 2 (part of the Controller circuitry).

A received signal strength indicator (RSSI) signal is available at U3101 pin 5, having a dynamic range of 70 dB. The RSSI signal is interpreted by the microprocessor (U0101 pin 63) and in addition is available at accessory connector J0501-15.

3.0 UHF (403-470MHz) Transmitter Power Amplifier (PA) 25 W

The radio's 25W PA is a three stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. All three stages utilize LDMOS technology. The gain of the first stage (U4401) is adjustable, controlled by pin 4 of PCIC (U4501) via U4402-1. It is followed by an LDMOS stage (Q4421) and LDMOS final stage (Q4441).

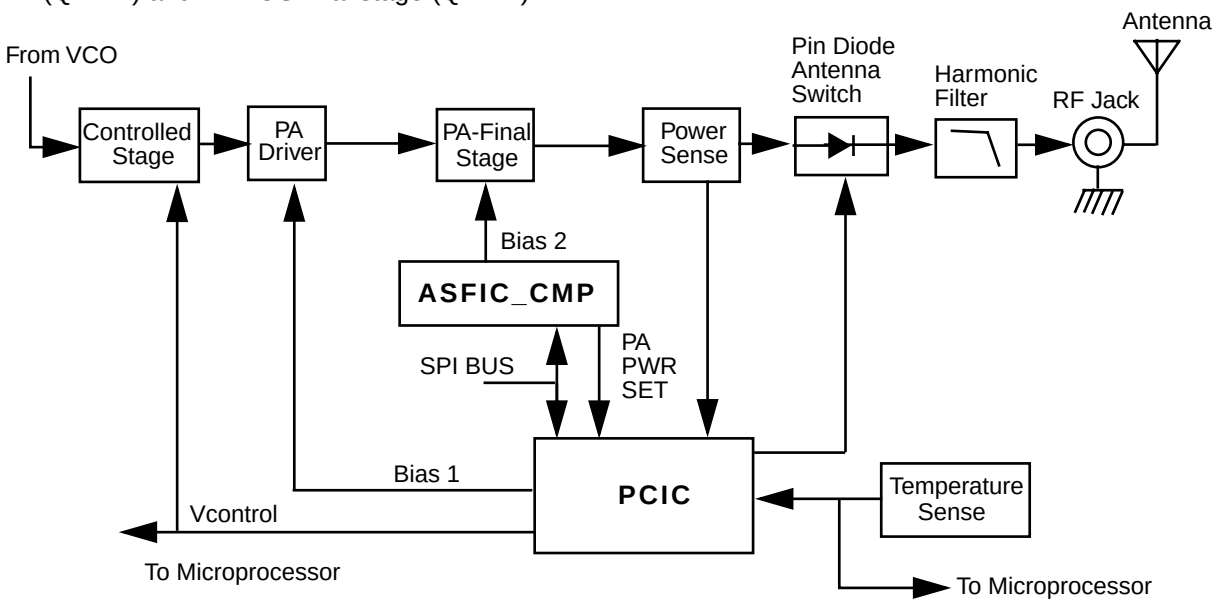


Figure 2-2 UHF Transmitter Block Diagram

Devices U4401, Q4421 and Q4441 are surface mounted. A pressure pad between board and the radio's cover provides good thermal contact between the devices and the chassis.

3.1 First Power Controlled Stage

The first stage (U4401) is a 20dB gain integrated circuit containing two LDMOS FET amplifier stages. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U4401 is

controlled by a DC voltage applied to pin 1 from the op-amp U4402-1, pin 1. The control voltage simultaneously varies the bias of two FET stages within U4401. This biasing point determines the overall gain of U4401 and therefore its output drive level to Q4421, which in turn controls the output power of the PA.
Op-amp U4402-1 monitors the drain current of U4401 via resistor R4444 and adjusts the bias voltage of U4401 so that the current remains constant. The PCIC (U4501) provides a DC output voltage at pin 4 (INT) which sets the reference voltage of the current control loop. A raising power output causes the DC voltage from the PCIC to fall, and U4402-1 adjusts the bias voltage for a lower drain current to lower the gain of the stage.
In receive mode the DC voltage from PCIC pin 23 (RX) turns on Q4442, which in turn switches off the biasing voltage to U4401.

Switch S5440 is a pressure pad with a conductive strip which connects two conductive areas on the board when the radio's cover is properly screwed to the chassis. When the cover is removed, S5440 opens and the resulting high voltage level at the inverting inputs of the current control op-amps U4402-1 & 2 switches off the biasing of U4401 and Q4421. This prevents transmitter key up while the devices do not have proper thermal contact to the chassis.

3.2 Power Controlled Driver Stage

The next stage is an LDMOS device (Q4421) providing a gain of 12dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The bias is set during transmit mode by the drain current control op-amp U4402-2, and fed to the gate of Q4421 via the resistive network R4429, R4418, R4415 and R4416.
Op-amp U4402-2 monitors the drain current of U4421 via resistors R4424-27 and adjusts the bias voltage of Q4421 so that the current remains constant. The PCIC (U4501) provides a DC output voltage at pin 4 (INT) which sets the reference voltage of the current control loop. A raising power output causes the DC voltage from the PCIC to fall, and U4402-2 adjusts the bias voltage for a lower drain current to lower the gain of the stage.
In receive mode the DC voltage from PCIC pin 23 (RX) turns on Q4422, which in turn switches off the biasing voltage to Q4421.

3.3 Final Stage

The final stage is an LDMOS device (Q4441) providing a gain of 12dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line MOSBIAS_2 is set in transmit mode by the ASFIC and fed to the gate of Q4441 via the resistive network R4404, R4406, and R4431-2. This bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Golbal Tuner. Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device’s drain current is drawn directly from the radio’s DC supply voltage input, PASUPVLTG, via L4436 and L4437.
A matching network consisting of C4441-49 and striplines transforms the impedance to 50 ohms and feeds the directional coupler.

3.4 Directional Coupler

The directional coupler is a microstrip printed circuit, which couples a small amount of the forward power delivered by Q4441. The coupled signal is rectified by D4451. The DC voltage is proportional to the RF output power and feeds the RFIN port of the PCIC (U4501 pin 1). The PCIC controls the gain of stages U4401 and Q4421 as necessary to hold this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

3.5 Antenna Switch

The antenna switch consists of two PIN diodes, D4471 and D4472. In the receive mode, both diodes are off. Signals applied at the antenna jack J4401 are routed, via the harmonic filter, through network L4472, C4474 and C4475, to the receiver input. In the transmit mode, K9V1 turns on Q4471 which enables current sink Q4472, set to 96 mA by R4473 and VR4471. This completes a DC path from PASUPVLTG, through L4437, D4471, L4472, D4472, L4471, R4474 and the current sink, to ground. Both diodes are forward biased into conduction. The transmitter RF from the directional coupler is routed via D4471 to the harmonic filter and antenna jack. D4472 also conducts, shunting RF power and preventing it from reaching the receiver port (RXIN). L4472 is selected to appear as a broadband lambda/4 wave transmission line, making the short circuit presented by D4472 appear as an open circuit at the junction of D4472 and the receiver path.

3.6 Harmonic Filter

Components L4491-L4493 and L4472, C4491, C4496-98 form a Butterworth low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R4491 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

3.7 Power Control

The transmitter uses the Power Control IC (PCIC, U4501) to control the power output of the radio. A portion of the forward RF power from the transmitter is sampled by the directional coupler and rectified, to provide a DC voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.

The ASFIC (U0221) has internal digital to analog converters (DACs) which provide a reference voltage of the control loop to the PCIC via R4505. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuit.

The PCIC provides a DC output voltage at pin 4 (INT) which sets the drain current of the first (U4401) and second (Q4421) transmitter stage via current control op-amps U3402-1 and U3402-2. This adjusts the transmitter power output to the intended value. Variations in forward transmitter power cause the DC voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power.

Capacitors C4502-4, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U4502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 30) proportional to temperature. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

4.0 UHF (403-470MHz) Frequency Synthesis

The synthesizer subsystem consists of the reference oscillator (Y4261 or Y4262), the Low Voltage Fractional-N synthesizer (LVFRAC-N, U4201), and the Voltage Controlled Oscillator VCO.

4.1 Reference Oscillator

The reference oscillator (Y4262) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An Analogue to Digital (A/D) converter internal to U4201 (LVFRAC-N) and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U4201 pin 25 to set the frequency of the oscillator. The output of the oscillator (pin 3 of Y4262) is applied to pin 23 (XTAL1) of U4201 via a RC series combination.

In applications where less frequency stability is required the oscillator inside U4201 is used along with an external crystal Y4261, varactor diode D4261, C4261, C4262 and R4262. In this case, Y4262, R4263, C4235 and C4251 are not used. When Y4262 is used, Y4261, D4261, C4261, C4262 and R4262 are not used, and C4263 is increased to 0.1 uF.

4.2 Fractional-N Synthesizer

The LVFRAC-N synthesizer IC (U4201) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analogue modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 5 volts.

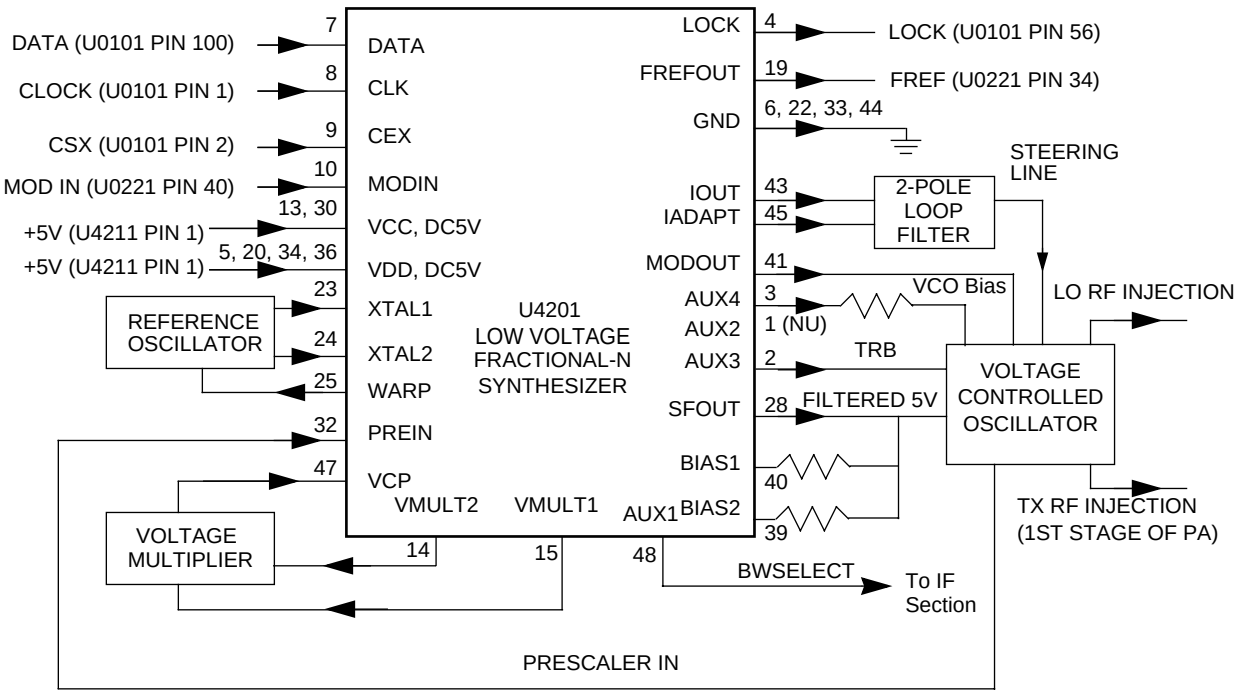


Figure 2-3 UHF Synthesizer Block Diagram

A voltage of 5V applied to the super filter input (U4201 pin 30) supplies an output voltage of 4.5 VDC(VSF) at pin 28. It supplies the VCO, VCO modulation bias circuit (via R4322) and the synthesizer charge pump resistor network (R4251, R4252). The synthesizer supply voltage is provided by the 5V regulator U4211.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U4201-47), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D4201, C4202, C4203). This voltage multiplier is basically a diode capacitor network driven by two (1.05MHz) 180 degrees out of phase signals (U4201-14 and -15).

Output LOCK (U4201-4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U4201 provides the 16.8 MHz reference frequency at pin 19.

The serial interface (SRL) is connected to the microprocessor via the data line DATA (U4201-7), clock line CLK (U4201-8), and chip enable line CSX (U4201-9).

4.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) consists of the VCO/Buffer IC (VCOBIC, U4301), the TX and RX tank circuits, the external RX buffer stages, and the modulation circuitry.

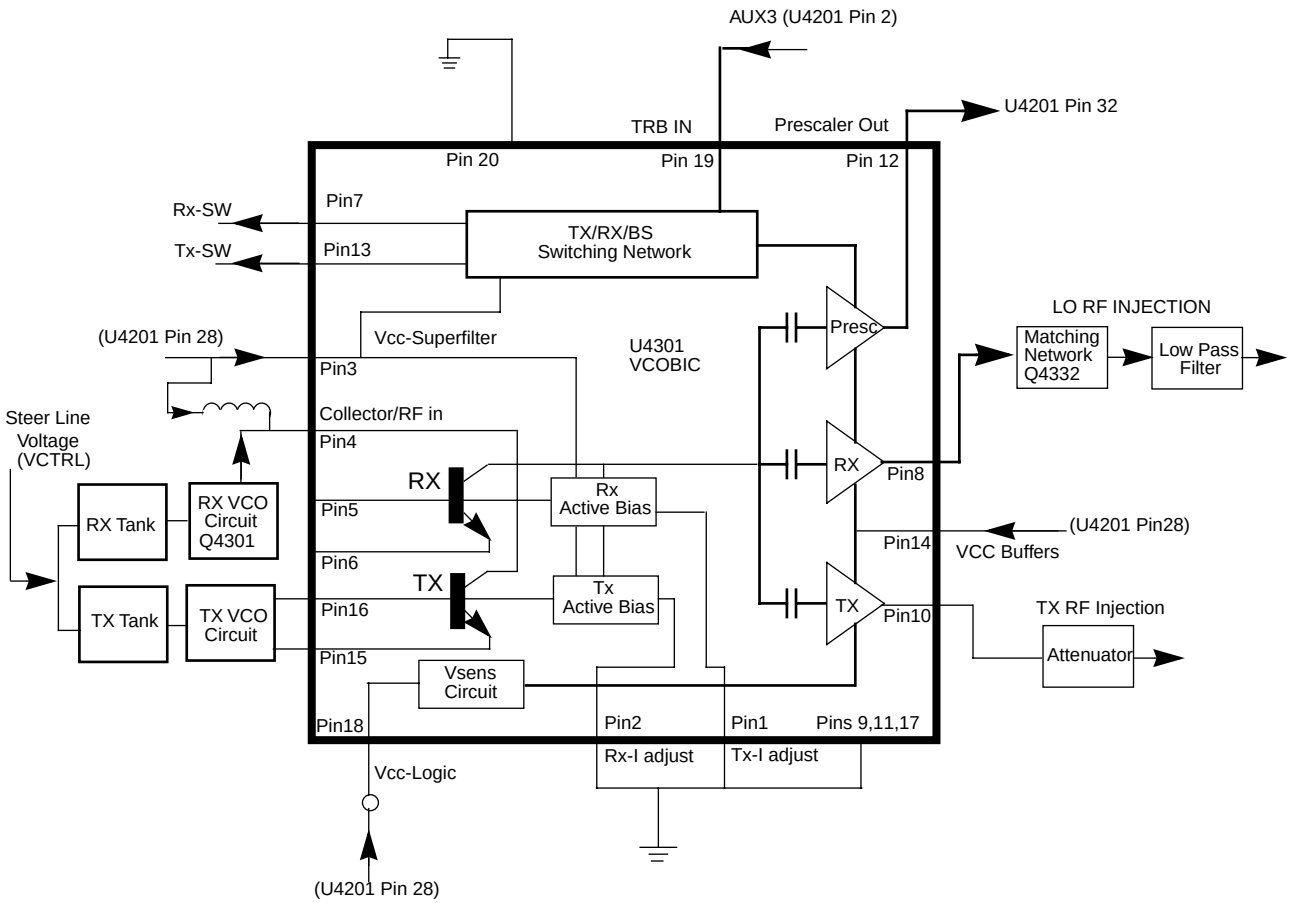


Figure 2-4 UHF VCO Block Diagram

The VCOBIC together with Fractional-N synthesizer (U4201) generates the required frequencies in both transmit and receive modes. The TRB line (U4301 pin 19) determines which tank circuits and internal buffers are to be enabled. A high level on TRB enables TX tank and TX output (pin 10), and a low enables RX tank and RX output (pin 8). A sample of the signal from the enabled output is routed from U4301 pin 12 (PRESC_OUT), via a low pass filter, to pin 32 of U4201 (PREIN).

A steering line voltage (VCTRL) between 3.0V and 10.0V at varactor diode CR4311 will tune the full TX frequency range (TXINJ) from 403 MHz to 470 MHz, and at varactor diodes CR4301, CR4302 and CR4303 will tune the full RX frequency range (RXINJ) from 358 MHz to 425 MHz. The tank circuits uses the Hartley configuration for wider bandwidth. For the RX tank circuit, an external transistor Q4301 is used in conjunction with the internal transistor for better side-band noise.

The external RX buffers (Q4332) are enabled by a high at U4201 pin 3 (AUX4) via transistor switch Q4333. In TX mode the modulation signal (VCOMOD) from the LVFRAC-N synthesizer IC (U4201 pin41) is applied modulation circuitry CR4321, R4321, R4322 and C4324, which modulates the TX VCO frequency via coupling capacitor C4321. Varactor CR4321 is biased for linearity from VSF.

4.4 Synthesizer Operation

The complete synthesizer subsystem comprises mainly of low voltage FRAC-N (LVFRACN) IC, Reference Oscillator (crystal oscillator with temperature compensation), charge pump circuitry, loop filter circuitry and DC supply. The output signal PRESC_OUT of the VCOBIC (U4301 pin12) is fed to pin 32 of U4201 (PREIN) via a low pass filter (C4229, L4225) which attenuates harmonics and provides the correct level to close the synthesizer loop.
The pre-scaler in the synthesizer (U4201) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y4261 or Y4262).
The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 43 of U4201 (IOUT). The loop filter (which consists of R4221-R4223, C4221-C4225,L4221) transforms this current into a voltage that is applied to the varactor diodes CR4311 for transmit, CR4301, CR4302 & CR4303 for receive and alters the output frequency of the VCO .The current can be set to a value fixed in the LVFRAC-N IC or to a value determined by the currents flowing into BIAS 1 (U4201-40) or BIAS 2 (U4201-39). The currents are set by the value of R4251 or R4252 respectively. The selection of the three different bias sources is done by software programming.
To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT (U4201-45) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the CSX line. When the synthesizer is within the lock range the current is determined only by the resistors connected to BIAS 1, BIAS 2, or the internal current source. A settled synthesizer loop is indicated by a high level of signal LOCK (U4201-4).
The LOCK (U4201-4) signal is routed to one of the µP´s ADCs input U101-56. From the voltage the µP determines whether LOCK is active. In order to modulate the PLL the two spot modulation method is utilized. Via pin 10 (MODIN) on U4201 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analogue modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U4201-41) and connected to the VCO modulation diode CR4321 via R4321, C4325.

5.0 UHF (403-470MHz) Transmitter Power Amplifier (PA) 40W

The radio's 40 W PA is a four stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. It consists of the following four stages in the line-up. The first stage is a LDMOS predriver (U4401) that is controlled by pin 4 of PCIC (U4501) via Q4473 (CNTLVLTG). It is followed by another LDMOS stage (Q4421), an LDMOS stage (Q4431) and a bipolar final stage (Q4441).

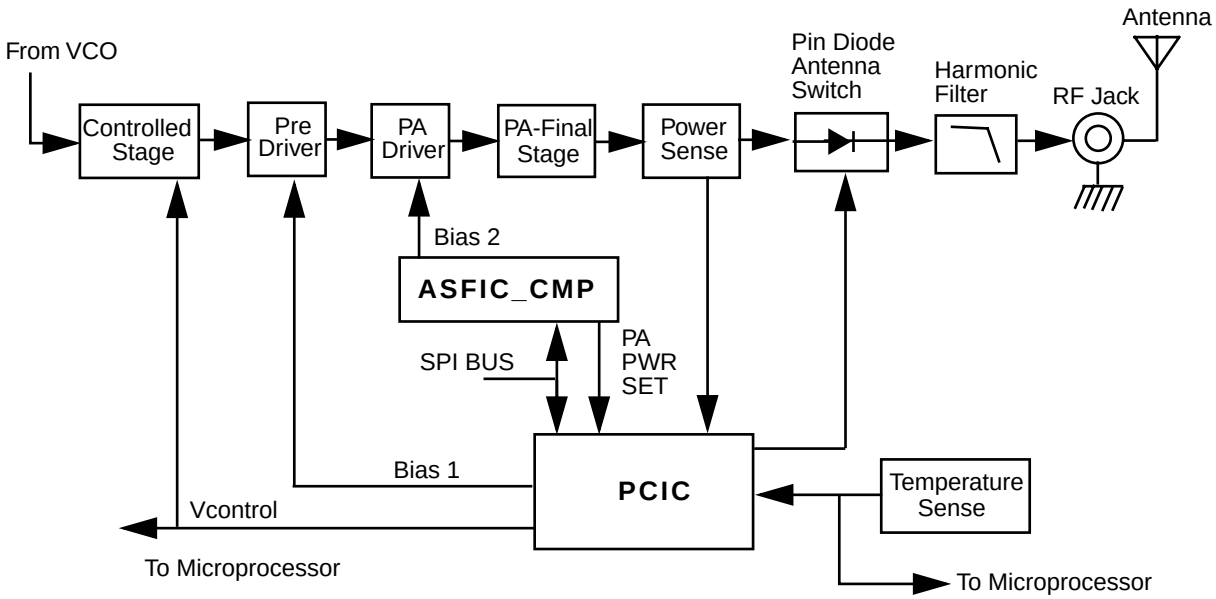


Figure 2-1 UHF Transmitter Block Diagram

Device Q4401 is surface mounted. Q4421, Q4431 and Q4441 are directly attached to the heat sink.

5.1 Power Controlled Stage

The first stage (U4401) amplifies the RF signal from the VCO (TXINJ) and controls the output power of the PA. The output power of the transistor U4401 is controlled by a voltage control line feed from the PCIC pin4(U4501). The control voltage simultaneously varies the bias of two FET stages within U4401. This biasing point determines the overall gain of U4401 and therefore its output drive level to Q4421, which in turn controls the output power of the PA.

In receive mode the voltage control line is at ground level and turns off Q4473 which in turn switches off the biasing voltage to U4401.

5.2 Pre-Driver Stage

The next stage is a 13dB gain LDMOS device (Q4421) which requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line PCIC_MOSBIAS_1 is set in transmit mode by PCIC pin 24 and fed to the gate of Q4421 via the resistive network R4480, R4416 and R4415. The bias voltage is tuned in the factory.

5.3 Driver Stage

The following stage is an enhancement-mode N-Channel MOSFET device (Q4431) providing a gain of 10dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line Bias_2_UHF_PA_1 is set in transmit mode by the ASFIC and fed to the gate of Q4431 via the resistive network R4632, R4631, R4485 and R4486. This bias voltage is also tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Customer Programming Software (CPS). Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's DC supply voltage input, A+, via L4421.

5.4 Final Stage

The final stage uses the bipolar device Q4441. The device's collector current is also drawn from the radio's DC supply voltage input. To maintain class C operation, the base is DC-grounded by a series inductor (L4441) and a bead (L4440). A matching network consisting of C4441-C4444, C4491 and two striplines transforms the impedance to 50 Ohms and feeds the directional coupler.

5.5 Directional Coupler

The Bi-directional coupler is a microstrip printed circuit, which couples a small amount of the forward and reverse power of the RF power from Q4441. The coupled signal is rectified to an output power proportional DC voltage by the diodes D4451 & D4452 and sent to the RFIN of PCIC. The PCIC controls the gain of stage U4401 as necessary to hold this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

5.6 Antenna Switch

The antenna switch consists of two PIN diodes, D4471 and D4472. In the receive mode, both diodes are off. Signals applied at the antenna jack J4401 are routed, via the harmonic filter, through network L4472, C4474 and C4475, to the receiver input. In the transmit mode, K9V1 turns on Q4471 which enables current sink Q4472, set to 96 mA by R4511 and VR4471. This completes a DC path from PASUPVLTG, through L4437, D4471, L4472, D4472, L4473, R4496 and the current sink, to ground. Both diodes are forward biased into conduction. The transmitter RF from the directional coupler is routed via D4471 to the harmonic filter and antenna jack. D4472 also conducts, shunting RF power and preventing it from reaching the receiver port (RXIN). L4472 is selected to appear as a broadband Lambda/4 wave transmission line, making the short circuit presented by D4472 appear as an open circuit at the junction of D4472 and the receiver path.

5.7 Harmonic Filter

Inductors L4491, L4492, L4493 and capacitors C4448, C4492,C4494, C4496 and C4498 form a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R4491 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

5.8 Power Control

The transmitter uses the Power Control IC (PCIC, U4501) to control the power output of the radio. A portion of the forward RF power from the transmitter is sampled by the bi-directional coupler and rectified, to provide a DC voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter s power detector circuitry.

The PCIC provides a DC output voltage at pin 4 (INT) which is applied as CNTLVLTG to the power-adjust input pin of the first transmitter stage U4401. This adjusts the transmitter power output to the intended value. Variations in forward transmitter power cause the DC voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power.

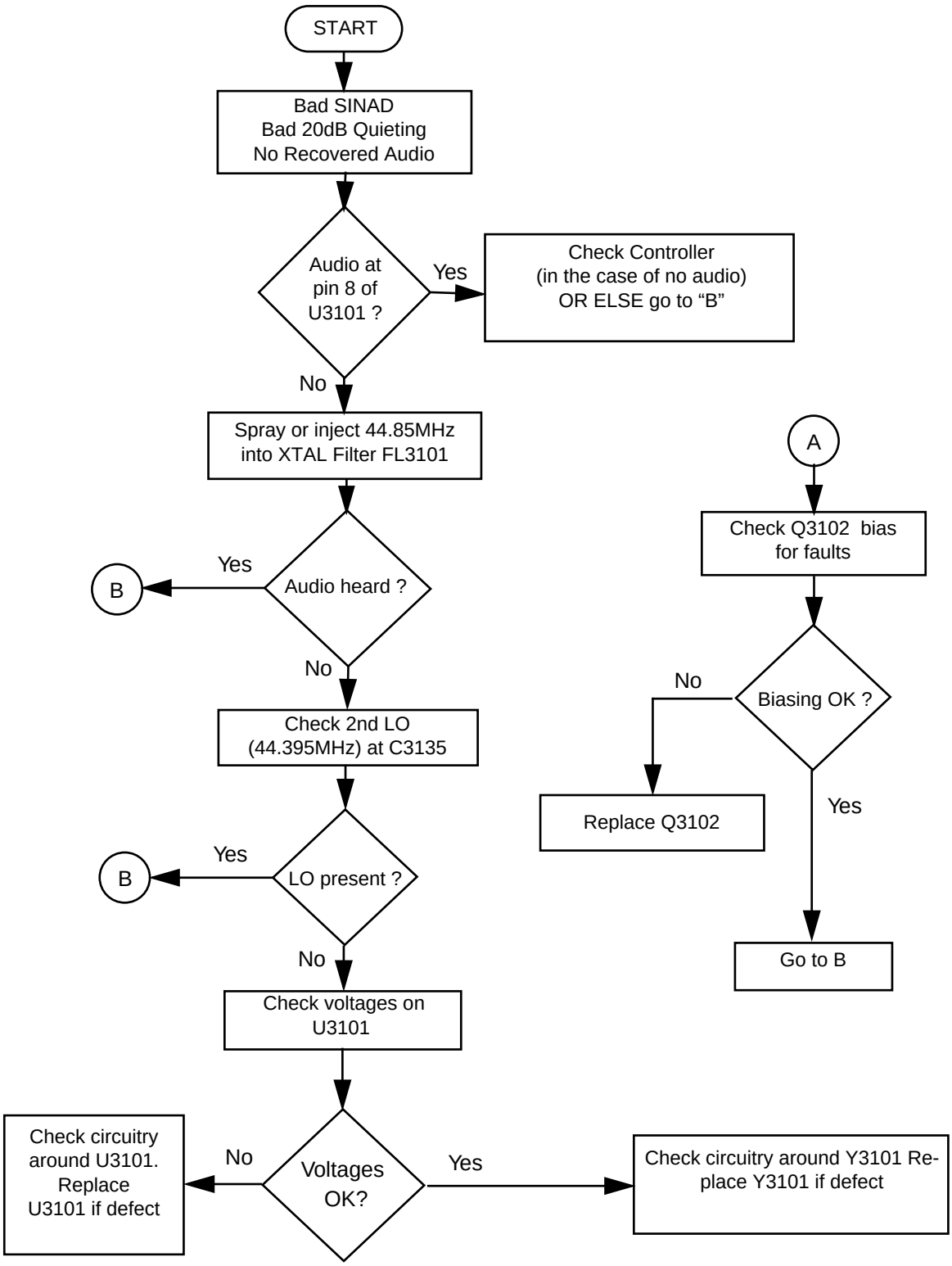
Capacitors C4502-4, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U4502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 29) proportional to temperature. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

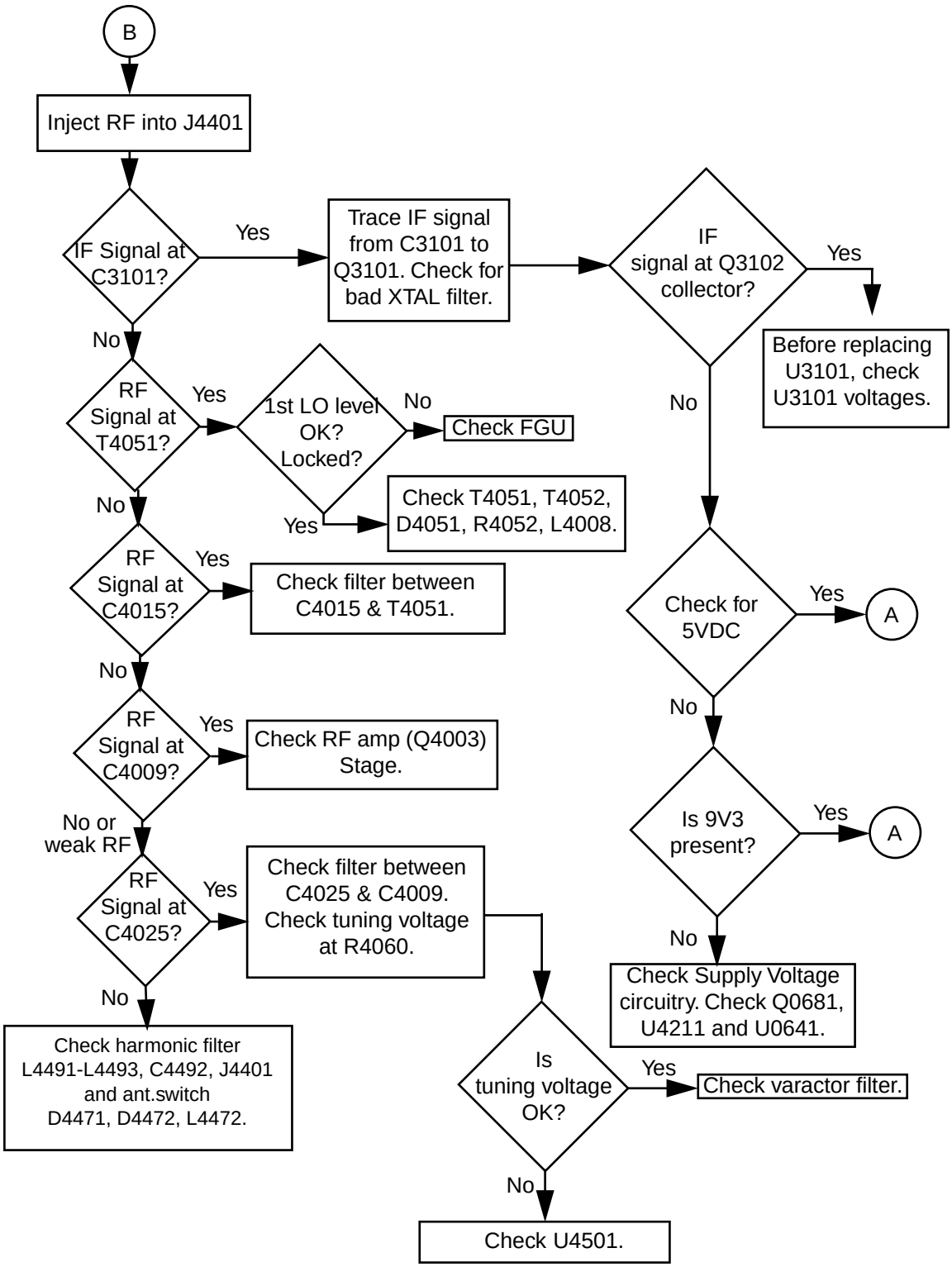
Chapter 3

TROUBLESHOOTING CHARTS

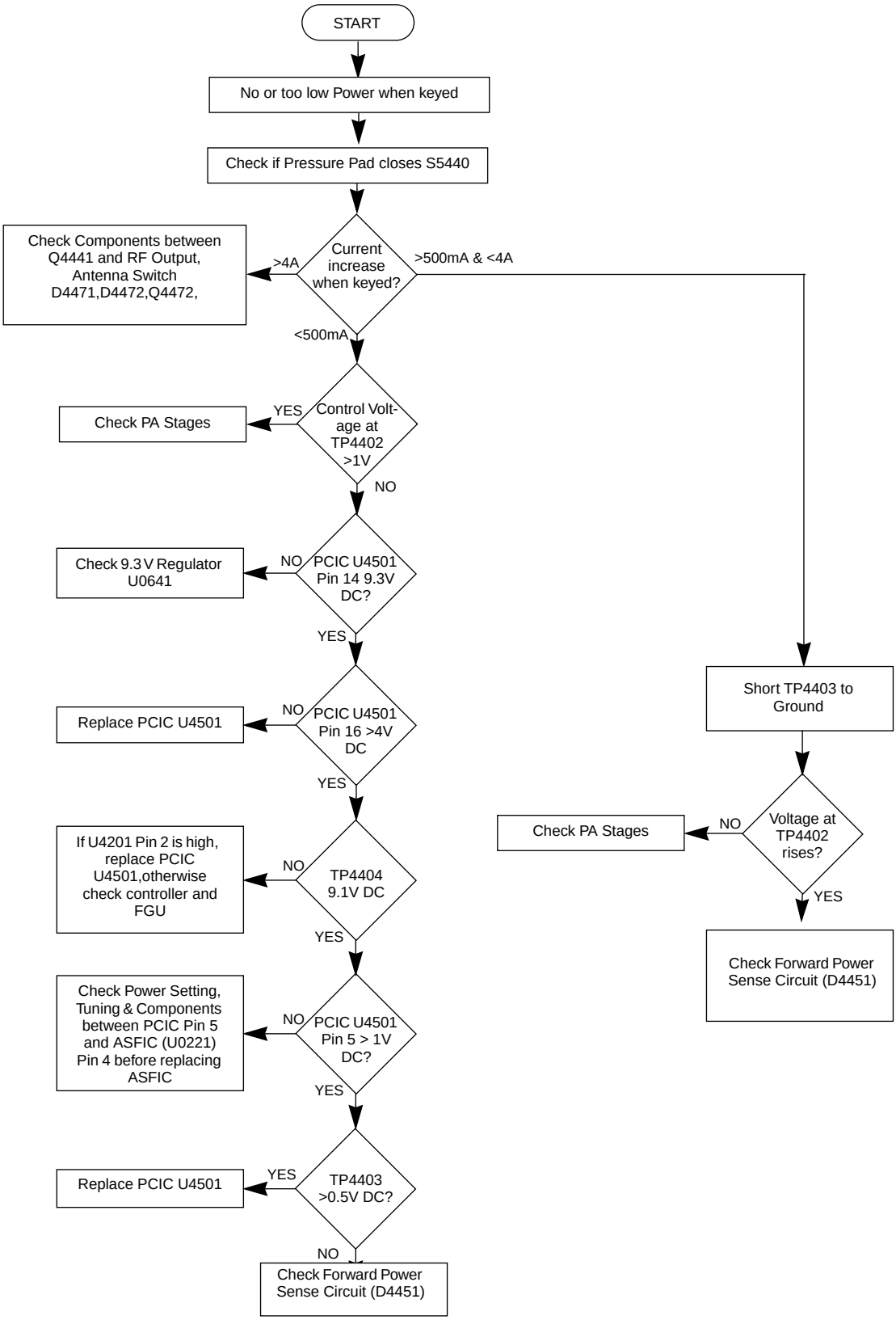
1.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



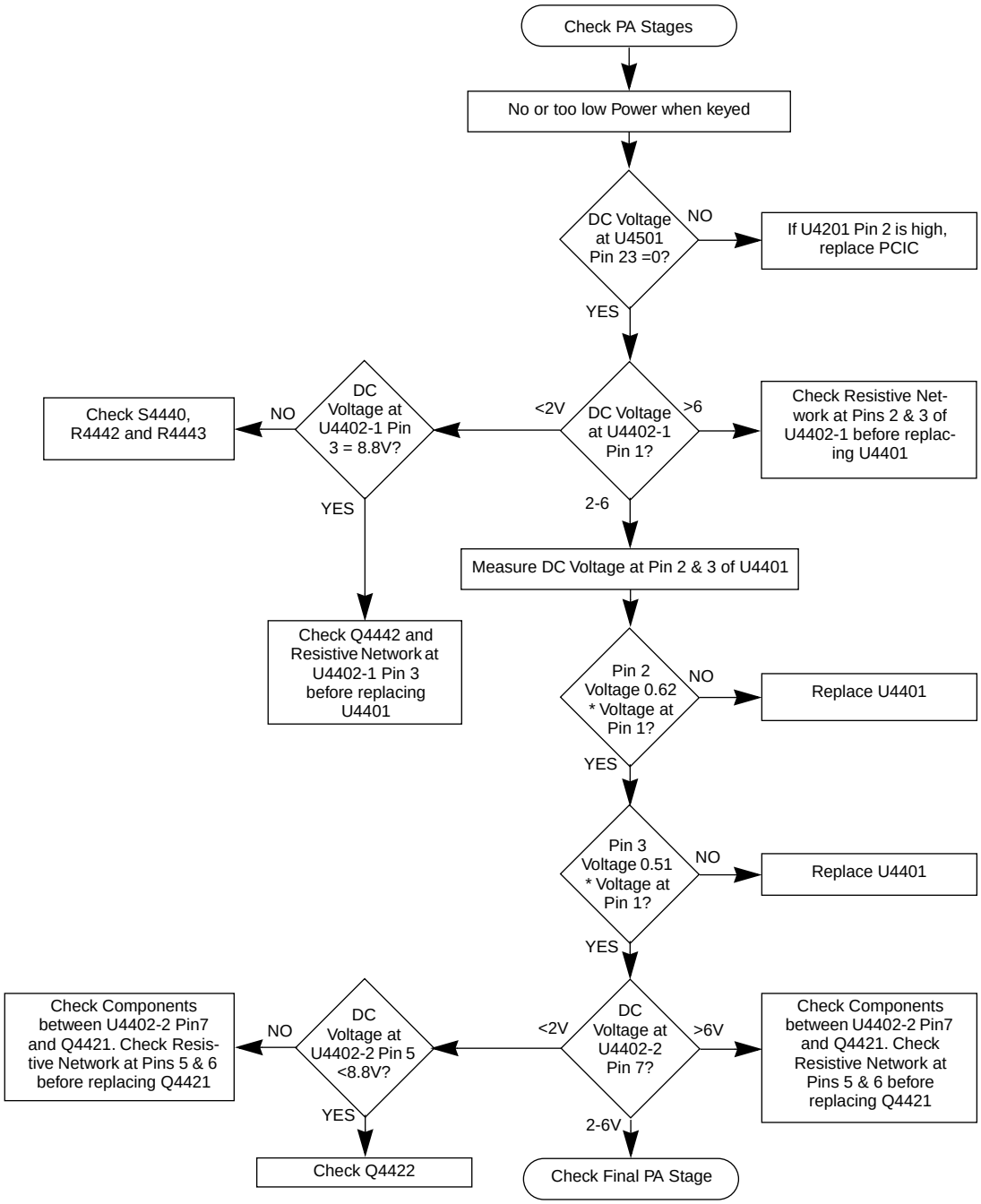
1.1 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



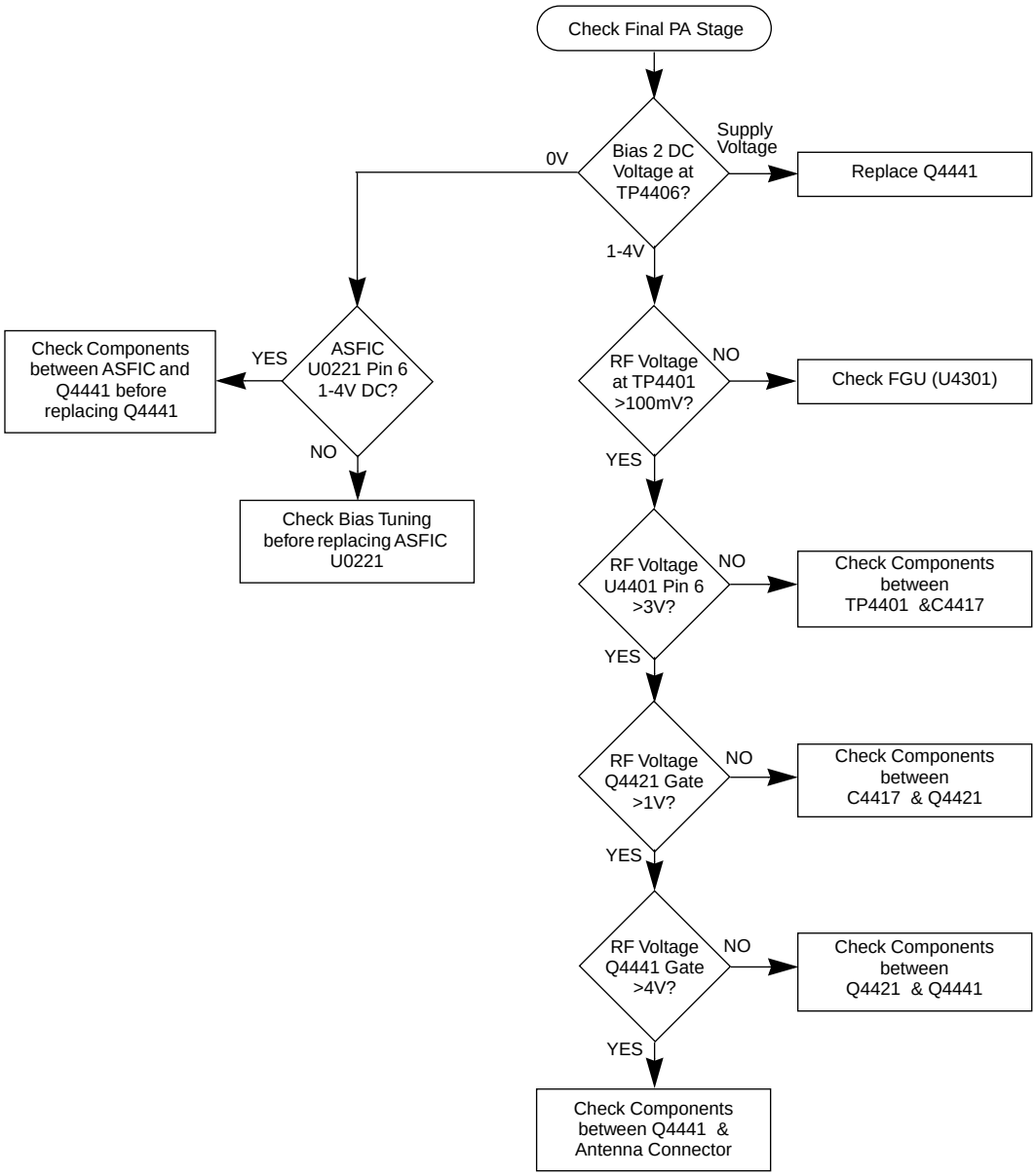
2.0 Troubleshooting Flow Chart for 25W Transmitter (Sheet 1 of 3)



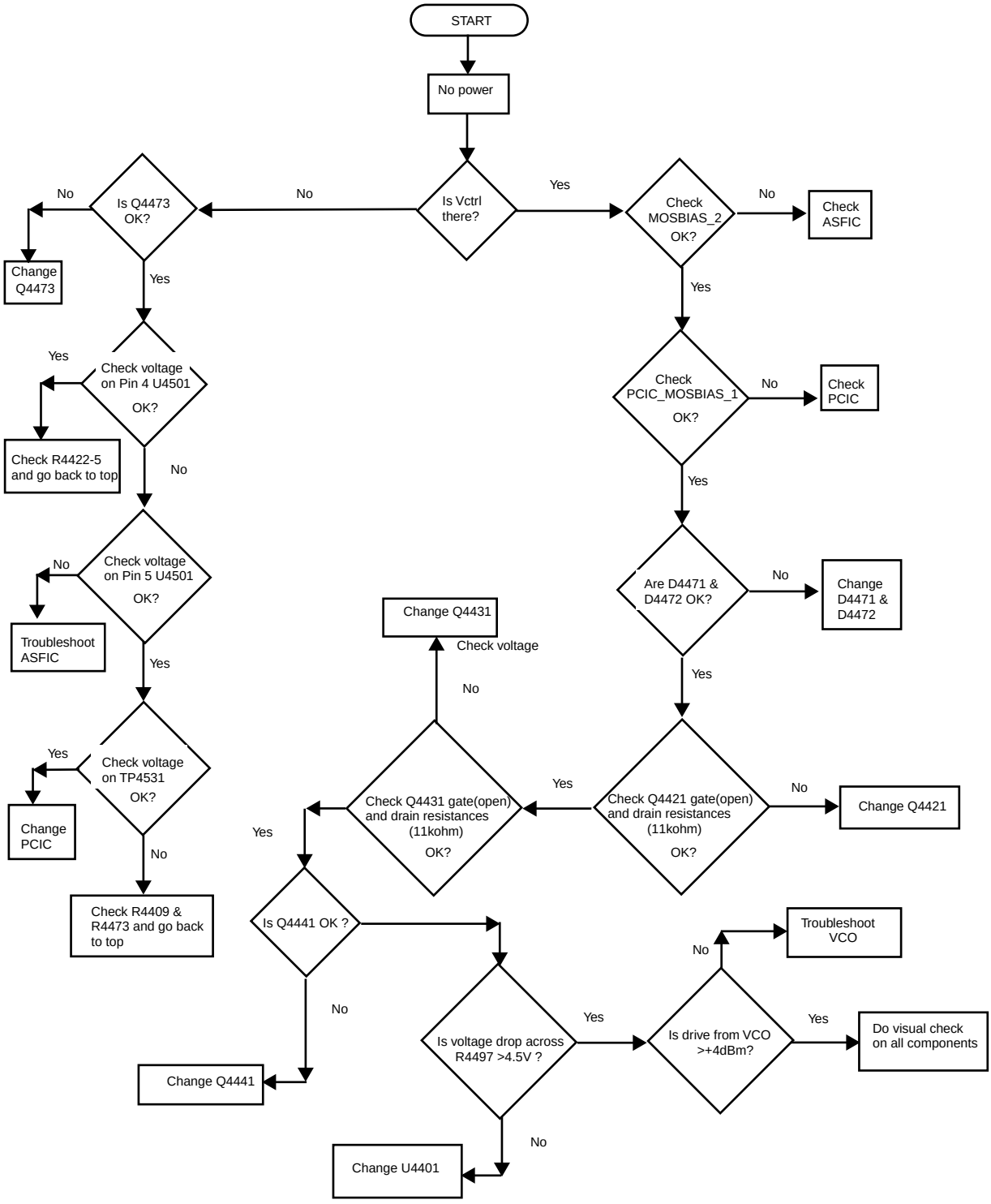
2.1 Troubleshooting Flow Chart for 25W Transmitter (Sheet 2 of 3)



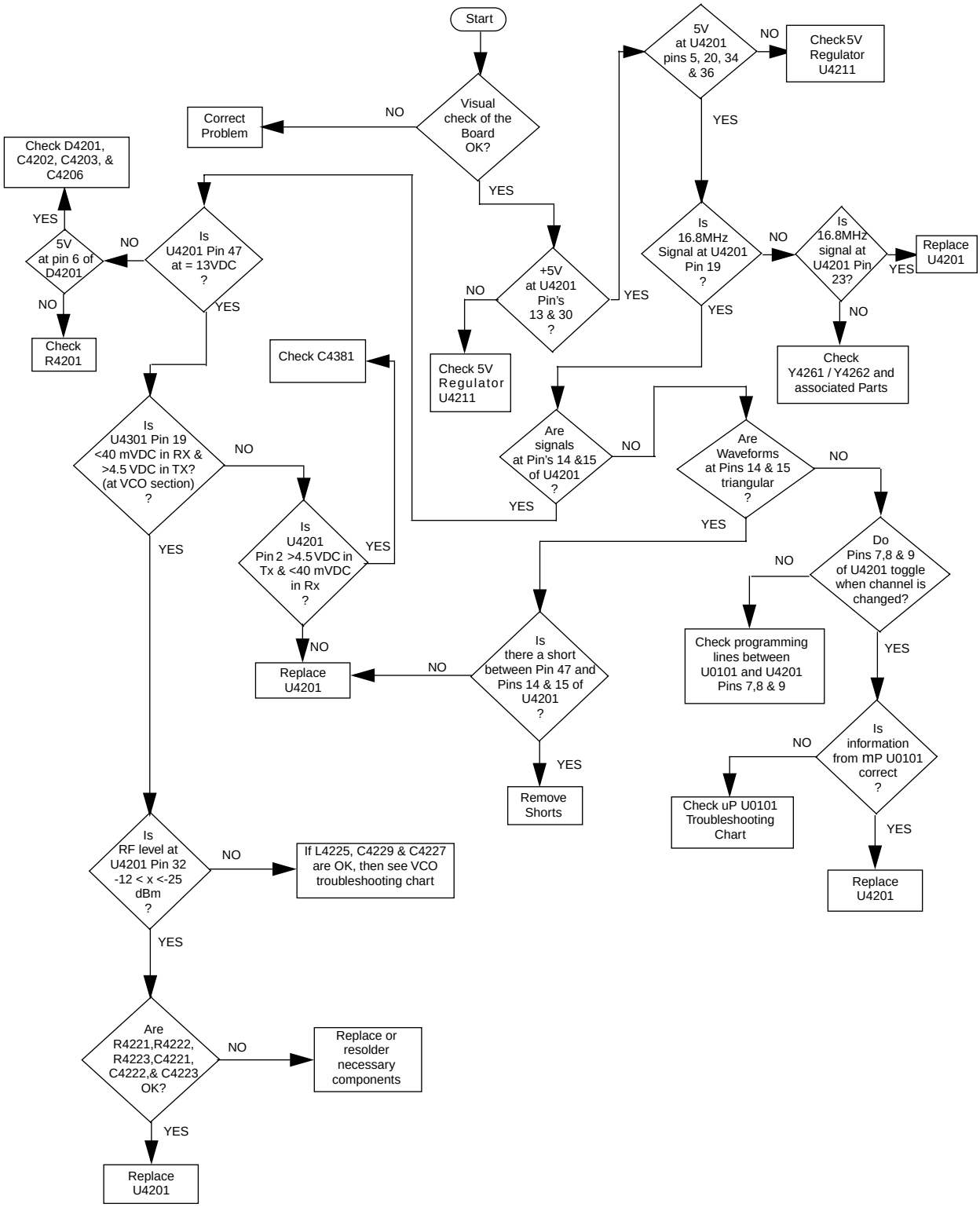
2.2 Troubleshooting Flow Chart for 25W Transmitter (Sheet 3 of 3)



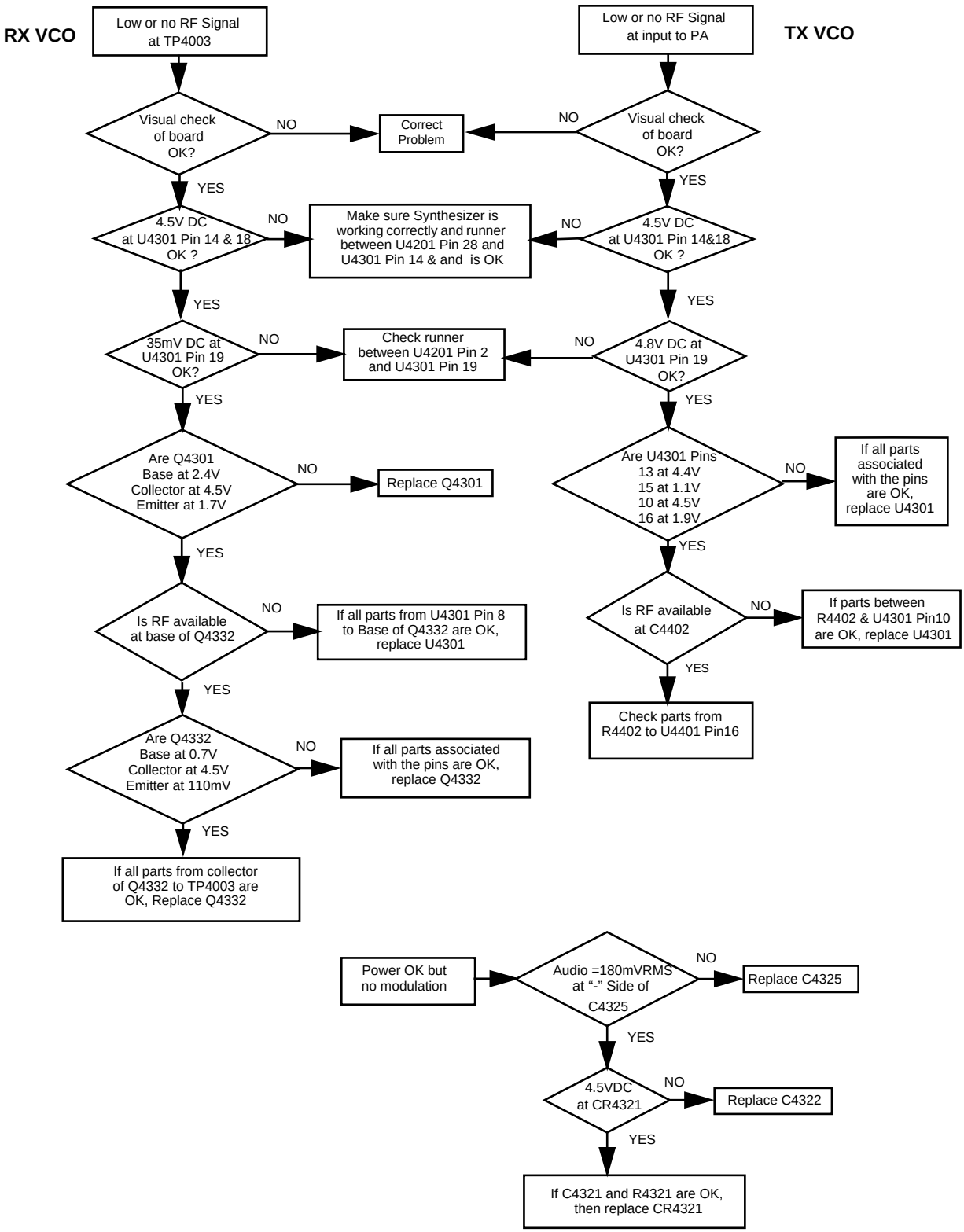
3.0 Troubleshooting Flow Chart for UHF 40W Transmitter



4.0 Troubleshooting Flow Chart for Synthesizer



5.0 Troubleshooting Flow Chart for VCO



Chapter 4

UHF PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

1.1 Controller Circuits

The UHF circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for the UHF circuits only, refer to the Controller section for details of the related Controller circuits . The PCB component layouts and the Parts Lists in this Chapter show both the Controller and UHF circuit components. The UHF schematics and the related PCB and parts list are shown in the tables below.

Table 4-1 UHF 1-25W Diagrams and Parts Lists

Table 4-2 UHF 25-40W Diagrams and Parts Lists

Table 4-3 UHF 1-25W Diagrams and Parts Lists

Table 4-4 UHF 25-40W Diagrams and Parts Lists