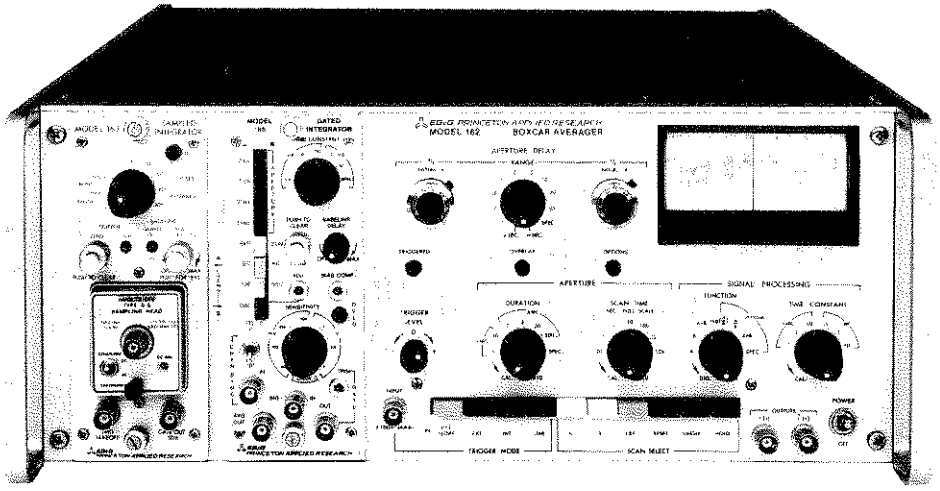
MODEL 162
BOXCAR AVERAGER

INCLUDING:
MODEL 163
SAMPLED INTEGRATOR
MODEL 164
GATED INTEGRATOR

READ SAFETY NOTICE PRECEDING
SECTION I BEFORE OPERATING
INSTRUMENT



OPERATING AND SERVICE MANUAL

EG&G
PRINCETON APPLIED RESEARCH

MODEL 162
BOXCAR AVERAGER

INCLUDING:
MODEL 163
SAMPLED INTEGRATOR
MODEL 164
GATED INTEGRATOR

OPERATING AND SERVICE MANUAL

EG&G PRINCETON APPLIED RESEARCH

M162; 6/82; 500; MtC

Printed in U.S.A.

SHOULD YOUR EQUIPMENT REQUIRE SERVICE

A. Contact the factory (609/452-2111) or your local factory representative to discuss the problem. In many cases it will be possible to expedite servicing by localizing the problem to a particular plug-in circuit board.

B. If it is necessary to send any equipment back to the factory, we need the following information.

(1) Model number and serial number.

(2) Your name (instrument user).

(3) Your address.

(4) Address to which instrument should be returned.

(5) Your telephone number and extension.

(6) Symptoms (in detail, including control settings).

(7) Your purchase order number for repair charges (does not apply to repairs in warranty).

(8) Shipping instructions (if you wish to authorize shipment by any method other than normal surface transportation).

C. U.S. CUSTOMERS—Ship the equipment being returned to:

EG&G PRINCETON APPLIED RESEARCH
7 Roszel Road
(Off Alexander Road, East of Route 1)
Princeton, New Jersey

D. CUSTOMERS OUTSIDE OF U.S.A.—To avoid delay in customs clearance of equipment being returned, please contact the factory or the nearest factory distributor for complete shipping information.

E. Address correspondence to:

EG&G PRINCETON APPLIED RESEARCH
P. O. Box 2565
Princeton, NJ 08540

Phone: 609/452-2111
TELEX: 84 3409

WARRANTY

EG&G PRINCETON APPLIED RESEARCH warrants each instrument of its manufacture to be free from defects in material and workmanship. Obligations under this Warranty shall be limited to replacing, repairing or giving credit for the purchase price, at our option, of any instrument returned, freight prepaid, to our factory within ONE year of delivery to the original purchaser, provided prior authorization for such return has been given by our authorized representative.

This Warranty shall not apply to any instrument which our inspection shall disclose to our satisfaction, has become defective or unworkable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation or other causes beyond our control. Instruments manufactured by others, and included in or supplied with our equipment, are not covered by this Warranty but carry the original manufacturer's warranty which is extended to our customers and may be more restrictive. Certain subassemblies, accessories or components may be specifically excluded from this Warranty, in which case such exclusions are listed in the Instruction Manual supplied with each instrument.

We reserve the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

THERE ARE NO WARRANTIES WHICH EXTEND BEYOND THE DESCRIPTION HEREIN. THIS WARRANTY IS IN LIEU OF, AND EXCLUDES ANY AND ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESSED, IMPLIED OR STATUTORY, INCLUDING MERCHANTABILITY AND FITNESS, AS WELL AS ANY AND ALL OTHER OBLIGATIONS OR LIABILITIES OF EG&G PRINCETON APPLIED RESEARCH, INCLUDING, BUT NOT LIMITED TO, SPECIAL OR CONSEQUENTIAL DAMAGES. NO PERSON, FIRM OR CORPORATION IS AUTHORIZED TO ASSUME FOR EG&G PRINCETON APPLIED RESEARCH ANY ADDITIONAL OBLIGATION OR LIABILITY NOT EXPRESSLY PROVIDED FOR HEREIN EXCEPT IN WRITING DULY EXECUTED BY AN OFFICER OF EG&G PRINCETON APPLIED RESEARCH.

TABLE OF CONTENTS

FIGURES

TABLES

SAFETY NOTICE
(READ BEFORE OPERATING INSTRUMENT)

A. INTRODUCTION

The Model 162 to which this instruction manual applies has been supplied in a safe condition. This manual contains some information and warnings that have to be followed by the user to ensure safe operation and to retain the instrument in a safe condition.

The described apparatus has been designed for indoor use.

B. INSPECTION

Newly received apparatus should be inspected for shipping damage. If any is noted, notify EG&G PARC and file a claim with the carrier. Be sure to save the shipping container for inspection by the carrier.

WARNING!

THE PROTECTIVE GROUNDING COULD BE RENDERED INEFFECTIVE IN DAMAGED APPARATUS. DAMAGED APPARATUS SHOULD NOT BE OPERATED UNTIL ITS SAFETY HAS BEEN VERIFIED BY QUALIFIED SERVICE PERSONNEL. DAMAGED APPARATUS WAITING FOR SAFETY VERIFICATION SHOULD BE TAGGED TO INDICATE TO A POTENTIAL USER THAT IT MAY BE UNSAFE AND THAT IT SHOULD NOT BE OPERATED.

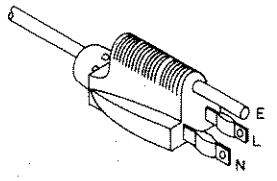
C. SAFETY MECHANISM

As defined in IEC Publication 348 (*Safety Requirements for Electronic Measuring Apparatus*), the Model 162 is Class I apparatus, that is, apparatus that depends on connection to a protective conductor to earth ground for equipment and operator safety. Before any other connection is made to the Model 162, the protective earth terminal shall be connected to a protective conductor. The protective connection is made via the earth ground prong of the power cord plug. The power cord plug shall only be inserted in a socket outlet provided with the required earth ground contact. The protective action must not be negated by the user of an extension cord without a protective conductor, by use of an "adapter" that doesn't maintain earth ground continuity, or by any other means.

WARNING!

ANY INTERRUPTION OF THE PROTECTIVE CONDUCTOR INSIDE OR OUTSIDE THE APPARATUS OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL MAY MAKE THE APPARATUS DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

The power cord plug provided is of the type illustrated in Figure 1. If the provided plug is not compatible with the available power sockets, the plug or power cord should be replaced with an approved type of compatible design.



L = LINE OR ACTIVE CONDUCTOR (ALSO CALLED "LIVE" OR "HOT")
N = NEUTRAL OR IDENTIFIED CONDUCTOR
E = EARTH OR SAFETY GROUND

Figure 1. POWER CORD PLUG WITH POLARITY INDICATIONS

WARNING!

IF IT IS NECESSARY TO REPLACE THE POWER CORD OR THE POWER CORD PLUG, THE REPLACEMENT CORD OR PLUG MUST HAVE THE SAME POLARITY AS THE ORIGINAL. OTHERWISE A SAFETY HAZARD FROM ELECTRICAL SHOCK, WHICH COULD RESULT IN INJURY OR DEATH, MIGHT OCCUR.

D. POWER VOLTAGE SELECTION

Before plugging in the power cord, make sure that the instrument is set for operation from the voltage of the ac power supply.

CAUTION!
THE APPARATUS DESCRIBED IN THIS MANUAL MAY BE DAMAGED IF IT IS SET FOR OPERATION FROM 110 V AC AND TURNED ON WITH 220 V AC APPLIED TO THE POWER INPUT CONNECTOR.

A detailed discussion of how to check and, if necessary, change the power voltage setting follows.

The line voltage is selected by means of a rear-panel switch. FOR SAFETY, UNPLUG THE POWER CORD WHEN CHECKING THE LINE VOLTAGE SETTING OR WHEN CHECKING THE POWER LINE FUSE (also located at the rear panel). FUSES SHOULD ONLY BE CHANGED BY QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE POSSIBLE SHOCK HAZARD. Depending on the switch position, either "115" or "230" (both are printed on the switch) will be visible to the viewer. For operation from a line voltage of nominally 115 V ac, the rear-panel fuse should be a slow-blow type rated at 1.0 A with a voltage rating of 125 V or higher. For operation from a line voltage of nominally 230 V ac, the rear-panel fuse should be a slow-blow type rated at 0.5 A with a voltage rating of 250 V or higher.

Make sure that only fuses with the required current and voltage rating, and of the specified type are used for replacement. The use of makeshift fuses and the short-circuiting of fuse holders are prohibited.

WARNING!
TO AVOID THE POSSIBILITY OF A SAFETY HAZARD FROM ELECTRICAL SHOCK WHICH COULD RESULT IN INJURY OR DEATH, DISCONNECT THE POWER CORD BEFORE REMOVING OR INSTALLING A FUSE.

E. VENTILATION

The Model 162 does not incorporate forced air cooling. However, with a power consumption of nominally 50 watts, provision must be made for adequate ventilation around the unit to prevent the internal temperature from reaching unacceptably high levels. This requirement is automatically satisfied during bench operation in a typical laboratory. If operated rack mounted, the user will have to take care that the ambient temperature in the rack not exceed 45°C.

F. DEFECTS AND ABNORMAL STRESSES

Whenever it is likely that the protection provided by the connection to earth ground has been impaired, the apparatus shall be made inoperative and secured against any unintended operation. The protection is likely to be impaired if, for example, the apparatus.

(1) Shows visible damage,

(2) Fails to perform the intended measurements,

(3) Has been subjected to prolonged storage under unfavorable conditions,

(4) Has been subjected to severe transport stresses.

Such apparatus should not be used until its safety has been verified by qualified service personnel.

G. DIGITAL STORAGE

Subsection 4.14 contains information relating to the operation, installation, and calibration of the Digital Storage Option. THE CALIBRATION AND INSTALLATION REQUIRE THAT THE COVER OF THE INSTRUMENT BE REMOVED, THUS EXPOSING POTENTIALLY LIVE TERMINALS. FOR THIS REASON, THE PROCEDURES OUTLINED IN SUBSECTION 4.14 SHOULD ONLY BE PERFORMED BY PERSONNEL EXPERIENCED IN WORKING ON ELECTRONICS CIRCUITRY AND WHO HAVE AN UNDERSTANDING OF THE SHOCK HAZARD INVOLVED. BEFORE REMOVING THE COVER, DISCONNECT THE INSTRUMENT FROM ALL POSSIBLE SOURCES OF VOLTAGE. Note that there are capacitors inside the Model 162 that may still be charged even if the instrument has been disconnected from all voltage sources. For this reason, after the instrument has been unplugged, service personnel are advised to wait several minutes before assuming that the capacitors are safely discharged.

H. OPTIONAL FUNCTIONS

Subsection 4.13C contains information relating to the operation, installation, and calibration of the Optional Function circuit cards. Since these cards cannot be installed without first removing the cover, the warnings contained in the preceding paragraph describing the safety considerations for the Digital Storage Option apply as well to these options.

SECTION I
CONDENSED OPERATING INSTRUCTIONS

The Condensed Operating Instructions are provided as an assistance in placing the Model 162 Boxcar Integrator into operation as quickly as possible, or as a handy "refresher" if the unit has not been operated in some time. Generally speaking, these condensed instructions will allow good results to be obtained in most instances. However, because of the brevity of these instructions, considerations that may be critical in a particular application have been foregone. Also, certain assumptions are made regarding operating parameters, and these assumptions will not be valid in all instances. In particular, operation of the options is not discussed. If operation with an option (including digital storage) is intended, first set up a simple "dummy" experiment and operate according to the condensed instructions to gain some operating familiarity with the instrument. Next read Subsection 4.13C, which discusses the various options. In any case, whether one intends to operate with an option or not, it will prove advisable to read all of Section IV to be assured of valid measurement data in every application.

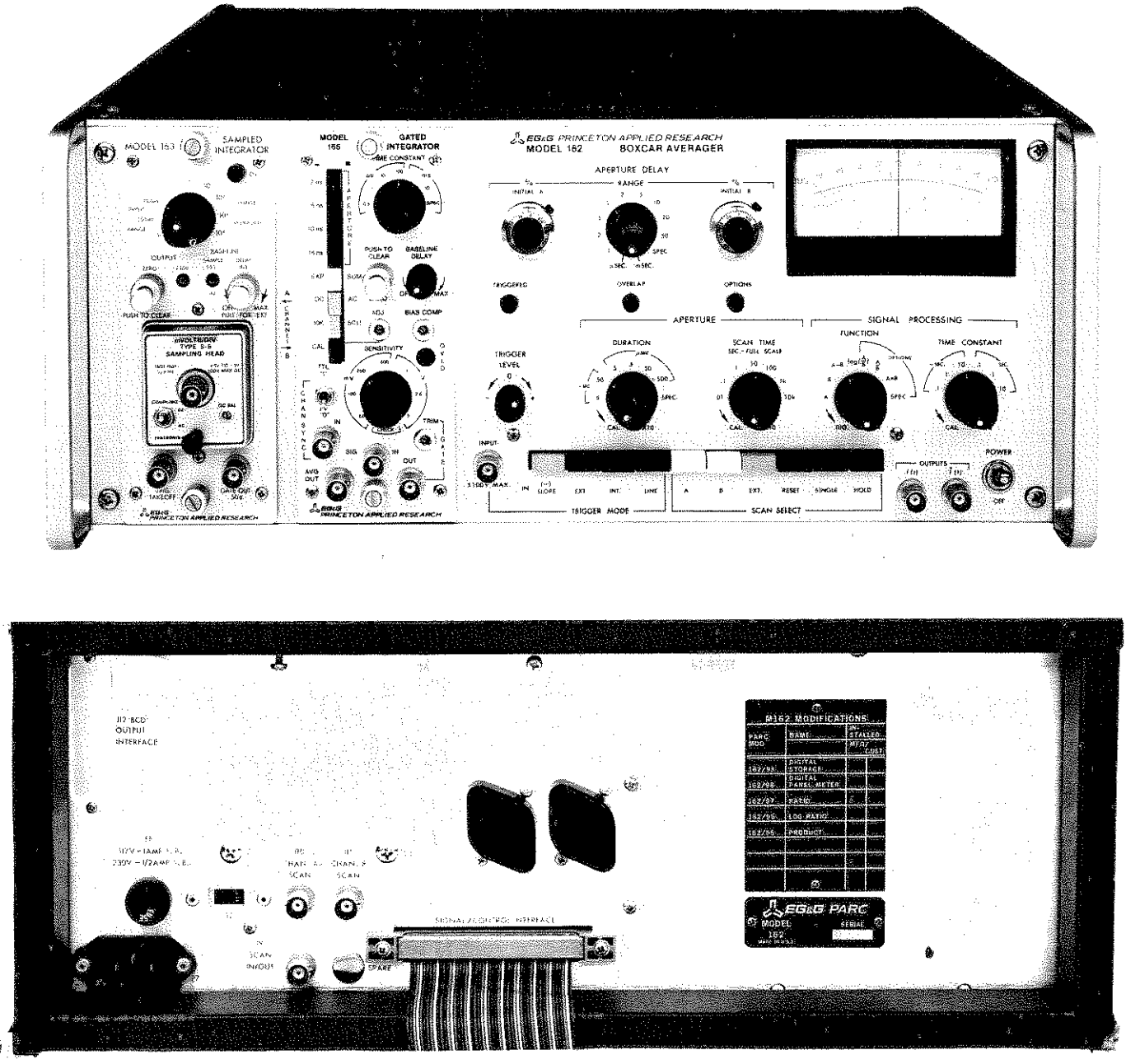


Figure I-1. MODEL 162 BOXCAR INTEGRATOR

STEP ONE

PRELIMINARY CONSIDERATIONS: Check that the rear-panel Line Voltage Selector is properly set. Plug in the Processor Module(s), with Sampling Head if a Model 163. Turn on the instrument power and allow a fifteen minute warmup. Set all SCAN SELECT pushbuttons to the released position. Set the main-frame Time Constant to .1 mSEC (multiplier to CAL). Function switch should be set to "A" or "B". Digital storage should be off (center knob of Function switch).

STEP TWO

TRIGGERING: Depress the EXT. Trigger Mode pushbutton. Then connect the externally derived trigger signal to the Trigger INPUT connector. Use the SLOPE pushbutton to determine on which slope of the applied signal triggering is to occur. Adjust the TRIGGER LEVEL control as required to establish proper triggering, as indicated by the TRIGGERED indicator lamp.

STEP THREE

APERTURE DELAY: Each trigger initiates an Aperture Delay Range interval as set by the APERTURE DELAY RANGE control. Signal to be processed must fall between trigger time and end of Aperture Delay Range interval. Set the APERTURE DELAY RANGE control as appropriate to achieve this timing requirement. Set % INITIAL A and B dials to 50% (five turns from fully counterclockwise position). These dials will be readjusted in later step.

STEP FOUR (M164)

M164 INITIAL ADJUSTMENTS: Depress GND and EXP pushbuttons. Then select the desired Coupling mode (AC or DC, 1 MΩ or 50 Ω) and connect the input signal to the M164 INPUT connector. At main frame, set APERTURE DURATION (affects M164 only) according to resolution requirements (effective rise time equals selected Aperture Duration). Set M164 TIME CONSTANT to 1 μSEC. Set FUNCTION switch (main frame) to "A" or "B", whichever corresponds to position of Processor Module being adjusted. Next adjust the M164 ZERO control for "0" panel-meter indication. The response time will be determined by the main-frame Time Constant (100 μs) and by the Observed Time Constant [M164 Time Constant ÷ (Aperture Duration x Trigger Repetition Rate)]. When Zero adjustment is completed, release GND pushbutton and depress CAL pushbutton. Then set the associated adjustment for full-scale panel meter indication. Release the CAL pushbutton. The signal source should be connected but with the signal "off".) Increase the M164 Time Constant as required for the anticipated signal-to-noise improvement needed (SNIR = $\sqrt{2TC/AD}$, where TC is M164 Time Constant and AD is the Aperture Duration). If two M164 Processor Modules are to be used, change the Function switch setting so that it corresponds to the position of the second module, and repeat the procedure for the second module. NOTE: To match the aperture durations in the two modules, monitor the M164 GATE OUT connectors with an oscilloscope and match pulse widths by means of the associated TRIM adjustments. If two Processor Modules are to be used and the other is a M163, go through the M163 INITIAL ADJUSTMENTS before proceeding to step 5.

STEP FIVE

SINGLE POINT ANALYSIS: Position aperture using % INITIAL A and % INITIAL B dials, whichever corresponds to Processor Module position. If two modules are in use, adjust both dials as required to locate apertures at desired points. The dials are direct reading in % of selected Aperture Delay Range, and so directly indicate the delay between the trigger time and the aperture. NOTE: Proper operation cannot be assured with dialed delays of less than 5%. Once the meter indication stabilizes, the meter will indicate the average value of the signal over the aperture duration interval. The FUNCTION switch should be set to "A" or "B", whichever corresponds to the module position. If two Processor Modules are in use, the FUNCTION switch will usually be set to "A-B". Do not select an option unless the unit in question is equipped with the option and the option function is understood. This includes DIGITAL STORAGE, which is selected with the inner knob. NOTE 1: Baseline Sampling and Digital Storage cannot both be selected at the same time. NOTE 2: SCAN SELECT "A" and "B" pushbuttons must both be in the released position for single-point analysis (these pushbuttons should still be in released position from step 1).

STEP FOUR (M163)

M163 INITIAL ADJUSTMENTS: Set the INPUT RANGE switch to 1 V and the SAMPLES AVERAGED switch to "1". The outer knob of the BASELINE SAMPLING control should be fully counterclockwise and the inner "pushbutton" should be "in". The main-frame FUNCTION switch should be set to "A" or "B", whichever corresponds to the position of the Processor Module being adjusted. Connect signal source impedance but with the signal "off". Adjust the M163 ZERO control for "0" panel meter indication (response time will be slow if trigger rate is low). Then set the INPUT RANGE switch to 100 mV and adjust the Sampling Head DC BALANCE adjustment for panel-meter "0". NOTE: A Sampling Head Extender (supplied with M163) is required to make DC BAL adjustment for any Sampling Head except the S-5, for which the DC BALANCE adjustment is located on the front panel. On all other Sampling Heads, the DC BALANCE adjustment is located on the left side, facing the instrument from the front. The main-frame power should be off anytime the Sampling Head is being plugged in or removed. Alternate between 1 V and 100 mV positions of INPUT RANGE switch, alternately adjusting the M163 ZERO and Sampling Head DC BALANCE adjustments until no further improvement in the meter "0" indication can be obtained. Remove the Sampling Head Extender and return the head to its proper position in the Model 163. (Power should be off for this step.) Apply input signal (any change in source impedance will necessitate re-adjusting of the ZERO control but not the DC BALANCE). Leave the INPUT RANGE switch set according to the anticipated signal amplitude. Set SAMPLES AVERAGED switch according to desired signal-to-noise improvement (varies as the square root of samples averaged). If Baseline Sampling is desired (with baseline sampling, module output is difference between level at signal sampling aperture position and level at baseline sampling aperture position; without baseline sampling, module output is difference between level at signal sampling aperture position and ground), monitor M163 GATE OUT connector with scope and adjust outer knob of BASELINE SAMPLING control to position baseline sampling aperture as desired (signal sampling aperture-position gate will also be observed; both gates will be 0.5 μs wide).

If two Processor Modules are to be used, change the FUNCTION switch setting so that it corresponds to the position of the second module. If second module is M163, repeat this procedure with second module. If second module is M164, go through M164 INITIAL ADJUSTMENTS before proceeding to step 5.

STEP FIVE

SCANNED ANALYSIS: If entire aperture delay range interval is to be scanned, set % INITIAL A dial, B dial, or both, as appropriate, to 5%. NOTE: Dials could be set fully counterclockwise. However, proper operation cannot be assured for the real time interval corresponding to the scanning of the first few percent of the Aperture Delay Range. If only a portion of interval is of interest, dials can be used to exclude part of range. Scan will begin at delay corresponding to dial setting and terminate at delay corresponding to end of selected Aperture Delay Range. If both channels are to be scanned, understand that scan will terminate when either aperture reaches 100% of the Aperture Delay Range. If only one scan is desired, SINGLE pushbutton should be depressed. Repetitive scans will take place if SINGLE pushbutton is in released position. Select the SCAN TIME as appropriate to the resolution and readout device requirements. The Scan Time is the time required to move the aperture position over the entire Aperture Delay Range interval. Minimum Scan Time commensurate with good resolution is computed differently for the two Processor Module types. For both, MST = 5 x Effective Time Constant x the ratio of the Delay Range to a Resolution Element. Effective Time Constant and Resolution Element are computed differently for the two module types. For the M163, a Resolution Element is simply the Sampling Head Rise Time (100 ps if Sampling Head Rise Time is less than 100 ps). Effective Time Constant = square root of sum of the squares of main-frame Time Constant and Observed Time Constant, where Observed Time Constant = selected SAMPLES AVERAGED (M163) divided by two times the trigger repetition rate. For the M164, a Resolution Element is the Aperture Duration itself. Effective Time Constant equals square root of sum of the squares of main-frame Time Constant and Observed Time Constant, where Observed Time Constant equals M164 Time Constant ÷ (Aperture Duration x Trigger Repetition Rate). If module is M163 and baseline sampling is being used, scan must be a factor of two slower than value computed. If two Processor Modules are to be scanned, scan times must be no faster than the slower of the two computation results. After setting SCAN TIME controls, depress SCAN SELECT "A", "B", or both pushbuttons as appropriate. Connect recording device and adjust its controls (X axis drive for X-Y plotter can be taken from rear-panel SCAN IN/OUT signal). Zero scan (dialed delay) can be established at any time by depressing SCAN SELECT RESET pushbutton. Set FUNCTION switch to "A" or "B", whichever corresponds to module position. NOTE: If two Processor Modules are in use, FUNCTION switch will usually be set to "A-B". Do not select an option unless unit in question is equipped with the option and the option function is understood. This includes DIGITAL STORAGE, which is selected with inner knob. NOTE: Baseline Sampling and Digital Storage cannot be selected at the same time. When ready to begin, depress RESET pushbutton to zero scan and then release RESET pushbutton to begin scan of record. Recording device will proceed to scan out the input signal waveform. Additional noise reduction can be obtained by increasing main-frame Time Constant. However, too much main-frame Time Constant will degrade resolution unless scan time is slowed further (see preceding statements on Scan Time computation).

Figure I-2. CONDENSED OPERATING INSTRUCTIONS

SECTION II
CHARACTERISTICS

2.1 INTRODUCTION

The Model 162 Boxcar Averager can be combined with one or two Model 163 or 164 Processor Modules to form a gated signal-recovery system of exceptional versatility. This system synchronously samples the input signal with an aperture that can be fixed at any point on, or slowly scanned across, the input signal. The signal passed through the aperture is applied to a variable time constant integrator, the output of which is the average of some number of repetitions of the input signal over the aperture duration. Because the average value of noise over a large number of repetitions is zero, an improvement in signal-to-noise ratio occurs. If the aperture is fixed on a single point of the input signal, the output of the Processor Module rises asymptotically towards the average value of the input signal at the sampled point. If the aperture is scanned across the input signal, the synchronous waveform is reproduced at the output at the scan rate.

The Model 162 Mainframe contains most of the timing and control functions, as well as the output signal-processing circuitry. There is provision for supplying the gated-and-averaged signal from either channel to the mainframe output. Alternatively, one can select the difference between the two gated-and-averaged signals at the mainframe output. With the addition of optional signal-processing circuit cards, the Model 162 can provide an output consisting of the product, ratio, or log of the ratio of the two averager channel outputs. Use of the digital storage option allows signals at extremely low repetition rates to be averaged. Prior to being made available at the Output connector, the mainframe output signal is smoothed by a low-pass filter. The time constant of this filter is adjustable from 100 μs to 100 s.

Front-panel delay controls are provided that permit the aperture in each channel to be delayed independently from about 5% to 100% of the Delay Range, selectable in 1-2-5 sequence from .1 μs to 50 ms. Pushbutton switches give a choice of external, internal, or line triggering, and permit independent selection of manual or automatic scanning for each channel. The scan time, the time required to scan the aperture across 100% of the selected Delay Range, can be set to any value from 10^{-2} s to 10^{5} s.

Each of the Processor Module types provides a unique set of operating characteristics, allowing the input parameters of the Model 162 to be optimized to a very wide range of signal-recovery applications. The Model 163 Sampled Integrator module utilizes a Sampling Head to achieve aperture resolutions from 100 ps to 1 ns according to the Sampling Head selected. The input sensitivity is switch-selectable from 100 mV to 1 V full-scale. There is provision for selecting the number of samples averaged and for baseline sampling. This latter function provides automatic compensation for dc drift and the effects of baseline wander.

The Model 164 Gated Integrator module offers a choice of aperture widths ranging from 10 ns to 5 ms. Pushbutton switches allow a choice of 50 Ω or 1 MΩ input impedance, ac or dc coupled, and the choice of either linear or exponential averaging. Both the module gain and aperture duration can be trimmed to provide an exact match between modules if two Model 164's are to be used in dual-channel operation.

Both the Model 163 and the Model 164 provide output and aperture monitors, output reset switches, and an Overload lamp to indicate overload. Both modules also provide a choice of the number of samples averaged. In the Model 163, a single switch selects the number of samples of which the output is the average. In the Model 164, the averaging Time Constant, together with the selected Aperture Duration, determines the number of samples of which the output is the average.

The built-in flexibility of the Model 162 makes it suitable for handling almost any application involving the examination of repetitive signals. Use of the ratio option in dual-channel operation, for example, permits automatic source compensation for fluctuations in the excitation power of pulsed lasers and transducers. Dual-channel operation also permits single-unit instrumentation in complex experiments such as time-shared dual-beam spectroscopy. As a single-channel or dual-channel gated averager, the Model 162 is ideally suited to such applications as time-of-flight studies, plasma physics research, fluorescence and phosphorescence decay, non-destructive testing, and turbulence studies in fluid mechanics. The use of plug-in signal channel modules and plug-in optional signal-processing function cards, when combined with its many built-in operating features, makes the Model 162 Boxcar Averager the most versatile gated signal averager available.

2.2 DESCRIPTION

2.2A INTRODUCTION

In its simplest form, boxcar averaging is a process of controlled sampling and averaging. The process involves repeatedly measuring the amplitude

of a specific point on a repetitive waveform while computing the average value of the measurements taken.

In some applications it is desirable to observe the shape of a repetitive waveform. This is accomplished in the Model 162 by time-scanning the sampling aperture across the waveform. The scanning rate is made slow enough to permit a sufficient number of samples to be taken in each segment of the waveform to assure accurate results. The output in the scanning mode is a reproduction of the input waveform slowed by the scan rate. An X-Y plotter can be used to obtain a hard-copy record.

2.2B BLOCK DIAGRAM DISCUSSION (A more detailed diagram and discussion is provided in Section VI)

Timing and Manual Delay: Figure II-1 is a simplified block diagram of the Model 162 Boxcar Averager together with the Models 163 and 164 Processor Modules. Referring to this diagram, note that a trigger signal synchronous with the signal being examined activates the Aperture Delay Range time-base generator. This generator produces a timing ramp (Figure II-2) that begins at time zero and continues to the end of the selected Aperture Delay Range.

In manual operation, the Aperture Delay Range time-base voltage is compared with the corresponding % Initial Delay control voltage. The gate opens at the time set by the % Initial Delay control. Each channel is provided with a separate % Initial Delay circuit, permitting the sampling switch of each channel to be operated at a different point on the Aperture Delay Range time base, if desired. Through the proper selection of the Aperture Delay Range and the setting of the % Initial Delay controls, any point on the repetitive waveform under study can be sampled.

Automatic Scan: When the Scan Select switches are set for automatic scanning, an internally generated scan ramp is also applied to the delay circuits. The % Initial Delay voltage and Scan Time ramp voltage are summed and sent to the Aperture Comparator which opens the gate. When the % Initial Delay control is set to its minimum position, the delay between the trigger and aperture position is determined solely by the Scan Ramp. Figure II-2 shows the time and amplitude relationships between the Aperture Delay Range time-base ramps, the Scan Ramp, and the aperture position. As the scan ramp ascends, the voltage applied to the Comparator rises, and the aperture opens slightly later relative to the trigger time with

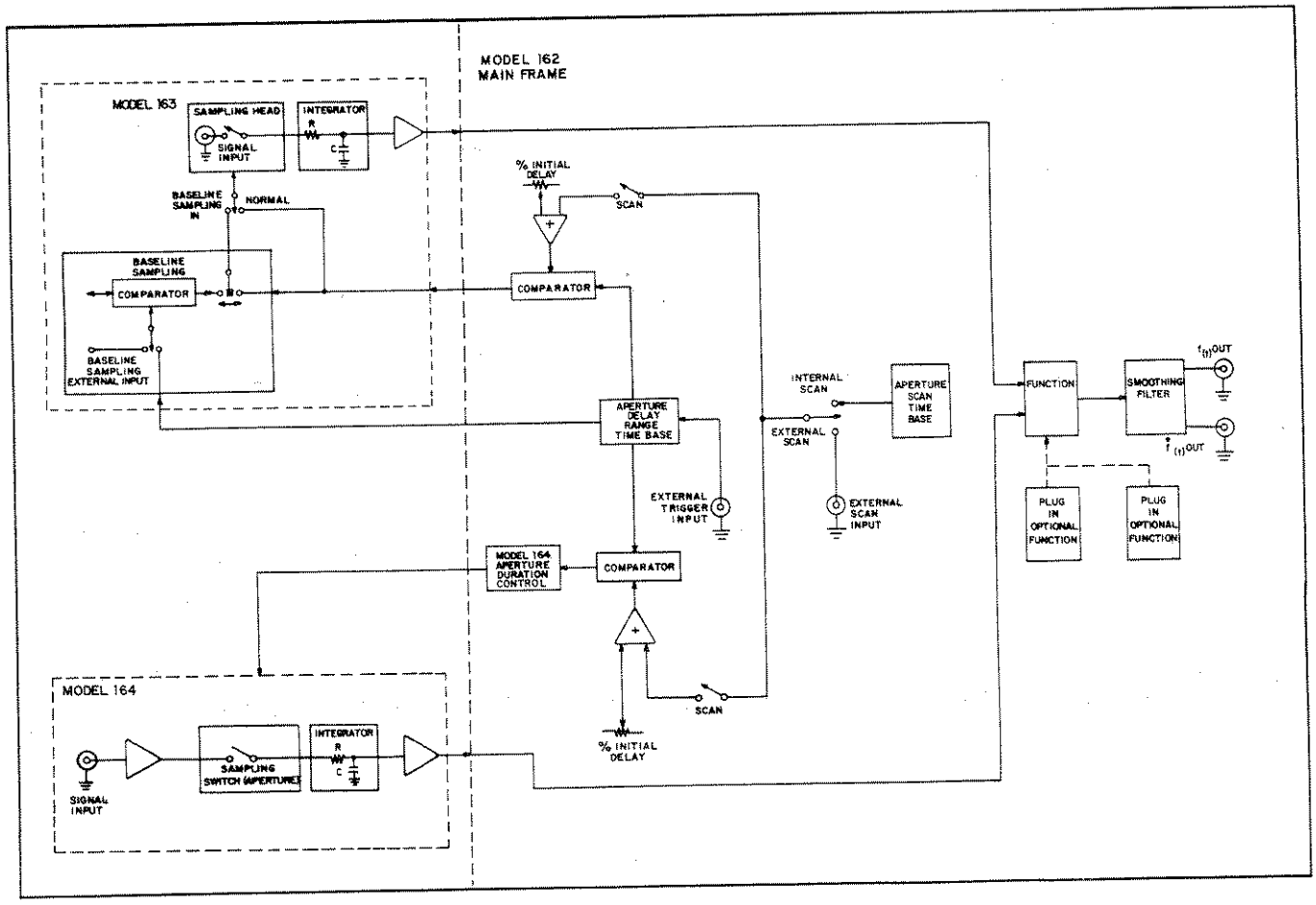


Figure II-1. SIMPLIFIED BLOCK DIAGRAM OF THE MODEL 162 WITH ONE M163 SAMPLED INTEGRATOR AND ONE M164 GATED INTEGRATOR INSTALLED

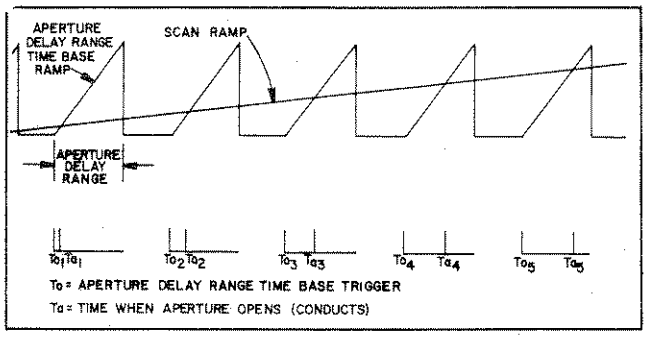


Figure II-2. TIME RELATIONSHIPS BETWEEN APERTURE DELAY RANGE, TIME BASE RAMPS, SCAN RAMP, AND APERTURE POSITION

each repetition. In effect, with each repetition, the aperture is positioned slightly later on the Aperture Delay Range interval.

When the % Initial Delay control is adjusted to a setting other than minimum, the comparator input voltage is "offset" by the amount of the dialed Initial Delay. As a result, the beginning of the aperture scan is time-shifted; the resulting scan is confined to an interval bounded at one end by the dialed Initial Delay, and at the other by the end of the selected Aperture Delay Range.

Aperture Duration and Averaging: The Aperture Duration (time for which the Sampling switch conducts with each repetition) depends on the Processor Module type. In the case of a Model 163, the aperture duration depends on the choice of Sampling Head. In the case of a Model 164, the aperture duration is determined by the mainframe Aperture Duration switch (this switch has no effect on the M163). For the interval that the gate conducts with each repetition, the input signal is applied to an integrating network, represented in Figure II-1 as a resistor-capacitor network. The capacitor charges towards the average potential over the aperture duration interval at a rate determined by the network time constant. When the gate is non-conducting, the input signal is disconnected, but the capacitor retains the charge acquired. With each successive aperture opening, the capacitor acquires additional charge. After a sufficient number of repetitions, the charge on the capacitor is essentially equal to the average value of the sampled signal segment. Noise is suppressed because its polarity and amplitude vary randomly in time, resulting in an average value of zero. The longer the network time constant and the shorter the aperture duration, the better the improvement in signal-to-noise ratio will be.

Digital Storage: Although the integrator circuitry is designed to retain the acquired capacitor charge, there is an inevitable slow discharge. This discharge is sufficiently low to be negligible in most applications. However, if the signal under study has a very low duty factor, the discharge can become a serious source of performance degradation. In such applications, it is advisable to equip the Model 162 with the Digital Storage Option. This option is basically a two-channel analog-to-digital-to-analog converter. When the Sampling switch opens at the end of each sample interval, the acquired charge is digitized and loaded into a digital storage register. The digital register contents are then read by a digital-to-analog converter which produces a dc voltage equal to the acquired charge on the capacitor. This dc voltage is fed back to the integrator to maintain its output potential at the same level until the next sample is taken, however long that may be. **NOTE:** During the "hold" interval between triggers, the output can drift as fast as 20 mV/minute, up to an *absolute maximum total* drift of 400 mV.

Output Signal Processing: The output of each Processor Module is applied to the mainframe Signal Processing circuitry. The Model 162 is supplied with three standard signal processing "functions", A only, B only, and A – B. In addition, there is provision for installing two plug-in optional function cards, if desired. Currently available options include A × B, A/B, and the log of A/B. User-designed and constructed optional functions can also be installed.

A front-panel switch selects the desired function. Whatever function has been selected is performed and the resulting signal applied to an output smoothing filter that provides additional noise suppression and meter damping. The smoothed signal is made available at the f(t) OUTPUT connector. A derivative output proportional to the rate of change of the output signal is also provided [f(t) OUTPUT]. If one of the optional functions is selected and the option in question has *not* been installed (including digital storage), a front-panel OPTIONS indicator lamp lights and there is no output.

Baseline Sampling: The Model 163 Processor Module is provided with a special baseline sampling function. When baseline sampling is selected, the sampling gate alternately samples the signal and then the baseline. The signal aperture position is determined by the % Initial Delay dial setting and Scan Ramp voltage as explained previously. However, the position of the baseline sample is determined solely by the M163 Baseline Sampling Delay control. A separate integrating circuit is provided to average the sampled segment of the baseline. In baseline sampling operation, the Model 163 output is the *difference* between the average value of the signal sample and the average value of the baseline sample. As a result, automatic compensation is provided for baseline wander.

2.3 APPLICATIONS

2.3A PICOSECOND DOMAIN FLUORESCENCE STUDIES

Interest in the study of fluorescence decay processes in the picosecond region has grown rapidly in recent years. Such processes yield information about molecular and crystal structure and provide insight into excitation processes which can help in defining reaction mechanisms.

The natural noise-producing processes and the usual extremely low light levels involved in picosecond time domain studies dictate the use of signal averaging techniques. In addition, the use of a boxcar averager permits the "time-translation" of the event under study from the picosecond domain to millisecond or second ranges where display on an oscilloscope or x-y plotter is feasible. The Model 162 with one or two Model 163 Processor Modules meets this need with a resolution as fine as 100 ps. Moreover, the baseline sampling mode built into the Model 163 enables it to automatically compensate for dc drifts in the detector or in the associated electronics. In dual-channel operation with the optional "ratio" function installed, the Model 162 can automatically compensate for fluctuations in the excitation source so that they do not include error in the resultant measurement. When the optional "log ratio" function is installed, the decay plot will appear as a straight line. In the case of a multiple decay function, the output may even appear as a series of connected straight-line segments, each with a different slope. In applications involving low repetition rates, use of the digital storage option allows results to be obtained that are as good as those one would normally consider to be achievable at high repetition rates only.

2.3B FLUORESCENCE AND PHOSPHORESCENCE DECAY STUDIES

Many fluorescence and phosphorescence studies fall well outside the picosecond domain and therefore do not require ultra-fast instrumentation. The Model 162 with one or two Model 164 Processor Modules is an economical approach to these studies. Gating resolution is continuously variable from 10 ns to 5 ms. Dual-channel operation with the optional "ratio" function installed provides automatic compensation for fluctuations in source power. Dual-channel operation also permits automatic compensation for baseline wander.

2.3C PULSED ULTRASONICS

The Model 162 can also be used in pulsed ultrasonics studies. Applications of pulsed ultrasonics to the study of materials and the examination of their internal structure are widespread. In this and other pulsed ultrasonic applications, the use of a boxcar averager permits separation of the echo originating in the region of interest from all other spurious signals while providing marked improvement in the signal-to-noise ratio.

2.3D PULSED RESONANCE EXPERIMENTS

In all applications of pulse-excited resonance, for both nuclear and electron resonance studies, application of a suitable signal averager permits the recovery of free induction decay waveforms and allows examination of the transitions induced by complex pulse sequences. Even though signals in these experiments are often extremely weak, and noise pickup by detectors is often a major problem, the boxcar averager easily separates the resonance signal from any obscuring influence.

2.3E LASER DEVELOPMENT

The use of pulse tchniques in laser development continues to gain acceptance as a practical and convenient method of determining operating parameters, even when the laser is being developed for continuous operation. This growing acceptance is due in part to the accuracy obtainable by this technique and in part to the simplifications in prototype laser construction made possible by the reduced heat dissipation of pulsed operation. The boxcar integrator, with its variable gate width and automatic scanning capability, is ideally suited to laser research. When extremely narrow pulses are being generated and very fine resolution is required, the Model 162 Boxcar Averager with the Model 163 Processor Module can provide resolution to 100 ps with built-in automatic baseline compensation that eliminates the effects of dc drifts. The use of two plug-in modules permits the Model 162 to simultaneously measure the output of two lasers and read the difference between their outputs, or optionally, the product, ratio, or log of the ratio. If a two-pen X-Y recorder is available, the output waveform of each laser can be plotted simultaneously for visual comparison. In some applications, particularly those involving high-power lasers, low duty factors are a must. The digital storage option permits the Model 162 to accurately average signals having an extremely low duty factor.

2.3F OPTICAL ABSORPTION STUDIES

Pulsed excitation is an attractive technique for making optical absorption measurements. This is due in part to the higher excitation powers, made possible by the reduced heat generated in the sample by pulsed excitation as compared to continuous excitation. The use of both channels allows one to also monitor the output of the pulsed exciter and automatically compensate for power fluctuations. If Model 163 plug-in modules are employed, automatic compensation for dc drifts in the detectors will also be provided so that the output is an accurate representation of the signal, free from outside influence. If Model 164

modules are employed, the continuously variable gatewidth permits the averaging parameters to be optimized to the signal source.

2.3G SAMPLING SCOPE

When used with an accessory oscilloscope, the Model 162 becomes a high-performance, variable-gatewidth, sampling scope. Actual performance parameters depend on the plug-in modules used. The Model 163 module offers a resolution from 100 ps to 1 ns, depending on the Sampling Head used, with automatic baseline compensation for ultra-fast *drift-free* sampling. The Model 164 module offers continuously variable gatewidths ranging from 10 ns to 5 ms, enabling the sampling time to be optimized to the signal under study. Dual-channel operation employing a pair of either type modules can provide simultaneous display of two waveforms if a dual-beam/dual-trace oscilloscope is available.

2.3H OTHER APPLICATIONS

EG&G PARC's Boxcar Averagers have already proven their worth in applications such as electroreflectance, pulsed Raman spectroscopy, measurement of non-linear electro-optical properties of materials using high-power pulsed-laser techniques, dual-beam magnetic resonance, spin-echo measurements, and ion-drift velocity investigations.

2.4 SPECIFICATIONS

2.4A MODEL 162 BOXCAR AVERAGER (MAINFRAME)

TIMING AND CONTROL

Trigger Modes:

(1) EXTERNAL: Unit can be triggered on either positive or negative going edge of external signal applied to a front-panel BNC connector. Trigger level is adjustable over a range of ± 15 V. Input impedance is 50 kΩ. Maximum input is ± 100 V. Minimum trigger duration is 10 ns. Minimum amplitude is 0.5 V baseline-to-peak.

(2) INTERNAL: Automatic repetitive triggering with period approximately equal to the selected Aperture Delay Range plus retrace time.

(3) LINE TRIGGERING: Unit can be triggered on either the positive or negative slope of ac power line voltage.

Maximum System Trigger Rate: For the Model 163, 10 kHz. For the Model 164, 5 MHz.

Aperture Delay: The interval between triggering and the beginning of the aperture opening can be independently adjusted for each channel from about 5% to 100% of the selected Aperture Delay Range by means of calibrated ten-turn % INITIAL DELAY dials (aperture may not open below 5%). Resultant delay will be that dialed plus a minimum delay of nominally 75 ns (max. 100 ns). There is also provision for automatically scanning the aperture time position from the set % delay to the end of the Aperture Delay Range. Nominal 75 ns minimum delay applies in scanned operation as well.

(1) APERTURE DELAY RANGE: Selectable in 1-2-5 sequence from 0.1 μs to 50 ms. There is also provision for a special user-installed range which allows one to obtain an Aperture Delay Range intermediate to, or longer than, those provided. The Aperture Delay Range setting is accurate to ± 2% of range. Accuracy of a specific dialed delay must take 75 ns (nominal) minimum delay into account as well.

(2) % INITIAL DELAY LINEARITY: Controls are linear to ± 0.25% of range or ± 3 ns, whichever is greater.

(3) DELAY JITTER: 50 ps rms or 0.05% of the selected Aperture Delay Range, whichever is greater.

Aperture Duration: A function of the type of Processor Module used.

(1) MODEL 163: Choice of 25 ps, 30 ps, 75 ps, 350 ps, or 1 ns fixed aperture as determined by the type of plug-in Sampling Head used. Resolution is limited to 100 ps by the delay jitter.

(2) MODEL 164: Aperture continuously variable from 10 ns to 5 ms. Aperture Duration control is located on front panel of mainframe. There is also a "special" range which can be used to achieve AD's intermediate to, or longer than, those provided. Minimum "special" AD is nominally 50 ns. A M164 Trim adjustment having a total range of 20% of the set aperture duration allows aperture duration matching in dual channel operation. Aperture duration selected at mainframe is obtained with TRIM set to center of range.

Aperture Position: Independent selection of manually adjusted delay or automatic scanning provided for each channel.

(1) MANUAL: Aperture position (delay between trigger and aperture) independently adjusted for each channel by % Initial Delay dials with full-scale delay being 100% of the selected Aperture Delay Range. **NOTE:** Reliable operation is uncertain with dialed delays of less than 5%. Also, total delay is dialed delay plus minimum of 75 ns nominal (max. is 100 ns).

(2) SCAN: Aperture position automatically scanned from dialed delay to 100% of selected Aperture Delay Range. One or both channels can be scanned, but scan rate is same for both. There is provision for controlling scan with internally or externally derived control signal. **NOTE:** If dial setting is less than 5%, aperture may not open while the first 5% of the Delay Range is being scanned. Normal operation over the remaining 95% is assured. Minimum 75 ns (nominal) delay applies in scanned operation as well as in manual.

(a) INTERNAL: Time required to scan aperture over *entire* Aperture Delay Range is that selected by SCAN TIME control, which allows scan times from 0.01 s to 100,000 s to be selected. *Actual* experimental time will be less if scan is restricted to only a portion of the Aperture Delay Range by using % INITIAL DELAY dials (scan always begins at dialed delay, not at "0"). Accuracy of selected Scan Time is ± 15% (multiplier to CAL. position).

(b) EXTERNAL: Scan time determined by external program applied to rear-panel SCAN IN/OUT connector. Sensitivity is 10% of Aperture Delay Range per + 1 V applied. Maximum program dV/dt is 10 V/ms. Input impedance is 10 kΩ. Maximum input without damage is + 20 V.

SIGNAL PROCESSING

Functions: The Model 162 is supplied with three standard output functions. Any two of four additional optional functions can be incorporated into the instrument, if desired. The optional function circuits are contained on plug-in circuit cards for which two mating connectors have been provided in the instrument, allowing the instrument to be equipped with no more than two options at one time. A front-panel OPTIONS light glows if an option is selected which has *not* been installed. **NOTE:** Limit of two options does not include Digital Storage.

(1) STANDARD FUNCTIONS

(a) Channel A Output only (A).

(b) Channel B Output only (B).

(c) Channel A Output minus Channel B Output (A – B).

(2) OPTIONAL FUNCTIONS

(a) MODEL 162/95, A × B: Channel A Output multiplied by Channel B Output. A × B Option has two modes of operation, A × B and A/|B|, as selected by switch on the Option Board. In the A × B mode, transfer function is $E_{OUT} = 0.1$ A × B. Product accuracy is ± 1% of full scale. In A/|B| mode, transfer function is $E_{OUT} = (A/|B|)$. Ratio accuracy is also ± 1% of full scale. **NOTE:** Accuracy specifications are for option only. Error introduced in option will be in addition to any error introduced elsewhere in the instrument.

(b) MODEL 162/97, A/|B|: Channel A Output divided by Channel B Output. Transfer function is $E_{OUT} = 10$ (A/|B|). Ratio accuracy is ± 0.7% of full scale. **NOTE:** Accuracy specifications are for option only. Error introduced by option will be in addition to any error introduced elsewhere in the instrument.

(c) MODEL 162/96, log (|A|/|B|): Logarithm of Channel A Output divided by Channel B Output. Transfer function is 4.00 $\log_{10}$ (|A|/|B|). Typical accuracy is as shown below. **NOTE:** Errors introduced by option will be in addition to any errors originating elsewhere in the system. Note that scale factor is 4 V per decade.

RATIO	OUTPUT	ERROR IN OUTPUT VOLTAGE AS A FUNCTION OF B MAGNITUDE		
|A|/|B|	4 $\log_{10}$ (|A|/|B|)	B = 10 V	B = 1 V	B = 100 mV
1.0	0 V	10 mV	10 mV	40 mV
0.316	–2.000 V	10 mV	20 mV	150 mV
0.10	–4.000 V	10 mV	40 mV	400 mV
0.0316	–6.000 V	10 mV	150 mV	--
0.01	–8.000 V	20 mV	400 mV	--
0.00316	–10.000 V	60 mV	--	--

(d) User designed and constructed function (SPECIAL). Blank circuit boards can be purchased from EG&G PRINCETON APPLIED RESEARCH.

Digital Storage Option: The Model 162/99 Digital Storage modification (option) provides the analog integrators with virtually infinite storage (holding) time. As installed (factory or field), two single-channel processor modules (Models 163, 164) may be accommodated with a single additional printed circuit board added to the mainframe (Model 162). Each channel comprises a unique Analog-to-Digital-to-Analog converter whose output reinforces the integrator's output and prevents loss of memory. Note that the Digital Storage Option can be installed *in addition to* any two of the previously described optional functions.

(1) ENCODE TIME: 1 ms ± 10%.

(2) ACCURACY: ± .1% of full scale (Dig. Storage only; will be in addition to any other errors).

(3) SHORT TERM HOLDING TIME: 2 mV/minute typical; ± 20 mV/minute maximum. Total drift for unlimited time will be no greater than ± 400 mV.

(4) LONG TERM HOLDING TIME: Virtually infinite for a ± 4% of full scale (± 400 mV) error.

Time Constant: Output smoothing filter with time constant adjustable in decade steps from 0.1 ms to 100 s. Continuously adjustable multiplier allows selected time constant to be increased by as much as × 10.

Outputs:

(1) ANALOG PANEL METER: Taut-band construction; ± 2% of full scale accurate; center-zero standard.

(2) DIGITAL PANEL METER (Option 162/98): 3½ digit display with digital output in BCD format provided at rear-panel connector. Meter accuracy is ± 0.1% ± 1 count. BCD output is in positive sense logic. Logic 0 = 0 V ± 0.2 V, 5 mA maximum sinking current. Logic 1 = + 3.5 V ± 1 V, 100 μA maximum sourcing current.

(3) ANALOG OUTPUT f(t): Smoothed output of function selected. ± 10 V corresponds to full scale. Output impedance is 1 kΩ. Taking the signal at the Processor Module OUT pinjack as E_{IN}, and that at the f(t) OUTPUT connector as E_{OUT}, the transfer function is:

$$\frac{E_{OUT}}{E_{IN}} = \frac{-1}{1 + j\omega T}$$

where ω is 2πf and T is the mainframe Time Constant.

(4) ANALOG TIME DERIVATIVE $\dot{f}(t)$: Output proportional to rate of change of Analog Output. Maximum out is ± 10 V. Output impedance is 1 kΩ. **NOTE:** Taking the signal at the Processor Module OUT pinjack as E_{IN}, and that at the $\dot{f}(t)$ OUTPUT connector as E_{OUT}, the transfer function is:

$$\frac{E_{OUT}}{E_{IN}} = \frac{kA}{9} \frac{1}{1 + 1/j\omega T}$$

where $\omega = 2\pi f$ and T is the mainframe Time Constant. A is a variable gain factor dependent on the setting of the inner knob of the Time Constant switch and varies from × 10 (CAL. position) to × 1 (× 10 position). Note that A is also a component of T. k is another gain factor set by an internal adjustment with range of × 1 to × 50. Factory setting for k is $10/2\pi$.

NOTE: No more than ± 20 V can be applied to the Analog or Analog Time Derivative Outputs without damaging circuitry.

System Gain Drift: Relative to full scale, less than 0.01%/°C and less than 0.1%/week.

System DC Drift: A function of the Processor Module. After a one-hour warmup the dc drift referred to the input is as follows.

(1) MODEL 163: 200 μV/°C typical, 10 μV/°C if Sampling Head is remotely operated and maintained at a constant temperature.

(2) MODEL 164: Less than 20 μV/°C.

GENERAL

Size: 17-1/8" W × 7" H × 18-1/4" D (43.5 cm W × 17.8 cm H × 46.4 cm D).

Weight: 27 lbs (12.3 kg).

Power Requirements: 105-125 or 210-250 V ac, 50-60 Hz, 50 VA maximum with typical loading.

Fuses: Rear-panel line fuse, 1.0 A SLOW-BLOW, 125 V, for operation from 105-125 V ac; 0.5 A SLOW-BLOW, 250 V, for operation from 210-250 V ac. Also, there are two internal fuses, 1/4 A, 125 V, SLOW-BLOW, that protect the ± 50 V supplies.

2.4B MODEL 163 SAMPLED INTEGRATOR

Hold Time (see 2.4D): Hold Time is defined in terms of the minimum trigger repetition rate that will result in no more than 1% of full-scale error. For the Model 163 the rate is 5 Hz in "normal" mode and 50 Hz in Baseline Sampling mode. In sampling scope applications, larger errors are generally tolerable allowing lower minimum trigger rates to be used. If the unit is equipped with the digital storage option, lower trigger rates without performance degradation due to hold-time limitations can be accommodated (see Digital Storage Option specifications).

Baseline Sampling:

(1) FREQUENCY: Every other repetition; signal sampling cycles and baseline sampling cycles alternate.

(2) BASELINE SAMPLE DURATION: Same as for signal sample.

(3) BASELINE SAMPLING AVERAGING: Same as for signal sampling averaging.

(4) M163 OUTPUT: Difference between average of signal sample and average of baseline sample. With Baseline Sampling not operative, output is difference between average of signal sample and ground.

(5) BASELINE SAMPLE POSITION: As set by front-panel uncalibrated control that allows baseline sample to be positioned over the range of about 5% to 100% of the Aperture Delay Range. Alternatively, position of baseline aperture can be set by externally derived voltage applied to M163 front-panel pin jack. **NOTE:** Control that sets position of baseline aperture also turns baseline sampling function on or off. Note that 75 ns (nominal) minimum delay applies to baseline sampling aperture delay as well as to signal sampling aperture delay.

(6) COMMON MODE REJECTION RATIO: >100:1 for signals <50% of full scale.

Input Characteristics:

(1) SENSITIVITY (full-scale): ±100 mV, ±250 mV, or ±1 V, switch selectable. Accuracy at each setting is ±2%.

(2) MAXIMUM SAFE INPUT: ±5 V. **NOTE:** Limit due to Sampling Head. Maximum input level can be raised by use of appropriate input attenuators.

(3) PARAMETERS THAT VARY AS FUNCTION OF SAMPLING HEAD TYPE:

Sampling Head Type	Input Impedance	Coupling	Aperture Duration*	Pk-pk Sampling Noise (Sam. Aver. set to 1)
S–1	50 Ω	dc	350 ps	5 mV
S–2	50 Ω	dc	75 ps	10 mV
S–3A	built-in probe; 100 kΩ shunted by 2.3 pF	dc	350 ps	20 mV
S–4	50 Ω	dc	25 ps	10 mV
S–5	1 MΩ shunted by 15 pF	ac/dc	1 ns	2 mV
S–6	50 Ω	dc	30 ps	10 mV

*NOTE: Effective Aperture Duration limited to 100 ps by delay jitter of Model 162/163.

Table II-1. SAMPLING HEAD PARAMETERS

Signal-to-Noise Improvement: Dependent on number of samples of which the M163 output is the average. This number, selectable in decade steps from 1 to 10^4 by front-panel SAMPLES AVERAGED switch, applies when the actual number of repetitions is large relative to the selected SAMPLES AVERAGED. Improvement in signal-to-noise ratio varies as the square root of the selected SAMPLES AVERAGED. When using baseline sampling, baseline samples are averaged in the same manner as signal samples. **NOTE:** Sampling doesn't "stop" after the selected number of samples have occurred.

Linearity: The deviation of the output from: (f.s.) × (IN), where f.s. is the output with a full-scale input applied and IN is the input expressed as a fraction of a full-scale input, is typically ±0.25%. This spec. is degraded at low duty factors.

Coherent Pickup: Less than 1 mV pk-pk referred to input. Varies with delay.

Dynamic Reserve: The peak-to-peak amplitude of wide band noise at the input can be as great as 30% of full scale. Higher levels can cause nonlinear operation. If the coherent plus non-coherent signal at the input exceeds full scale, the OVERLOAD indicator will light.

Zero: Zeroing is provided by a front-panel control. Total range is full scale with Baseline Sampling turned OFF. Total range with Baseline Sampling turned ON is nominally 20% of full scale. Zero range is not necessarily symmetrical with respect to "0" output.

Clear: Pushbutton switch resets output of all processor modules and digital storage option, if installed, to zero. Similar to CLEAR pushbutton in a Model 164.

Outputs:

(1) SIGNAL MONITOR OUTPUT: Inverted ±10 V full-scale module output available at front-panel pin jack. Output impedance is 1 kΩ. **NOTE:** No more than ±20 V can be applied to this output without damaging instrument.

(2) GATE OUT: 0.5 μs marker pulse to indicate aperture position. If baseline sampling is used, two 0.5 μs marker pulses are provided, one to show the position of the signal sampling aperture, the other to show the position of the baseline sampling aperture. *There is typically 10 ns delay between the time the aperture opens and the leading edge of the corresponding marker pulse.* Marker pulse amplitude is nominally +1 V into 50 Ω; +3 V into an open circuit. **NOTE:** No more than +20 V can be applied to this output without damaging the instrument.

(3) TRIGGER TAKEOFF: Limited rise-time replica of input signal available at this output. With noise-free input, this output can be used to trigger mainframe or other peripheral apparatus. The amplitude is twice that of the input signal. The source impedance is several kilohms and the baseline is at +2 V.

General:

(1) SIZE: 2-5/8" W × 6-5/8" H × 15" D (6.7 cm W × 16.8 cm H × 38.1 cm D).

(2) WEIGHT: 5 lbs (2.3 kg) maximum.

(3) POWER REQUIREMENTS: Power is supplied by Model 162 Mainframe.

2.4C MODEL 164 GATED INTEGRATOR

Input Characteristics:

(1) SENSITIVITY (full scale): ± 100 mV. Accuracy is ±2%.

(2) MAXIMUM SAFE INPUT: ± 10 V.

(3) INPUT COUPLING: ac or dc, switch selectable. Ac coupling time constant is one second. Pushbutton allows input circuit to be internally grounded for convenient zero adjustment.

(4) INPUT IMPEDANCE: 50 Ω or 1 MΩ shunted by 25 pF, switch selectable.

(5) DYNAMIC RESERVE: The Model 164 can accept wide-band input noise levels of four times full scale peak-to-peak. Higher input noise levels can cause non-linear operation. The OVERLOAD indicator will light when the coherent plus non-coherent input signal exceeds four times full scale.

Aperture Duration: Continuously variable from 10 ns (nominal minimum) to 5 ms by means of front-panel switch and multiplier. Also provision for user-installed "special" range for achieving aperture durations longer than, or intermediate to, those provided, down to a minimum of nominally 50 ns. M164 front-panel control allows aperture duration to be trimmed for matching aperture durations in dual-channel operation. Total range of trim is 20% of selected Aperture Duration. Selected aperture is obtained with TRIM set to center of range.

Sampling Noise: With minimum M164 Time Constant, pk-pk sampling noise referred to input varies with Aperture Duration as follows.

AD	Pk-Pk Sampling Noise
10 ns < AD < 100 ns	< 2 mV
100 ns < AD < 1 μs	< 1 mV
1 μs < AD < 10 μs	< 500 μV
10 μs < AD	< 200 μV

Hold Time: Hold time is defined in terms of the maximum trigger period that will result in no more than 1% of full-scale error. For the Model 164, this rate depends on the setting of the Aperture Duration and the Time Constant. For Aperture Durations less than 5 μs, $P_{MAX} = 4 \times 10^7 C\,(1 - e^{-AD/\tau})$. For Aperture Durations of 5 μs or longer, $P_{MAX} = 4 \times 10^8 C\,(1 - e^{-AD/\tau})$, where:

P_{MAX} is the maximum allowable trigger period in seconds,
AD is the Aperture Duration in seconds,
τ is the Time Constant in seconds as selected by the M164 Time Constant switch, and
C is the value of the integrating capacitor as determined by the setting of the Time Constant switch. The value of C as a function of the switch setting is:

Time Constant Setting	C, in Farads
1 μs	62×10^{-12}
10 μs	500×10^{-12}
100 μs	5×10^{-9}
1 ms	50×10^{-9}
10 ms	500×10^{-9}
SPEC	User-determined

NOTE: If the unit is equipped with the digital storage option, lower trigger rates can be accommodated without performance degradation.

Signal-to-Noise Improvement:

(1) SUMMATION (LINEAR) AVERAGING: Varies as the square root of the number of repetitions of the applied signal. Model 164 Time Constant and Aperture Duration have no effect on signal-to-noise improvement.

(2) The signal-to-noise ratio improvement varies as $\sqrt{2TC/AD}$, where: TC is the Model 164 Time Constant switch setting in seconds, AD is the Aperture Duration in seconds, the noise has an upper frequency limit of 1/2AD Hz, and where the measurement has continued for a minimum of five times the observed time constant. The observed time constant is defined as TC/(rr•AD), where: rr is the trigger repetition rate in repetitions per second and where the other parameters are as previously defined.

Time Constant: Front-panel switch allows choice of decade-spaced time constants from 1 μs to 10 ms plus SPECIAL, in which a Time Constant intermediate to, or longer than, those provided can be set by user-installed internal capacitor.

Linearity: When system has been zeroed and gain-calibrated, the deviation of the output from (f.s.) × (IN), where f.s. = full scale and IN = input expressed as fraction of full scale, is typically ± 0.1% of full scale. This spec. is degraded at low duty factors.

Coherent Pickup: Delay-variable; less than 2 mV pk-pk referred to input.

Zero: Zeroing provided by front-panel control with *total* range of 100 mV relative to input of M164. Range not necessarily symmetrical with respect to "0".

Clear: Pushbutton switch resets output of all Processor Modules and Digital Storage Option, if installed, to zero. Similar to M163 CLEAR pushbutton.

Outputs:

(1) SIGNAL MONITOR OUTPUT: Inverted ± 10 V full-scale module output available at front-panel pin jack. Output impedance is 1 kΩ. **NOTE:** No more than ± 20 V can be applied to this output without damaging instrument.

(2) GATE OUT: Marker pulse equal in duration to selected Aperture Duration is provided at front-panel BNC connector. There is a 10 ns delay (nominal) between actual aperture opening and leading edge of marker pulse. Amplitude is nominally + 1 V into 50 Ω; + 5 V into open circuit. Width or marker pulse tracks aperture duration down to about 50 ns if terminated in 50 Ω.

Gain Calibration: 100 mV ± 0.25% internally developed voltage is available for calibrating M164 gain using front-panel Gain Adjustment which has range of ± 10% of full scale. Permits gain matching in dual-channel operation.

General:

(1) SIZE: 2-5/8" W × 6-5/8" H × 15" D (6.7 cm W × 16.8 cm H × 38.1 cm D).

(2) WEIGHT: 2 lbs (0.9 kg) maximum.

(3) POWER REQUIREMENTS: Power is supplied by Model 162 mainframe.

2.4D ACCESSORIES

Model 115 Wideband Preamplifier (see page VII-27 for Interface Cable).

Characteristics	Low Impedance Input	High Impedance Input	High Impedance Input w/10:1 Probe
Input Impedance (dc to 50 MHz)	50 Ω (± 10%)	1 MΩ shunted by 20 pF	10 MΩ shunted by 10 pF
Input Coupling	dc, gnd.	dc, ac, gnd.	dc, ac, gnd.
Maximum Input Voltage	± 5 V pk	± 5 V pk	± 500 V pk
Input Noise (R_s = 50 Ω, f = 100 Hz, BW = 1 Hz)	20 nV/$\sqrt{Hz}$	50 nV/$\sqrt{Hz}$	4 μV/$\sqrt{Hz}$
Input Noise (R_s = 50 Ω, BW = 50 MHz)	10 μV rms	50 μV rms	500 μV rms
Frequency Response + 1 dB, − 3 dB	dc to 70 MHz	dc to 50 MHz	dc to 50 MHz
Rise Time	5 ns	7 ns	8 ns
Voltage Gain	× 100 or × 10 switch-selectable		× 10 or × 1 switch-selectable
Gain Stability	± 0.5%	± 0.5%	± 1%
Dc Stability (Ref to Input)	± 100 μV/°C	± 100 μV/°C	± 1 mV/°C
Output Voltage	± 500 mV into 50 Ω		
Detector Bias Supply	− 1 V to − 100 V at 150 μA. Adjustable with front panel control. Stability is ± 2%.		
Power Requirements	+ 12 V @ 100 mA, − 12 V @ 80 mA, supplied by Model 162.		
Temperature Range	10°C to 45°C.		
Dimensions	8.6" W × 4.1"H × 11.3"D.		
Weight	5 lbs.		

SECTION III
INITIAL CHECKS

3.1 INTRODUCTION

The following procedure is provided to facilitate initial performance checking of the Model 162 Boxcar Averager and its associated Processor Modules. This procedure should be performed after inspecting the instrument for shipping damage (any noted to be reported to the carrier and to EG&G PRINCETON APPLIED RESEARCH), but before using it to make measurements. Should any difficulty be encountered in carrying out these checks, contact the factory or the authorized factory representative. It might be mentioned that it is not the purpose of these checks to demonstrate that the instrument meets its specifications, but rather simply to show that it has arrived in good working order. Each instrument receives a painstaking alignment and checkout before leaving the factory and users can have a high degree of confidence that their Model 162 will meet or exceed all specifications if no shipping damage has occurred. The following checks will usually reveal any such damage.

Note that the checkout procedure calls for operating the Model 162 in conjunction with either a Model 163 or a Model 164. If the customer has two modules, either of different types or both the same type, they should be checked out one at a time. Once each has been checked, dual-channel checks can be performed as indicated in Subsection 3.6

3.2 EQUIPMENT NEEDED

(1) Square-wave source capable of furnishing 0-to-100 mV 1 kHz square waves and 0-to-1 V 1 kHz square waves, the two to be synchronous. It should be possible to set the 100 mV level to within a few percent of the desired level. The 1 V level, however, is not critical as long as the amplitude is high enough to trigger the M162 ($\pm$ 0.5 V minimum). This is most easily done by using a 1 V source followed by a 10:1 attenuator, arranged such that the 1 V square wave can be applied to the Ext. Trigger input of the Model 162 and the 100 mV square wave can be applied to the Signal Input of either the Model 163 or the Model 164. The 100 mV source should be such that the amplitude will be 100 mV *when loaded with 50* Ω. The 1 V source will be driving the 50 kΩ input impedance of the Trigger Input so that loading considerations for the 1 V signal should not be critical.

NOTE 1: If the Processor Module is a Model 163 equipped with either a Type S-3A or S-5 Sampling Head, the signal input impedance will be high (100 kΩ and 1 MΩ respectively), simplifying input loading considerations for the 100 mV source as well. If the Processor Module is a Model 164, plan to use the 50 Ω input impedance. The TEKTRONIX type 114 Pulse Generator is a suitable signal source.

NOTE 2: If the available generator does not produce a square wave that is unipolar with respect to ground, but rather one that goes plus and minus, the procedure will have to be adapted to the generator characteristics. With a unipolar generator, the sampled levels will be + 100 mV and 0 V. In the case of a generator that swings plus and minus at the output, the sampled levels will be + 50 mV and − 50 mV, and the indicated M162 output levels will change accordingly.

NOTE 3: A basic assumption underlying this procedure is that the generator trigger output and signal output are in phase. Some generators provide a trigger output that is 180° out of phase with the signal output. Where this is the case, be sure to select negative-slope triggering at the Model 162 mainframe, even though the instructions call for triggering on the positive slope.

(2) Oscilloscope suitable for monitoring 1 μs 5 V pulses.

(3) Watch with second hand, or a stop watch.

(4) Coaxial cables having a characteristic impedance of 50 ohms and fitted with BNC connectors.

3.3 PRELIMINARY STEPS

(1) Check the position of the rear-panel Line Voltage Selector switch. For operation from a line voltage in the range of 105-125 V ac, "115" should show in the switch window. For operation from a line voltage in the range of 210-250 V ac, "230" should show.

(2) Plug the Processor Module into the "A" (left-hand) module receptacle. If the module is a Model 163, first plug the Sampling Head (TEKTRONIX S-1, S-2, S-3A, S-4, S-5, or S-6) into the module. **NOTE:** If the Sampling Head is other than a Model S-5, it will be necessary to mount the Head on an Extender (supplied) to give access to the DC BALANCE adjustment (left side facing unit from front). In the case of an S-5, the DC BALANCE adjustment is on the front and use of the extender is not required. Most Sampling Heads also have a right-side

adjustment. This right-side adjustment ABSOLUTELY SHOULD NOT BE DISTURBED. Next plug in the line cord and turn the Power switch on. If Sampling Head is an S-5, select dc coupling. The meter reading may be either on or off scale, depending on the setting of the front-panel controls. The front-panel indicator lamps may or may not be on. Allow about five minutes for the instrument to warm up before proceeding.

3.4 PROCEDURE IF PROCESSOR MODULE IS MODEL 163 (If Model 164, go to Subsection 3.5)

(1) Set the controls as follows.

Mainframe
% Initial A: 75% (ten turns is 100%)
% Initial B: fully counterclockwise
Aperture Delay Range: 1 mSEC
Aperture Duration: setting immaterial
Scan Time: 10 SEC (mul. to CAL)
Function: A (digital storage selector OFF)
Time Constant: .1 mSEC (mul. to CAL)
Trigger Mode pushbuttons: EXT depressed; all others released
Scan Select pushbuttons: all released

Model 163
Input Range: 1 V
Samples Averaged: 1
Baseline Sample Delay: fully counterclockwise; center pushbutton depressed
Coupling (sampling-head switch, if present): DC

(2) Triggering

(a) Connect the 0-to-1 V square wave at 1 kHz to the Trigger INPUT connector (mainframe front panel).

(b) Adjust the TRIGGER LEVEL control (mainframe front panel) as required to establish proper triggering as indicated by a steady glow of the TRIGGERED lamp (mainframe).

(3) Zero and DC Bal.

(a) Leaving 1 V trigger line connected, connect the signal generator to the M163 input. Then turn the generator off and select INT. triggering at the M162. (Internal triggering may not start the first try. If this happens, release and depress the INT. Trigger pushbutton until internal triggering is established as indicated by the TRIGGERED lamp.) The objective of this step is simply to connect the M163 input to the signal source resistance but without a signal.

(b) Adjust the M163 ZERO control for "0" panel meter indication.

(c) Change the setting of the INPUT RANGE switch to 100 mV. Then adjust the Sampling Head DC BAL adjustment for "0" on the panel meter.

(d) Return the INPUT RANGE switch to 1 V and adjust Zero again. Continue in this manner, alternating between the 1 V and 100 mV position while adjusting the ZERO and DC BAL adjustments until no further improvement in the "0" indication can be made. Leave the INPUT RANGE switch set to 100 mV.

When the Zero Adjustment and DC Balance Adjustments are completed, remove the extender, if appropriate, and return the Sampling Head to its normal position. The power should be off and the signal disconnected for this operation. Reconnect the cable interconnecting the signal source and the M163 input when the Sampling Head is in its normal operating position.

(4) Signal Processing—Manual Delay

(a) Turn the signal generator on and select EXT. triggering at the M162 mainframe. Then adjust the M163 ZERO control (only) for "0" panel meter indication. **NOTE:** The assumption is that the 0 V level of the 100 mV square wave is being sampled. If the square wave is swinging ±50 mV, no zero adjustment will be possible, and the best one can do is to adjust the ZERO control for a nominal −50% of f.s. M163 panel meter indication.

(b) Set the % INITIAL DELAY A dial to 10%. The panel meter indication should be nominally full-scale to the right. The tolerance will be that of the 100 mV input signal amplitude plus or minus the gain tolerance of the M162/163.

(c) Adjust the signal amplitude at the source to get the desired full-scale indication.

(d) Begin rotating the % INITIAL A dial clockwise. At about the 50% point the meter indication will drop to "0", indicating that the lower level of the 0-to-100 mV square wave is being sampled. The actual point where the crossover from full-scale to "0" occurs will vary according to the symmetry of the input square wave. From 50% to 100% delay (five revolutions to ten revolutions, the maximum), the "0" indication will be maintained. If the period of the input signal is a bit short, towards

100% delay the meter indication might rise again to full scale, indicating that the upper level of the next cycle is being sampled. After verifying the indicated behavior, leave the % INITIAL DELAY dial set to 10%.

(5) Signal Processing—Scanned Operation

(a) Depress the SCAN SELECT "A" pushbutton.

(b) Hold in the SCAN SELECT RESET pushbutton. While the button is held down, the panel meter will indicate nominally full scale. At some convenient time, release the RESET pushbutton. The panel meter will continue to indicate full scale for about four seconds, indicating that the upper level of the input square wave is being scanned. Then the indication will drop to "0", where it will remain for about five seconds as the lower level of the square wave is scanned. These nine second (nominal) "cycles" of four seconds of full-scale indication followed by five seconds of "0" indication will follow one another automatically.

(6) Baseline Sampling and Gate Out

(a) Connect the oscilloscope signal input to the M163 GATE OUT connector. The oscilloscope should be triggered on the positive edge of the same signal as is being used to trigger the Model 162 (negative edge if trigger and signal are 180° out of phase). The sweep time should be 100 μs per cm.

(b) A 0.5 μs marker pulse should be visible on the oscilloscope. As the scan cycles repeat, this marker pulse will be observed to "slide" across the trace, taking nominally nine seconds to complete each scan. At the end of each scan, the pulse position will reset to the sweep beginning and then start to scan again.

(c) Turn the BASELINE SAMPLE DELAY control (M163) clockwise. As soon as the control is rotated off the fully counterclockwise position, a second 0.5 μs pulse will be noted. This one will not scan. Its position is determined by the setting of the BASELINE SAMPLE DELAY control. With the control as far counterclockwise as it can be without turning the Baseline Sampling function off, the second pulse will be positioned near the beginning of the scope trace. With the control fully clockwise, this pulse will be at the end of the trace.

(d) Note the panel-meter indication as a function of the position of the two marker pulses. When both pulses are on the same half of the input square wave (both on the left half of the scope trace or both on the right half), the panel meter will indicate "0". When both pulses are on opposite halves of the trace, the panel meter will indicate nominally full scale, either plus or minus. When the signal aperture marker is on the left half of the trace and the baseline aperture marker on the right, full-scale positive output is obtained. When their positions are reversed, full-scale negative output is obtained. If the oscilloscope has dual-sweep capabilities, it may prove instructive to monitor the input signal simultaneously so that the position of the apertures relative to the input square wave can be more easily seen.

NOTE: this completes the Initial Checks for a system consisting of a Model 162 and a single Model 163. If there is a second Model 163 to be checked, plug it into module receptacle "B", and return to step 1 of Subsection 3.4, the only differences being that the FUNCTION switch, instead of being set to "A", is set to "B", and that the settings of the % INITIAL A and % INITIAL B dials must be reversed. Once the second one is checked out, go to Subsection 3.6 to check dual-channel operation.

3.5 PROCEDURE IF PROCESSOR MODULE IS MODEL 164

3.5A CHECKS IN THE EXTERNAL TRIGGER MODE

(1) Set the controls as follows.

Mainframe

% Initial A: 10% (one revolution from fully counterclockwise position)
% Initial B: same as % Initial A
Aperture Delay Range: 1 mSEC
Aperture Duration: 5 μSEC (mul. to CAL)
Scan Time: 10 SEC (mul. to CAL)
Function: A (digital storage OFF)
Time Constant: .1 mSEC (mul. to CAL)
Trigger Mode pushbuttons: EXT depressed; all others released
Scan Select pushbuttons: all released

Model 164

Time Constant: 1 μSEC
Pushbuttons: EXP/SUM, CAL, GND, and DC/AC depressed; all others released

(2) Triggering

(a) Connect the 1 V trigger signal at 1 kHz to the Trigger INPUT connector (mainframe front panel).

(b) Adjust the TRIGGER LEVEL control as required to establish proper triggering as indicated by a steady glow of the TRIGGERED lamp (mainframe).

(3) Zero and Gain Calibration

(a) Adjust the Model 164 ZERO control for "0" panel meter indication.

(b) Release the GND pushbutton. Then set the screwdriver adjustment associated with the CAL pushbutton for exactly full-scale panel meter indication.

(c) Release the CAL pushbutton.

(4) Signal Processing—Manual Delay

(a) Leaving 1 V trigger connected, connect the 0-to-100 mV square wave to M164 INPUT. **NOTE:** Be sure to take the loading effect of the 50 Ω input impedance into account; the signal should be 100 mV loaded with 50 Ω.

(b) Note the panel meter indication, which should be nominally full-scale to the right. The tolerance is simply that of the source signal amplitude. Adjust the source amplitude as required to get exactly full-scale meter indication.

(c) Begin rotating the % INITIAL A dial clockwise. At about the 50% point the meter indication will drop to "0", indicating that the lower level of the 0-to-100 mV square wave is being sampled. The actual point where the crossover from full scale to "0" occurs will vary according to the symmetry of the input square wave. From 50% to 100% delay (five revolutions to ten revolutions), the "0" indication will be maintained. If the period of the input signal is a bit short, towards 100% delay the meter indication might rise again to full scale, indicating that the upper level of the next cycle is being sampled. After verifying the indicated behavior, set the % INITIAL DELAY dial to 10%.

(5) Signal Processing—Scanned Operation

(a) Depress the SCAN SELECT "A" pushbutton.

(b) Hold the SCAN SELECT RESET pushbutton. While the button is held down, the panel meter will indicate nominally full scale. At some convenient time, release the RESET pushbutton. The panel meter will continue to indicate full scale for about four seconds, indicating that the upper level of the input square wave is being scanned. Then the panel meter indication will drop to "0", where it will remain for five seconds as the lower level of the square wave is scanned. These nine-second (nominal) cycles of four seconds of full-scale indication followed by five seconds of "0" indication will follow one another automatically.

(6) Summation Averaging Checks

(a) Release the SCAN SELECT "A" pushbutton and set the M164 Time Constant to 10 ms.

(b) Depress the M164 CLEAR pushbutton (meter indication will zero) and, while continuing to hold the CLEAR pushbutton down, release the M164 EXP/SUM pushbutton.

(c) At some convenient time, release the CLEAR pushbutton. The meter indication will begin rising linearly from zero and will reach full scale in about four seconds. It will not stop at full scale but will continue to rise until the stops are reached. **NOTE:** The exact timing is not very critical. Several factors affect the time required to reach full scale, among them the frequency of the input trigger signal, the tolerance of the Model 164 Time Constant, and the tolerance of the Aperture Duration. It should be noted that the trigger rate with a 1 kHz input trigger signal and a 1 ms Aperture Delay Range will be 500 Hz. (Because the cycle time with a 1 ms Aperture Delay Range is slightly longer than 1 ms, the unit triggers on every other cycle.)

(d) At some convenient time, depress the GND pushbutton (which latches) and the CLEAR pushbutton (which does not latch). The meter indication will instantly go to zero. When the CLEAR pushbutton is released, the meter indication will be observed to drift slowly away from zero. The drift could be in either direction.

(e) Depress the EXP/SUM pushbutton to restore exponential averaging.

3.5B INTERNAL TRIGGER MODE CHECKS

(1) Triggering

(a) Release the EXT Trigger pushbutton. The TRIGGERED lamp should extinguish.

(b) Depress the INT Trigger pushbutton. The TRIGGERED lamp should glow steadily again. **NOTE:** Although unlikely, it could happen that internal triggering will not start. If this is the case, alternately release and press in the INT pushbutton until internal triggering, as indicated by the TRIGGERED lamp, is established.

(2) Signal Processing

(a) Set the APERTURE DELAY RANGE to 10 mSEC. Check that the M164 Time Constant is 10 ms.

(b) Check that the GND pushbutton is still depressed. The meter ndication should be "0".

(c) At some convenient time, depress the CAL pushbutton and release the GND pushbutton (in that order). The meter indication will begin rising, approaching full scale asymptotically. The observed time constant will be nominally 20 seconds, that is, the meter will reach 63% of full scale in 20 s (the actual time required can vary somewhat as determned by the tolerances of the circuits involved). After 40 s, the meter indication should be nominally 86%, after 60 s it should be 95%, after 80 s it should be 98%, and after 100 s it should be within 1% of full scale. The actual time required to reach full scale may vary somewhat from these numbers. The important thing is that the general behavior indicated is observed.

(d) Depress the GND pushbutton (leave CAL depressed). The meter indication will now decrease, asymptotically approaching zero.

(e) Momentarily depress the CLEAR pushbutton. The meter indication will quickly go to "0".

3.5C HOLD CHECKS

(1) Zero Hold

(a) Decrease the M164 TIME CONSTANT to 100 μSEC.

(b) At some convenient time, release the INT Trigger pushbutton. The TRIGGERED light will extinguish, showing that the unit is no longer triggering.

(c) Note the panel meter indication. For as long as the unit is not triggering the meter indication drift should be less than 1% of full scale per second.

(2) Full-Scale Hold

(a) Depress the EXT Trigger pushbutton to restore triggering. The meter indication will quickly go to "0".

(b) Release the GND pushbutton (CAL should still be depressed). The meter indication will go to full scale in a few seconds.

(c) At some convenient time, release the EXT Trigger pushbutton.

(d) Note the panel meter indication. For as long as the unit is not triggering, the meter indication drift should be less than 1% of full scale per second.

NOTE: this completes the Initial Checks for a system consisting of a Model 162 and a single Model 164. If there is a second Model 164 to be checked, plug it into module receptacle "B", and return to step 1 of Subsection 3.5A, the only differences being that the FUNCTION switch, instead of being set to "A", is set to "B". Also, the SCAN SELECT A pushbutton should be released and the SCAN SELECT B pushbutton depressed. Once the second Processor Module is checked out, go to Subsection 3.6 to check dual-channel operation.

3.6 DUAL-CHANNEL OPERATION

These checks presuppose that the operator has two M163's or two M164's, and that both have been checked out according to the previous procedures. In other words, the ZERO and DC BAL or CAL adjustments, whichever is appropriate, have been made.

(1) Procedure with two M163's.

(a) Both modules should be plugged in and the controls should be set as indicated in step 1 of Subsection 3.4. The trigger input should be connected and the Trigger Level control adjusted for proper triggering. The 0-to-100 mV square wave should be connected to both inputs. **NOTE:** Take into account the change in loading caused by having the two inputs connected in parallel.

(b) Note the meter indication with the FUNCTION switch set to "A". Then set the FUNCTION switch to "B". The meter indication should be the same, plus or minus a few percent to allow for gain differences between the two modules.

(c) Set the FUNCTION switch to "A – B". The meter indication should go to "0", plus or minus a few percent of full scale.

This completes the dual-channel checks for a pair of Model 163's.

(2) Procedure with two M164's

(a) Both modules should be plugged in and the controls should be set as indicated in step 1 of Subsection 3.5A. The trigger input should be connected and the Trigger Level control adjusted for proper triggering. There is no need to connect the 100 mV signal; the Model 164 Processor Modules are checked using the internal Calibrate level.

(b) Release the GND pushbutton. The CAL pushbutton should still be depressed (preceding step).

(c) With the FUNCTION switch set to "A", the panel meter should indicate full scale.

(d) Transfer the FUNCTION switch setting to "B". The panel meter should continue to indicate full scale.

(e) Transfer the FUNCTION switch setting to "A – B". The meter indication should go to "0", plus or minus a percent or two of full scale (depends on how well the zero and calibrate operations were performed when the modules were checked out individually).

This completes the Initial Checks. If the indicated results were observed, one can reasonably conclude that the M162 and the Processor Modules with whch it was furnished are working properly. Note that no dual-channel checks were furnished for the case where dual-channel operation is attempted with one M163 Processor Module and one M164 Processor Module. Operation with this combination is perfectly feasible and there should be little difficulty in adapting the preceding procedures to checking out dual-channel operation with one module of each type.

SECTION IV
OPERATING INSTRUCTIONS

4.1 INTRODUCTION

This section of the manual begins with a discussion of several preliminary operating considerations, such as installation, cooling, warmup, and power requirements. These discussions are followed by a description, keyed to photographs, of the controls and connectors. The remainder, the largest part of Section IV, consists of the detailed operating instructions, which discuss in detail how to use the Model 162 and its associated processor modules to obtain the best measurement results possible.

4.2 PRELIMINARY CONSIDERATIONS

4.2A INSTALLATION

The Model 162 Mainframe can be either bench or rack mounted. The rack-mounting angles, which are supplied as part of an optional accessory kit, are easily bolted to the side of the instrument immediately behind the front panel. To mount the angles, it is first necessary to remove the decorative cover strips which are secured by the same bolts as are used to mount the angles.

4.2B POWER REQUIREMENTS

When equipped with two processor modules and with typical loading, the Model 162 requires a maximum of 50 VA of either 105-125 V ac or 210-250 V ac, 50-60 Hz. A rear-panel switch enables transfer from one line voltage range to the other. The processor modules take their power from the mainframe.

4.2C FUSING

There are three fuses in all, a rear-panel slow-blow type fuse (1.0 A for 117 V operation, 0.5 A for 220 V operation) in series with the ac input power, and two internal ¼ A slow-blow type fuses that protect the ±50 V regulators. These regulators supply power to the Tektronix Sampling Head when the mainframe is operated in conjunction with a Model 163 Processor Module.

4.2D GROUNDING

The chassis of the Model 162 is internally connected to the "third wire" or grounding pin of the input power connector. It is important that this grounding pin be connected to a good earth-ground connection, either through the power distribution system of the laboratory, or at least by running a separate ground wire to a cold water pipe, which in turn has a good ground connection. This precaution serves to prevent shock hazards and to prevent the entire chassis from being driven at some high ac voltage.

Should it be necessary to electrically isolate the input power to the instrument, use a good quality, electrostatically-shielded, isolation transformer. the chassis of the instrument should still maintain its earth-ground integrity by running a heavy wire (#18 AWG or larger) from the chassis to input neutral or to an earth-ground connection.

4.2E COOLING

No special cooling techniques are required. However, if the instrument is operated in an enclosed rack with other equipment, the ambient temperature within the rack should not exceed 40°C.

4.3 CONTROLS, CONNECTORS, AND INDICATOR LAMPS

4.3A MAINFRAME FRONT PANEL (Figure IV-1)

NOTE: Inasmuch as the APERTURE DURATION control affects the M164 only, that control is described in Subsection 4.3C, which treats the M164 Module.

A. **Trigger Mode**—Four pushbuttons select instrument triggering mode.

(1) EXTERNAL—With this pushbutton depressed, instrument is trigger-sensitive to external signal applied to Trigger Input connector. This is the most frequently used trigger mode in measurement applications.

(2) INTERNAL—With this pushbutton depressed, instrument is automatically self-triggering. Trigger rate is approximately the inverse of the selected Aperture Delay Range (plus retrace time). Useful mainly for servicing.

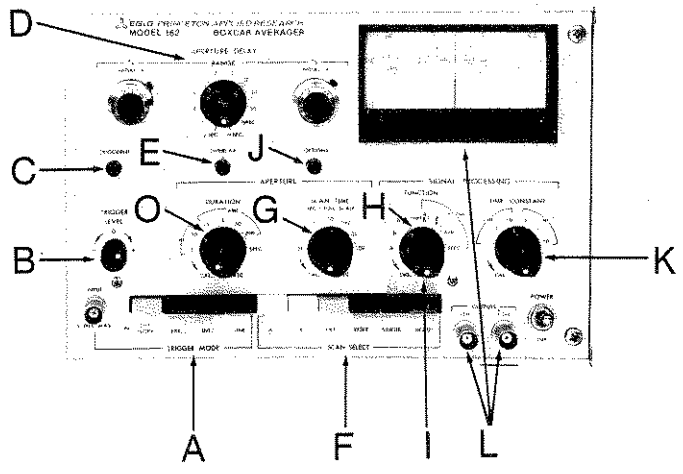


Figure IV-1. MAINFRAME FRONT PANEL

(3) LINE—With this pushbutton depressed, trigger signal is derived from power frequency signal. This trigger mode is used mainly in servicing.

(4) SLOPE—This pushbutton allows the operator the option of triggering on either the positive (pushbutton out) or negative (pushbutton depressed) slope of the applied trigger waveform in EXT and LINE TRIGGER operation.

B. **Trigger Level**—This control determines where on the applied trigger waveform triggering will take place. Range of control is ±15 V.

C. **Triggered Lamp**—This lamp flashes each time the Model 162 is triggered. The duration of the flash is long enough to be noticed independent of the selected operating parameters.

D. **Aperture Delay Range**—Dual-concentric switch and two associated ten-turn dials determine the Aperture Delay characteristics.

(1) RANGE—This switch determines the interval (beginning marked by trigger) over which the leading edge of the aperture opening can be positioned. In Internal Trigger operation, this switch also sets the trigger repetition rate, which is approximately the reciprocal of the selected Delay Range plus the retrace time.

(2) % INITIAL A and % INITIAL B—Function depends on whether aperture is to be manually positioned or scanned. If the aperture is to be manually positioned, these dials directly set the position of the aperture leading edge as a % of the selected Delay Range. As indicated, one dial affects the A Processor Module, the other the B Processor Module. In scanned operation, the interval over which the leading edge of the aperture will be scanned begins with the % Initial A & B Delay dial settings and finishes with the end of the selected Aperture Delay Range.

E. **Overlap Lamp**—This lamp lights whenever the trailing edge of the aperture opening extends beyond the end of the selected Aperture Delay Range. Overlap circuit not active for M163 Processor Module.

F. **Scan Select**—Six pushbutton switches control the aperture scan characteristics.

(1) A & B—These pushbuttons allow the operator to select manual or scanned positioning of the aperture for each Processor Module. In the released position, the position of the aperture leading edge at the corresponding Processor Module is directly set by the % Initial Delay dial. In the depressed position, the aperture is scanned over the interval beginning with the % Initial Delay dial setting and ending at 100% of the selected Aperture Delay Range. **NOTE 1:** The RESET, SINGLE, and HOLD pushbuttons are relevant to scanned operation only. **NOTE 2:** If EXT. Scan pushbutton is depressed, A and B pushbuttons select channel(s) to be affected by external program (% Initial Delay dials always effective).

(2) EXT—With this pushbutton depressed, the aperture position is determined by the sum of the % Initial Delay dial setting plus any delay programmed by externally derived voltage applied to rear-panel SCAN IN/OUT connector. Note that with no program applied to rear-panel connector, % Initial Delay dials set aperture position. A & B pushbuttons determine which channel(s) will be affected by applied program.

(3) SINGLE—Affects scanned operation only. When depressed, aperture position remains at 100% of selected Aperture Delay Range when a given scan ends. When released, aperture position automatically resets to delay determined by % Initial Delay dial setting to mark beginning of new scan. Scans follow one another with no operator action required. **NOTE:** If A and B are both depressed, one aperture will generally reach 100% of Aperture Delay Range before the other. Whichever reaches 100% of Delay Range first dominates, that is, as soon as one aperture or the other reaches 100%, both apertures will reset or both will scan no further according to position of SINGLE pushbutton.

(4) HOLD—When depressed, aperture position scan stops advancing. When button is released, scan continues from hold point.

(5) RESET—Depressing this momentary action switch causes the scan to reset immediately to the delay set by the % Aperture Delay dials. **NOTE:** Hold pushbutton overrides reset.

G. **Scan Time**—Dual-concentric controls determine time required to scan leading edge of Aperture opening over the entire Aperture Delay Range.

H. **Function**—Switch provides choice of seven functions (three standard and four optional). A given instrument can only be equipped with two optional signal-processing functions at a time. This limit of two does not apply to the digital storage option.

(1) STANDARD FUNCTIONS
A: Channel A output only.
B: Channel B output only.
A – B: Channel A output minus Channel B output.

(2) OPTIONAL FUNCTIONS—Circuitry is contained on plug-in printed circuit cards for which two connectors have been provided inside the Model 162.

A/B: Channel A output divided by Channel B output (see specs. for transfer function).

A × B: Channel A output multiplied by Channel B output (see specs. for transfer function).

LOG A/B: Logarithm of Channel A output divided by Channel B output (see specs. for transfer function).

SPEC: User-designed and constructed function. Blank circuit cards can be purchased from EG&G Princeton Applied Research Corporation.

I. **Digital Storage Option**—Front-panel switch activates Digital Storage Option circuitry. Digital Storage Option allows operation at very low duty factors (see specs.).

J. **Options Lamp**—This lamp lights if the Function switch is set to a position for which a proper plug-in circuit card has NOT been installed. Also lights if Digital Storage is turned on without a Digital Storage card having been installed.

K. **Time Constant**—Output smoothing filter time constant in decade steps from .1 ms to 10 s. Continuously variable × 10 multiplier extends range to 100 s.

L. **Outputs**
(1) ANALOG PANEL METER—Taut-band, center zero standard.

(2) DIGITAL PANEL METER—3½ digit display with BCD output is available as extra cost option.

(3) ANALOG OUTPUT— ± 10 V corresponding to full-scale output.

(4) ANALOG DERIVATIVE— ± 10 V scan-time derivative of averaged output.

4.3B MODEL 163 PROCESSOR MODULE (Figure IV-2)

V. **Input**—Utilize standard plug-in sampling head to achieve aperture widths as narrow as 100 ps. Can be operated remotely with optional Sampling Head Extender.

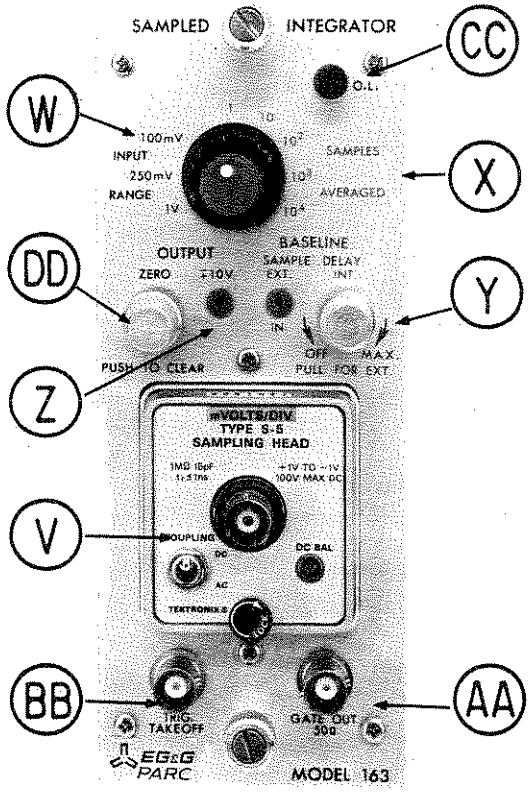


Figure IV-2. MODEL 163 PROCESSOR MODULE

W. **Input Sensitivity**—Switch-selectable choice of 100 mV, 250 mV, or 1 V full scale.

X. **Samples Averaged**—Switch allows selection of number of samples of which output is the average (assuming number of samples taken is very much larger than SAMPLES AVERAGED selected). Sampling does not "stop" after number of samples selected have occurred.

Y. **Baseline Sampling**—When activated, alternate sampling apertures are time positioned as determined by associated Baseline Sampling Delay control or by external signal applied to adjacent pin jack. Model 163 output is the difference between averaged segment of input signal and averaged segment of baseline, thereby providing automatic compensation for dc drifts and baseline wander.

Z. **Output Monitor**—Processor Module output is provided at this pin jack. Adjacent control permits processor-module output dc level to be adjusted.

AA. **Aperture Monitor**—0.5 μs marker pulse. Leading edge of marker pulse occurs about 10 ns after leading edge of aperture opening. Note

that aperture duration is determined by choice of Sampling Head and is otherwise invariable.

BB. Trigger Takeoff—Risetime-limited replica of input signal provided at this connector. Baseline is nominally + 2.5 V ± 1.5 V. Amplitude is twice input amplitude. This signal is provided with type S1, S2, S4, and S5 Sampling Heads only.

CC. Overload Lamp—Lights to indicate overload condition in M163.

DD. Clear—Pressing this pushbutton sets all instrument integrators to zero, including those in the Model 164. If the instrument is equipped with the digital storage option, the digital storage memory contents will be erased as well. **NOTE:** The Model 164 Processor Module is also equipped with a Clear pushbutton that performs exactly the same function.

4.3C MODEL 164 PROCESSOR MODULE (Figure IV-3)

M. Input Controls—Three pushbutton switches provide a choice of high or low input impedance and ac or dc coupling. Also provided is a means of internally grounding the input to facilitate zeroing.

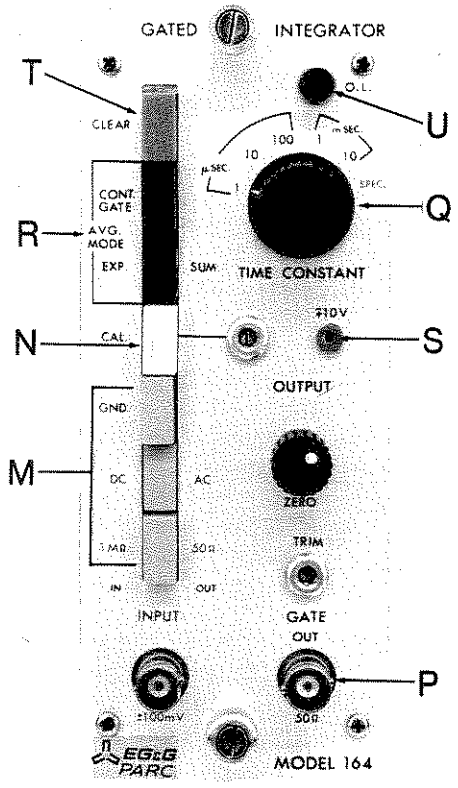


Figure IV-3. MODEL 164 PROCESSOR MODULE

N. Calibrate—When depressed, this pushbutton causes an internally derived 100 mV signal to be applied to the input. Adjacent gain-trim control permits output to be adjusted to full scale with calibrated input. Trim control can be used to match the gain of one M164 to the gain of another in dual-channel operation.

O. Aperture Duration—Dual-concentric controls located at the MAINFRAME determine the M164 Aperture width. Aperture can be set at any width over the range of 10 ns to 5 ms plus "special" user installed range. Aperture Duration controls have no effect on M163 Processor Module.

P. Gate Out—Pulse coincident with aperture provided at this connector. Tracks accurately down to 50 ns aperture durations when terminated in 50 Ω. Adjacent Trim control permits aperture duration to be trimmed, useful in matching the aperture characteristics of two Model 164's. Selected Aperture Duration is obtained with Trim set to center of range.

Q. Time Constant—Enables averaging time constants from 1 μSEC to 10 mSEC to be selected (plus "SPECIAL" user-installed range).

R. Averaging Mode—Two pushbuttons.

(1) EXP/SUM—Gives choice of exponential or summation (linear) averaging.

(2) CONT. GATE—When this pushbutton is depressed, unit is locked into continuous-aperture state. Useful mainly for servicing.

S. Output Monitor—Processor Module output is available at this pin jack. Adjacent Zero control permits processor-module output dc level to be adjusted.

T. Clear—Pressing this pushbutton sets all instrument integrators to zero, including those in the Model 163. If the instrument is equipped with the digital storage option, the storage-option memory contents will be erased as well. **NOTE:** The Model 163 Processor Module is also equipped with a CLEAR pushbutton that performs exactly the same function.

U. Overload Indicator Lamp—This indicator glows when the Model 164 amplifiers are overdriven.

4.3D REAR PANEL

BNC CONNECTORS

(1) SCAN IN/OUT: Function depends on setting of front-panel Scan Select EXT. pushbutton. If this pushbutton is depressed, aperture position is determined by % Initial Delay dial plus voltage program applied to this connector. Sensitivity is 10% of selected Aperture Delay Range per +1 V applied. A and B pushbuttons determine which channel(s) are affected by externally derived program. $Z_{IN} = 10$ kΩ. If pushbutton is in released position, positive Scan Ramp is provided at this connector. Ramp is referenced to 0 V. Peak amplitude is proportional to setting of % Initial Delay dial with a maximum of +5 V. $Z_{OUT} = 600$ Ω.

(2) CHANNEL A SCAN: When Channel A is being scanned, sum of scan ramp and % Initial Delay A voltage is provided at this connector. Ramp is referenced to dialed % Initial Delay voltage (maximum of +5 V at 100%). When ramp plus dialed delay voltage reach +5 V, ramp either maintains five volt level (Single pushbutton depressed) or resets to start another ramp (Single pushbutton released). $Z_{OUT} = 1$ kΩ. **NOTE:** In EXT. Scan operation, output is sum of EXTERNAL PROGRAM plus % of Initial Delay A voltage (A pushbutton depressed).

(3) CHANNEL B SCAN: Same as for Channel A, except that % Initial Delay B dial sets reference voltage.

NOTE: If both A and B are being scanned, reset (or end-of-scan hold) occurs for both when either aperture opening reaches 100% of delay range position, corresponding to +5 V level being reached at either of the Channel Scan BNC connectors.

BCD AND SIGNAL/CONTROL INTERFACES (Tables IV-1 and IV-2)

The DVM used in the Model 162 has a four-digit display. Each digit is represented at the rear panel connector in Binary Coded Decimal (BCD) format. The most significant digit is the leftmost of the four digits displayed. The Teletype digit #1 (? for overload) is 1 digit to the left of the Most Significant Digit. The notation A, B, C, and D after the digit notation refers to column headings of the truth table. The value of each of these outputs when a logic 1 is 1, 2, 4 and 8 respectively. For each digit, the A, B, C, and D outputs, taken together, represent a number (0 to 9) in BCD format.

4.4 DETAILED OPERATING CONSIDERATIONS, INTRODUCTION

In most applications, the Model 162 is used to determine the exact shape of a repetitive waveform that is obscured by noise. By sliding an aperture over the interval of interest and averaging the signal that passes through the window, the waveform can be reproduced at the output. In general, the recovery of any given input waveform is accomplished as follows.

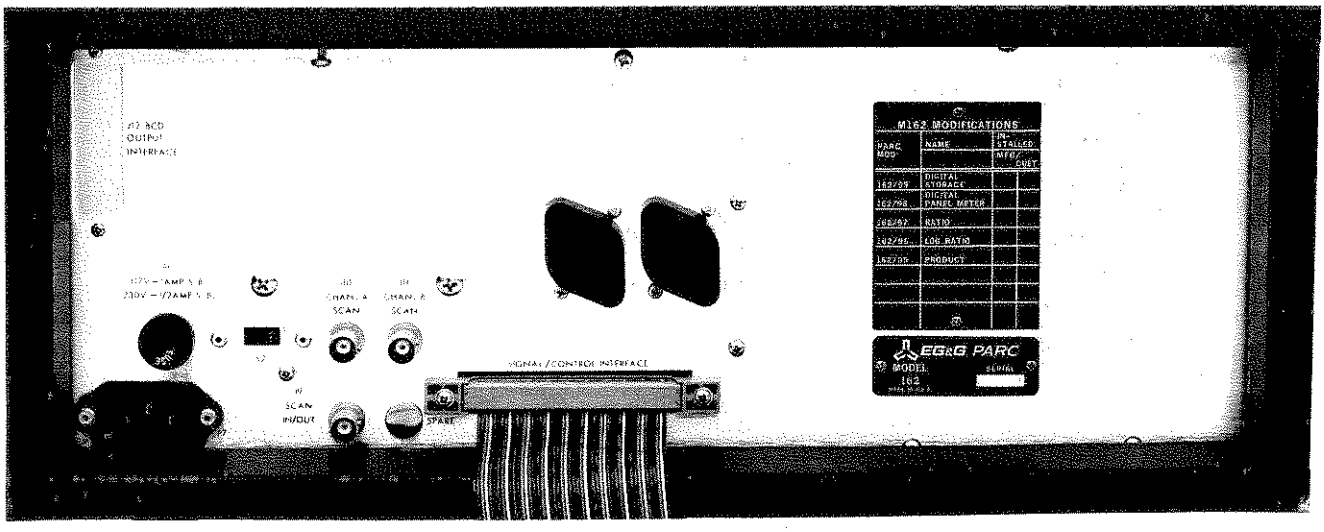


Figure IV-4. MODEL 162 REAR PANEL

Pin numbering used on cable assembles 6020-0131 & 0132	Pin numbering used on ribbon-cable assemblies	Function or Signal
1A, 25B	1, 50	– E OUT (B): ∓10 V f.s. Channel B Module Out.
1B, 25A	2, 49	– E OUT (A): ∓10 V f.s. Channel A Module Out.
2A, 24B	3, 48	F (E OUT): Mainframe analog derivative output
2B, 24A	4, 47	F (E OUT): Mainframe analog output.
3A, 23B	5, 46	SCAN IO/OUT: Same as for SCAN IN/OUT BNC connector.
3B, 23A	6, 45	SCAN SUPPRESS: Externally derived voltage applied to this point can be used to vary scan rate plus or minus relative to that selected by the Scan Time controls.
4A, 22B	7, 44	CHANNEL B SCAN: Same as for CHANNEL B SCAN BNC connector except that $Z_{OUT} \cong 0\ \Omega$.
4B, 22A	8, 43	CHANNEL A SCAN: Same as for CHANNEL A SCAN BNC connector except that $Z_{OUT} \cong 0\ \Omega$.
5A, 21B	9, 42	$\overline{\text{SCAN RESET}}$: Logic 0 applied to this input parallels function of front-panel SCAN RESET pushbutton.
5B, 21A	10, 41	$\overline{\text{SIGNAL RESET}}$: Logic 0 applied to this input parallels function of front-panel CLEAR pushbutton (provided on both Models 163 and 164).
6A, 20B	11, 40	$\overline{\text{SCAN HOLD}}$: Logic 0 applied to this input parallels function of front-panel HOLD pushbutton.
6B, 20A	12, 39	TRIGGER HOLDOFF: Logic 1 applied to this input inhibits instrument from being triggered. Source must provide 500 μA.
7A, 19B	13, 38	$\overline{\text{SCOPE BLANKING}}$: This output is at logic 0 when a scan is in progress. It is at +50 V (10 kΩ source) when scan is NOT in progress.
7B, 19A	14, 37	SCOPE BLANKING: This output is at +50 V (10 kΩ source) when scan is in progress. It is at logic 0 when scan is NOT in progress.
8A, 18B	15, 36	spare
8B, 18A	16, 35	PENLIFT (NO): Normally open 1 A contact of pen-lift relay.
9A, 17B	17, 34	+15 V ±15 mV; 100 mA capacity.
9B, 17A	18, 33	PENLIFT (W): Wiper of pen-lift relay (rated at 1 A).
10A, 16B	19, 32	–15 V ±15 mV; 100 mA capacity.
10B, 16A	20, 31	PENLIFT (NC): Normally closed 1 A contact of pen-lift relay.
11A, 15B	21, 30	+5 V ±50 mV; 300 mA capacity.
11B, 15A	22, 29	spare
12A, 14B	23, 28	GND (ground return).
12B, 14A	24, 27	GND (ground return).
13A, 13B	25, 26	HIGH QUALITY (SIGNAL) GROUND

NOTE: Mating connector (3M#3415) with short length of ribbon cable is supplied.

Table IV-1. P101 INTERFACE (REAR PANEL)

(1) The Model 162 is synchronized with the signal of interest. This is usually done by applying an externally derived trigger signal to the Trigger Input connector of the Model 162.

(2) The signal is applied to either the Model 163 or the Model 164, and the module controls are adjusted for optimum processing of the signal.

(3) The Aperture Delay and Scan controls are adjusted as required.

(4) The proper function is selected and the actual signal recovery performed.

In the following pages, each of these steps is discussed in detail.

4.5 SYNCHRONIZATION

4.5A INTRODUCTION

Figure IV-5 illustrates the basic timing relationships in the Model 162 Boxcar Integrator. Each time the unit is triggered (triggering on the positive edge of an externally derived trigger is indicated in the figure), there occurs a fixed Trigger Delay of nominally 30 ns, at the end of which the selected Aperture Delay Range begins. (For convenience in illustration, the Aperture Delay Range is shown as a pedestal, although from an operating point of view, it is simply a selected time interval.) At some time after the beginning of the Aperture Delay Range interval, but before it ends, an aperture opening occurs. The duration of the aperture opening can extend beyond the end of the Aperture Delay Range, but normally does not. Usually, the aperture opening is very short relative to the selected Delay Range. In single-point analysis, the aperture opens at the same

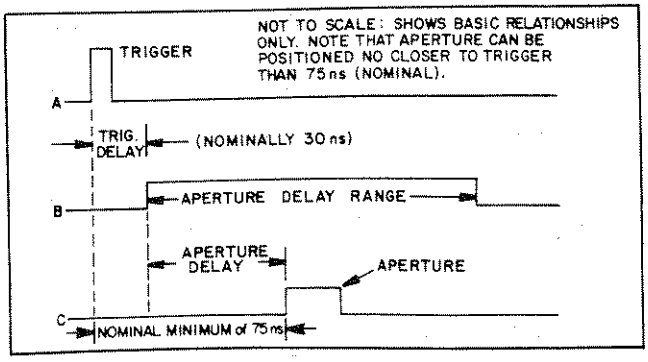


Figure IV-5. BASIC MODEL 162 TIMING RELATIONSHIPS

Pin	Function	Function when applied to 131 System M262
1	Polarity (logic 1 = 1)	1 = Polarity +
2	+ 4 V	Not Used
3	Overload Output (Logic 1 = Overload)	Digit 1, A
4	Overload Output (Logic 1 = Overload)	Digit 1, C
5	DVM Most Significant Digit, A	Digit 2, A
6	DVM Most Sig. Digit, C (always ground)	Digit 2, C
7	DVM 1nd Most Significant Digit, A	Digit 3, A
8	DVM 2nd Most Significant Digit, C	Digit 3, C
9	DVM 3rd Most Significant Digit, A	Digit 4, A
10	DVM 3rd Most Significant Digit, C	Digit 4, C
11	DVM Least Significant Digit, A	Digit 5, A
12	DVM Least Significant Digit, C	Digit 5, C
13	Spare	
14	Spare	
15	Spare	
16	Spare	
17	DVM Least Significant Digit, D	Digit 5, D
18	Conversion Complete (inverted)	EXECUTE
19	Conversion Complete	Not Used
20	External Trigger Input	TTL logic 1 that goes to logic 0 for at least 1.5 μs (max. 2 ms). Unit resets on neg. slope, triggers on pos. slope.*
21	Spare	
22	Spare	
23	NOT BUSY input (Output data will remain fixed when this line is at logic 0. Must be 1 or open for conversions to continue)	BUSY
24	Exponent, A (always ground)	Digit 6, A
25	Exponent, C (always ground)	Digit 6, C
26	Exponent, B (always ground)	Digit 6, B
27	Exponent, D (always ground)	Digit 6, D
28	DVM Overload Output (Logic 1 = Overload)	Digit 1, B
29	DVM Overload Output (Logic 1 = Overload)	Digit 1, D
30	DVM Most Sig. Digit, B (always ground)	Digit 2, B
31	DVM Most Sig. Digit, D (always ground)	Digit 2, D
32	DVM 2nd Most Significant Digit, B	Digit 3, B
33	DVM 2nd Most Significant Digit, D	Digit 3, D
34	DVM 3rd Most Significant Digit, B	Digit 4, B
35	DVM 3rd Most Significant Digit, D	Digit 4, D
36	DVM Least Significant Digit, B	Digit 5, B

NOTES: Logic 1 = + 3.5 V ± 1 V, Logic 0 = 0.2 V ± 0.2 V. Mating connector is Amphenol Blue Ribbon #57-30360.

*For external triggering of digital display, there must first be a 5 kΩ resistor (nominal value) connected betrween pins R and 15 of J2 (upper connector at rear of panel meter) to inhibit internal triggering.

Table IV-2. DIGITAL OUTPUT CONNECTOR

time after each trigger. In scanned operation, with each repetition it opens a bit later with the incremental increase in Aperture Delay normally being small relative to the duration of the aperture opening itself. Note that in both scanned and single-point analysis, internal fixed-delays act to prevent positioning the aperture any closer to the trigger than 75 ns (nominal).

A gated integrator is made to "see" the input signal for the duration of each aperture opening. If the same point is sampled for many repetitions, the integrator output gradually assumes the average level of the input signal at the sampled point. In scanned operation, if the scan is slow enough, each point will be sampled enough times to be "captured" by the integrator, so that, if the integrator output is used to drive the "Y" axis input of a recording device, the input waveform will be reproduced at the scan rate.

In any case, whether doing single-point or scanned analysis, it is absolutely essential that the timing of the aperture opening be known and controlled relative to the timing of the input signal. In short, the signal and the Model 162 timing sequence must be synchronized. This is normally done by operating the Model 162 in the External Trigger mode and applying a trigger signal having a fixed time relationship to the waveform being examined. Frequently it may be possible to trigger the Model 162 from the same stimulus as initiates the signal to be processed. Operation of the Model 162 in each of the Trigger modes is discussed in the following paragraphs.

4.5B EXTERNAL TRIGGER MODE

As long as the EXT Trigger Mode pushbutton is depressed, a timing sequence is initiated each time an approriate externally derived trigger signal is applied to the Trigger INPUT connector. The

SLOPE pushbutton and TRIGGER LEVEL control determine when, in terms of the fine structure of the trigger pulse, the Aperture Delay Range begins. However, regardless of how these controls define the trigger detection point, there is always a minimum delay of nominally 30 ns between the trigger detection point and the beginning of the subsequent Aperture Delay Range. Other internal delays add to this, with the result that the aperture can follow the trigger by no less than 75 ns (nominal). Thus, when operating with a short Delay Range, it may prove advantageous to pre-trigger the M162 or to delay the signal to be recovered by means of an appropriate delay line. The Trigger Level control allows triggering over a range of ± 15 V and the Slope pushbutton allows triggering on either the positive-going or negative-going edge of the applied trigger. For reliable operation the applied triggers should be at least 0.5 V in amplitude and have a duration of no less than 10 ns. Trigger pulses larger than 100 V (zero-to-peak) should not be applied because such pulses may damage the trigger detection circuitry. $Z_{IN} = 50\ k\Omega$.

Figure IV-6 shows the variation in trigger detection point for two arbitrarily determined trigger levels and for both slopes. The main criterion in setting these controls is to select a point which gives a stable trigger point for each input trigger pulse.

Proper triggering is indicated by the front-panel TRIGGERED indicator lamp. Each time the unit is triggered, this lamp glows briefly. The duration of the glow is independent of instrument operating parameters. As a result, even with a very short trigger pulse and Aperture Delay Range, the glow lasts long enough to be noticed. With relatively low trigger rates, the individual triggers are clearly distinguishable by separate flashes of light. With fast trigger rates, the light will appear to be intensity modulated. This is normal and does not indicate improper triggering.

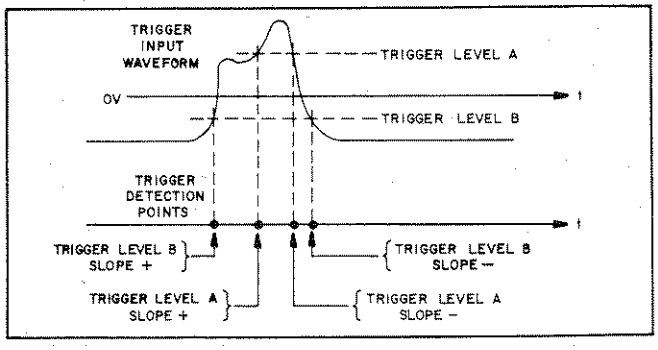


Figure IV-6. TRIGGERING AS A FUNCTION OF SLOPE AND TRIGGER LEVEL

While a timing sequence is in progress, the instrument remains trigger insensitive. The trigger insensitive state extends somewhat beyond the selected Aperture Delay Range to allow the involved circuits time to reset. Trigger inhibiting also occurs for the duration of an aperture opening that extends beyond the end of the Aperture Delay Range. In the case of a Model 163 Processor Module, the maximum trigger rate is limited to 10 kHz.

Trigger inhibiting is provided because it is frequently neither necessary nor desirable that every trigger pulse initiate a timing sequence. Consider the case where the experiment is triggered by an oscillator, with the oscillation period shorter than the duration of the waveform being investigated.

In such a case, it would be awkward (to say the least) to start a new timing sequence while another is still in progress.

Internal to the instrument, there is an Aperture Delay Range ramp which is on the order of five to ten percent longer in duration than the selected Aperture Delay Range. This five to ten percent overhang has to be considered in addition to the reset time. For Aperture Delay Ranges from 100 ns to 50 μs, the reset time is 100 ns. For Aperture Delay Ranges from 100 μs to 50 ms, the reset time is 100 μs. Thus, depending on the choice of Aperture Delay Range, the reset time may be either short or long relative to the Delay Range overhang. In any case, there is trigger inhibiting beyond the end of the Aperture Delay Range equal to the sum of the reset plus overhang.

To illustrate the effects of trigger inhibiting in an experimental application, consider the following example. Suppose one were operating with an Aperture Delay Range of 20 μs and a trigger repetition period of 23 μs. Further suppose the Aperture Duration to be 5 μs and that the aperture position is to be scanned over the Aperture Delay Range. Early in the scan, the aperture opening terminates well before the end of the Aperture Delay Range, so there is no trigger inhibiting as a consequence of aperture opening overlap. With a reset time of 100 ns and a Delay Range overhang of nominally 2 μs, these those factors can also be neglected as far as trigger holdoff considerations are concerned. Thus, assuming the system does not include a Model 163 (maximum trigger rate of 10 kHz), the information early in the scan will be one sample per 23 μs. At the end of the scan, however, the situation changes. Before the aperture delay reaches 100%, it will extend far enough beyond the end of the Aperture Delay Range to overlap the next trigger. Because the instrument is rendered trigger insensitive whenever the aperture extends beyond the Aperture Delay Range (indicated by glowing of the front-panel OVERLAP indicator lamp), the trigger falling in the Overlap interval is ignored and

the information rate at the end of the scan decreases to one sample per 46 μs. If the scan rate had been selected according to the higher information rate, the resolved output waveform would be "blurred" towards the end of the scan. The simplest solution would be to increase the trigger period to about 30 μs. In that way, the controls could be idealized to an information rate that would remain constant over the scan time.

4.5C LINE TRIGGER MODE

Line Trigger operation is actually a variation of External Trigger mode operation. A signal derived from the ac power line is applied to the same point internally as is the regular external trigger signal. The Slope pushbutton and Trigger Level controls remain effective; operation is the same as if one were operating in the External Trigger mode, and using a 1.2 V pk-pk square wave input at the line frequency as the trigger signal. Line trigger operation is mainly used in servicing the Model 162. However, there is no reason why it could not be used in experimental applications where the event under study is synchronized with the line. Generally speaking, it is better to operate asynchronous with the line to reduce the possibility of bothersome pickup and interference at the line frequency and its harmonics.

4.5D INTERNAL TRIGGER MODE

With the INT Trigger pushbutton depressed, the Model 162 becomes self-triggering and free runs. The interval between successive aperture openings equals (at least) the Aperture Delay Range, plus the Delay Range overhang (nominally 5% to 10% of the selected Aperture Delay Range), plus the reset time (100 ns or 100 μs as explained in the preceding discussion of trigger inhibiting with External Trigger operation). If the system includes a Model 163 Processor Module, the 10 kHz trigger rate limit still applies. In other words, assuming the system includes a Model 163, the interval between successive apertures will be at least 100 μs, no matter how short the Aperture Delay Range.

Internal trigger mode operation is intended for servicing use. Unless one is willing to go to a great deal of trouble, there is no way of synchronizing the Model 162 with the experiment. Almost always, it will prove more convenient to trigger both the experiment and the Model 162 from an external trigger source. **NOTE:** When the INT. pushbutton is depressed, triggering may not begin. If this happens, the remedy is simply to alternately release and depress the INT. pushbutton until proper triggering is established as indicated by the triggered lamp.

4.6 INPUT SIGNAL PROCESSING, GENERAL

The Model 162 can be operated with either one or two Processor Modules. Mixing of the module types is allowed, that is, the "A" module can be either a Model 163 or a Model 164, and the same is true for the "B" module. Because of the considerable difference in operating controls provided on the two modules, they are discussed separately.

4.7 INPUT SIGNAL PROCESSING, MODEL 164

The Model 164 can be operated in either position. Installation consists simply of sliding the Module into one of the two slots, and then securing it by means of the two knurled locking screws provided, one at the top and the other at the bottom of the module panel. The mainframe power should be off when a module is being inserted or removed. A discussion of each of the Model 164 controls follows.

4.7A INPUT IMPEDANCE

This pushbutton selects the input impedance, either 1 MΩ (pushbutton depressed) or 50 Ω (pushbutton released). For operation from source impedances high enough to result in significant attenuation with a 50 Ω input impedance, one should choose the 1 MΩ input impedance. However, bear in mind that as the source impedance becomes higher, the high-frequency attenuation introduced by the Model 164 input shunt capacitance will increase as well. This input shunt capacitance is typically 25 pF. It may happen, such as when one wishes to use certain external attenuator probes (EG&G PARC #1150-2400-08S), that a higher shunt capacitance will be desirable so that the overall attenuator response (probe resistance shunted by compensation adjustment in series with Model 164 input resistance shunted by its input capacitance) will be within range of the compensation adjustment. Unused pads have been provided on the Model 164 circuit board to facilitate adding this capacitance. The M164 Parts Location Diagram (Section VII) indicates exactly where the capacitor should be installed.

In those applications calling for the highest possible resolution, and where the source impedance is fifty ohms, use of the 50 Ω input is mandatory. Also, 50 Ω cables must be used to interconnect the signal source and the Model 164. Suitable cable types include RG58C/U, RG188A/U, and many others. In many situations, the source impedance may be other than 50 Ω (93 Ω, 110 Ω, etc.). Where this is the case, the cable characteristic impedance should be that of the source and a series resistor should be provided at the input of the Model 164 to achieve impedance matching. The resistance of the series resistor is determined by:

$$R_{SERIES} = Z_{SOURCE} - 50\ \Omega$$

4.7B INPUT COUPLING

This pushbutton allows the operator to choose either DC coupling (pushbutton depressed) or AC

coupling (pushbutton released). DC coupling is preferred when measuring low-frequency phenomena. Where dc drift at the signal source is a consideration, especially over long analysis intervals, ac coupling might be preferred.

The use of ac coupling prevents input dc offsets from being included in the analysis. However, low frequency components which may be of interest are lost. The input network used gives a 3 dB down low frequency response of 0.16 Hz. Below this frequency the response goes down at the rate of 6 dB/octave. Note that the internal connections differ according to the choice of input impedance. As shown in Figure IV-7, dc components are blocked altogether with the 1 MΩ input impedance. With the 50 Ω input impedance, the dc components are blocked with respect to the input amplifier, but they are applied to the 50 Ω input resistor. Consequently, when operated with the 50 Ω input impedance, whether ac or dc coupled, the applied dc should be limited to 5 V (equivalent to half a watt dissipation in the 50 Ω input resistance).

4.7C GND PUSHBUTTON

This pushbutton, when depressed, grounds the input of the first amplifier, useful when zeroing. Note that the Input connector is NOT grounded. If the 1 MΩ input impedance is selected, an applied input signal simply sees an open circuit. If the 50 Ω input impedance is selected, an applied input signal sees 50 Ω to ground, regardless of whether one is operating ac coupled or dc coupled.

4.7D CAL. PUSHBUTTON

When this pushbutton is depressed, the input signal is disconnected from the input amplifier and an internally derived 0.25% accurate full-scale dc level is applied in its place. An associated screwdriver adjustment allows the gain of the instrument to be precisely set by monitoring for −10 V at the front-panel Output Monitor pin jack (instrument must be triggered). The total range of the adjustment is about 20% of full scale. Note that, for the gain to be accurately set, the module must first be zeroed (GND pushbutton depressed).

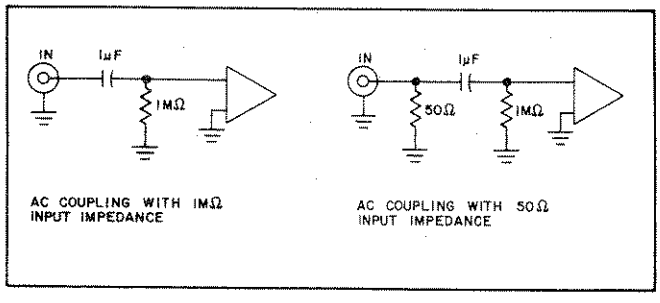


Figure IV-7. INTERNAL COUPLING CONNECTIONS AS A FUNCTION OF SELECTED INPUT IMPEDANCE IN AC COUPLED OPERATION

4.7E ZERO CONTROL

This multi-turn, high-resolution control allows the module output to be precisely adjusted to 0 V with zero applied to the input (GND pushbutton). The total range of the control is nominally 100 mV relative to the input of the Model 164. **NOTE:** To obtain a valid zero adjustment, the unit must be triggering. Also, for best results, the Aperture Duration should be set to the signal recovery value. In particular, one should NOT do a zero adjustment with the CONT. GATE pushbutton depressed unless CONT. GATE operation is intended. A suitable zero-adjustment procedure follows.

(1) Establish proper triggering from an external source. If preparing to examine an externally derived signal, the aperture duration should be set to the intended signal-recovery value.

(2) Depress the GND pushbutton.

(3) Monitor the level at the Model 164 front-panel pin jack or at the mainframe output (Output connector or panel meter). Then adjust the Zero control for 0 V at the monitored point. Note that the observed rate of response will depend on the selected Model 164 Time Constant and on the duty factor (observed time constant equals selected time constant divided by aperture duty factor). With a narrow aperture and low repetition rate, the response time can become very long. The effect of the mainframe "Signal Processing" Time Constant is independent of duty factor.

NOTE: A zero adjustment (GND depressed) is usually followed by a gain adjustment (CAL depressed).

There may also be instances when one would wish to deliberately introduce offset with the Zero control, such as when a non-zero baseline could give a more convenient display. When operating dc coupled, the Zero control can be used to null out dc offsets accompanying the input signal.

4.7F EXP/SUM PUSHBUTTON

This pushbutton allows the operator to select either exponential (weighted) or true (linear or summation) averaging. When operated in the exponential averaging mode, the output signal asymptotically approaches "G" times the input signal level, where "G" is the gain. The time required for the output to reach its final level is five times the observed time constant (selected Model 164 time constant divided by the aperture duty factor). Once the output reaches "G" times the input signal, there is no further change in the output level, regardless of how many repetitions of the input signal occur. After a large number has occurred, at least enough to give five time constants of analysis time, the output of the Processor Module can be considered to be the average of 2TC/AD

repetitions of the input signal, where TC is the selected Model 164 Time Constant and AD is the selected Aperture Duration, both in seconds. The SNIR (signal-to-noise improvement ratio) achieved in the M164 then is $\sqrt{2TC/AD}$. Note that this is a weighted average, that is, the most recent repetition has more influence on the output level than the one preceding it, which has more influence than the one preceding it, and so forth, on back to the early repetitions which have negligibly small influence. Note also that when noise is mentioend in this manual it is assumed to be "white" (constant spectral power density independent of the frequency), but band-limited from dc to a maximum frequency equivalent to 1/2AD. The advantages of exponential averaging are that the final output level bears a simple fixed relationship to the input signal level, and that any arbitrary amount of SNIR can be obtained by appropriately selecting the Time Constant and Aperture Duration. The mainframe Signal Processing time constant gives additional improvement in the signal-to-noise ratio as explained in Subsection 4.13E.

With the pushbutton in the released position, the instrument becomes a linear averager, that is, one in which all repetitions of the signal contribute equal volt-second pieces of information to the output. As a consequence, the output does not asymptotically approach G times the input, but rather increases by the same amount with each repetition of the input until output overload occurs. In linear averaging operation, the output is simply the average of N repetitions, where N is the actual number that has occurred. The M164 SNIR then is simply $\sqrt{N}$. Note that the SNIR is independent of both the time constant and the aperture duration. These parameters do, however, affect the rate of growth of the output level, that is, the size of the volt-second piece of information contributed with each repetition.

Figure IV-8 shows the M164 output response as a function of time for the two averaging modes. Note that in exponential averaging, the output response is given by the standard RC charging curve. After an analysis time equal to one time

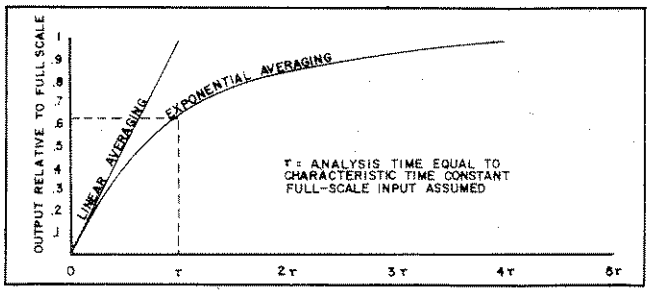


Figure IV-8. OUTPUT RESPONSE AS A FUNCTION OF ANALYSIS TIME FOR BOTH EXPONENTIAL AND SUMMATION AVERAGING

constant, the output reaches 63% of its final value. After five time constants of analysis time, the output is within one percent of its final value. Operated as a linear averager, the output reaches the same level after an analysis interval of only one time constant. This level is not final. If subsequent repetitions occur, the output will continue to rise until overload occurs.

From a practical point of view, the principal difference between linear and exponential averaging is that linear averaging gives a better SNIR for a given number of repetitions of the event under study. However, in most instances, one is not limited with regard to the number of repetitions. By simply extending the experiment somewhat longer, exponential averaging yields results equal to those obtainable with linear averaging and with the advantage that the output level reached bears a simple direct relationship to the input signal level. Consequently, exponential averaging is used in most applications. Nevertheless, situations where the absolute number of allowable repetitions is limited do occur, and in such an application, one would do better to use linear averaging. Consider the following example.

Suppose that the effect under study in a given application deteriorates with repeated stimulation so that the maximum number of useful repetitions is limited to 500. Further suppose that the resolution requirement is 1 μs and that an aperture duration of 1 μs is used. Consider the comparative results of recovering this signal, first with exponential averaging, and second with linear averaging.

For the output to reach its final value in exponential averaging, it is necessary that five time constants of analysis time occur. In the example at hand, there are 500 repetitions, each having a duration of 1 μs, giving a total analysis time of 500 μs. For full output response, the time constant cannot exceed one fifth the analysis time. For maximum SNIR, the time constant wants to be as large as possible. Thus the optimum time constant in this application is 500/5 or 100 μs. The SNIR achieved by the M164 with a time constant of 100 μs and an aperture duration of 1 μs is $\sqrt{2TC/AD} = 14.1$.

Now consider the same example with linear averaging. The M164 SNIR will simply be $\sqrt{N} = \sqrt{500} = 22.4$, regardless of the time constant selected (we assume that resolution requirements dictate the 1 μs aperture duration). The time constant will, however, affect the size of the volt-second increments. Since the analysis time is 500 μs, a time constant of exactly 500 μs will result in full-scale output after 500 repetitions. With a lower time constant, the output level will exceed full scale, resulting in overload. If the time constant is very long, the final level will be very small, perhaps

even so small as to make the drift and noise of the mainframe output amplifiers significant in comparison. Ideally, the time constant selected should give as much output as possible consistent with avoiding output overload. In the case of the Model 164, the proper choice would be 1 ms, the next time constant larger than the ideal (but unavailable) 500 μs time constant.

It should be noted that all of this is with reference to single-point analysis. If the input signal is being scanned, the only possible choice is exponential averaging. Also, note that one must be operating with exponential averaging to perform the earlier mentioned zeroing and gain-calibration operations.

As a final note, it might be mentioned that the combination of summation averaging and continuous gate allows the instrument to be operated as a simple dc integrator.

4.7G CONT. GATE PUSHBUTTON

When this pushbutton is depressed, the instrument is no longer a gated integrator. Instead, the aperture is "locked" open, and the instrument functions as a gain of $\times 100$ amplifier having its upper frequency response set by the Model 164 and Mainframe Time Constant switches. Although there may be laboratory applications for the instrument operated in this manner, this function primarily serves to simplify servicing.

4.7H CLEAR

This pushbutton allows the operator to reset the various instrument integrators to zero. If the unit is equipped with the digital storage option, the data stored in the option memory circuits is wiped out and replaced with all zeros as well. Each processor module is furnished with a Clear pushbutton and all work in parallel. Thus, if the Mainframe in question is equipped with two Model 164's, two Model 163's, or one of each, it doesn't matter which Clear pushbutton is activated. Activating any one of them clears and zero-sets all of the integrators. Usually, clearing is done just prior to starting an analysis. If the analysis has to be terminated prior to its completion, use of the Clear function will shorten the time required to get started again. From an operational point of view, the clearing action is virtually instantaneous and doesn't depend on the instrument's being triggered.

4.7I TIME CONSTANT

The choice of time constant is particularly important with regard to obtaining good measurement results in the minimum possible time. Not only does Time Constant directly affect the SNIR (signal-to-noise improvement ratio), but it also influences the time required to recover a given point or waveform. As explained previously, in exponential averaging, the SNIR achieved in the Processor Module is given by the expression

$$\text{SNIR} = \sqrt{2TC/AD}$$ [white input noise having upper frequency limit of 1/(2AD) Hz assumed]

where the Time Constant and Aperture Duration are given in seconds. By making the time constant large and the aperture duration narrow, any arbitrary amount of SNIR can be achieved. However, there is a tradeoff in that operating time is increased. Each point on the recovered waveform must be analyzed for at least five time constants for that point to be represented at the output with an amplitude of G (G = instrument gain) times the input amplitude. Thus the experimental time required to do an analysis varies directly with the time constant, while the improvement in SNIR varies with the square root of the time constant. Clearly, in an application where minimizing operating time is an important consideration, the time constant should be no longer than is required to reduce the noise to an acceptable level. Additional SNIR can be obtained in the mainframe by means of the Signal Processing Time Constant (see SIGNAL-TO-NOISE and MAINFRAME TIME CONSTANT, Subsection 4.13E).

Besides allowing the choice of time constants from 1 μs to 10 ms, the Time Constant switch also has a special position to allow time constants greater than, or intermediate to, the time constant values provided. With the switch set to SPEC, the time constant is determined by a capacitor mounted on normally unused terminals of the Time Constant switch. (For safety, capacitor to be installed by qualified service technicians only.) Figure IV-9 shows the mounting terminals for the special time constant capacitor. The relationship between capacitance and time constant is:

$$C = \frac{\tau}{2 \times 10^4}$$

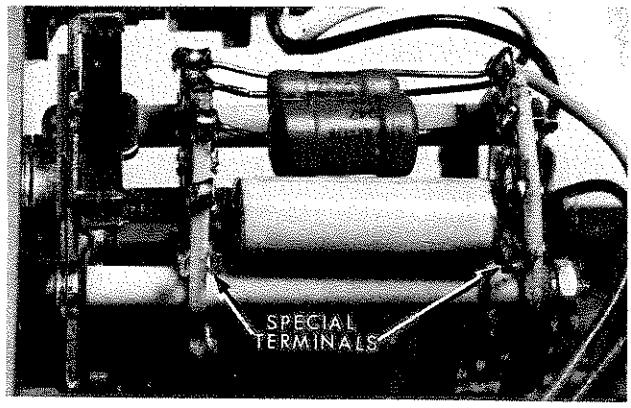


Figure IV-9. TIME CONSTANT SWITCH TERMINALS TO BE USED FOR INSTALLATION OF "SPECIAL" TIME CONSTANT CAPACITOR

where C is the required capacitance in farads, and τ is the desired time constant in seconds.

Only low leakage capacitors should be used. Film capacitors such as Mylar, polystyrene, polycarbonate, and Teflon are all suitable. Specifically to be avoided are electrolytics and tantalum capacitors. The high leakage of such capacitors will severely degrade the hold-time (minimum trigger rate) capabilities of the Model 164 when operated with the Time Constant switch in the SPECIAL position. With no capacitor, the time constant will be nominally 1 μs.

It is important to realize that the observed response time depends on the aperture duty factor as well as on the time constant. Five time constants of analysis time are required to fully "capture" one amplitude point. Because the analysis proceeds only during the aperture open times, the output response is "slowed" by one over the aperture duty factor. For example, suppose one were doing a single point analysis with a one microsecond aperture duration. Further suppose the repetition rate to be 1 kHz and the selected time constant to be 1 ms. Consider the time needed to acquire the point and the SNIR that can be expected. The analysis time must be at least five time constants in duration, or, in this case, five milliseconds. However, because the analysis progresses only when the aperture is open, the real time required to achieve five time constants of analysis time will be longer. With an aperture duration of one microsecond and a repetition rate of 1 kHz, the duty factor (aperture duration divided by aperture period) will be .001, and the time required for 5 ms of analysis time will be 5 s (5 ms ÷ .001). Thus, assuming exponential averaging is used, the point will be acquired in five seconds. The SNIR is given by the selected time constant, not by the observed or slowed time constant. For the example at hand, $SNIR = \sqrt{2 \times 10^{-3}/10^{-6}} = 45$. Realize that the actual SNIR obtained depends on the nature of the noise and interference accompanying the signal. The derivation of the formula for SNIR assumes the input noise has equal energy per unit bandwidth, and that it does not extend beyond 1/(2AD) Hz in frequency. Because actually encountered noise can have altogether different characteristics, the real SNIR obtained may be better or worse than that given by the formula.

4.7J APERTURE DURATION

Like Time Constant, Aperture Duration is particularly important in determining overall instrument performance because it affects both SNIR and the time required to do a specific analysis. In addition, Aperture Duration also directly determines the maximum achievable resolution. Another important performance parameter influenced by the aperture duration is the hold time, that is, the lowest possible repetition rate one can have without information loss due to leakage losses between aperture openings. In the case of the Model 164 Processor Module, the Aperture Duration is set by means of a dual-concentric control located at the Mainframe. This control has no effect whatsoever on the Model 163 Processor Module. The outer knob allows calibrated aperture durations from 10 ns to 500 μs to be selected. The inner knob allows the selected aperture duration to increase by factors ranging from $\times 1$ (calibrated) to $\times 10$, thus allowing intermediate values of Aperture Duration to 5 ms. A screwdriver TRIM adjustment on the front panel of the M164 allows exact matching of Aperture Durations when working with two M164 Processor Modules. The Aperture Duration selected at the mainframe is obtained with the TRIM adjustment set to the center of its range. **NOTE:** Although the panel symbolization indicates a lower limit of 5 ns, typical units will provide AD's down to about 10 ns.

In addition, there is a SPEC. position of the switch in which the aperture duration is determined by a user-installed capacitor to obtain aperture durations longer than those provided. This capacitor is mounted on the Model 164 circuit board (see M164 Parts Location Diagram in Section VII). The expression relating the magnitude of this capacitor and the aperture duration is $C = AD/250$, where C is the capacitance in farads and AD is the desired aperture duration in seconds.

In selecting the aperture time, one must make a compromise between resolution, output noise-to-signal ratio, and the operating time required to do the analysis. Although it is desirable to keep all three as small as possible, achieving any two of these objectives always seems to require sacrificing the third. These three "conflicting" goals are discussed in the following paragraphs, along with other parameters affected by the choice of Aperture Duration.

Aperture Duration and Resolution: The aperture duration determines the basic system resolution of the Model 164 Processor Module. If two input signals are separated in time by Δt seconds, and the aperture duration is also Δt seconds, the two signals will be blurred together at the output but will nevertheless still be clearly resolvable. Another way of specifying the resolution limitation is to consider the effective rise and fall time of the Model 164 to be equal to the selected aperture duration. Figure IV-10 shows how the aperture time affects the recovery of an input pulse of duration Δt. Note that the processed waveform, in addition to showing waveshape distortion with wide apertures, also undergoes an apparent time shift equal to the aperture time.

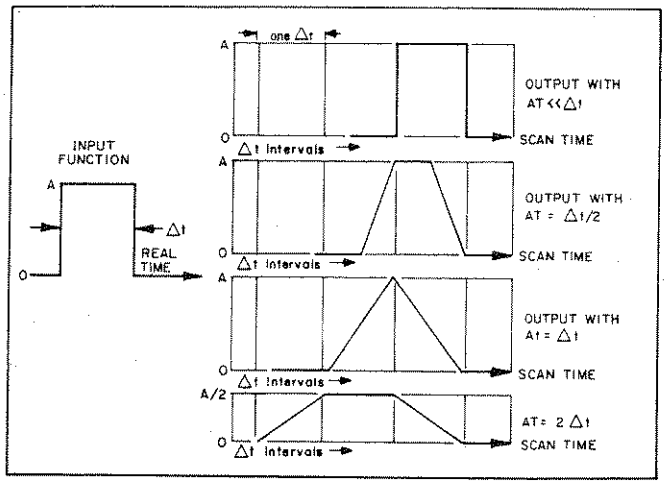


Figure IV-10. RELATIVE DISTORTION OF PROCESSED PULSE AS A FUNCTION OF APERTURE DURATION

Aperture Duration and Operating Time: As explained in the earlier discussion of time constant, the real-time or observed time constant differs from the selected time constant by one over the duty factor, and it is the observed time constant that determines the response time of the instrument when operating.

In single-point analysis, an operating time of five times the observed time constant is required for the output to fully respond (within 1%) to the input signal over the aperture duration interval. Because the observed time constant varies inversely with the selected aperture duration, the use of aperture durations smaller than absolutely necessary unduly prolongs the time required to recover the signal. This becomes even more critical in scanned operation because there the scan time (operating time) required to obtain a step function response equal to that obtainable with point-by-point analysis varies as the inverse *square* of the aperture duration, making it even more important to realistically appraise the required resolution.

Aperture Duration and SNIR: As pointed out in the earlier discussion of time constant, aperture duration and time constant work together to determine the M164 in exponential averaging operation, with the relationship being:

$$SNIR = \sqrt{2TC/AD}$$

The narrower the aperture opening, the better the SNIR will be. The tradeoff one makes is extended operating time. Consider the following example. Suppose one were doing a single point analysis and wished to improve the SNIR by a factor of two by narrowing the aperture duration. From the above expression for SNIR, the aperture duration will have to be reduced by a factor of four to obtain the desired factor of two improvement. In addition, since the operating time varies inversely with aperture duration in single-point analysis, the operating time will have to be extended by a factor of four as well. Now consider the same example but with scanned operation, where the operating time varies inversely with the SQUARE of the aperture duration. There, the same factor of four reduction in aperture duration would necessitate a factor of sixteen increase in operating time. In many applications, a factor of sixteen increase in operating time for a factor of two improvement in SNIR would be a high price to pay. Clearly, in scanned operation anyway, resolution should be the dominant consideration in selecting the aperture duration. Once the aperture duration is set according to the resolution requirements, the time constant can be set as required to obtain the necessary SNIR. Frequently, it will be possible to significantly enhance the overall SNIR by means of the mainframe Signal Processing Time Constant WITHOUT adversely affecting the minimum scan time. See Subsection 4.13E.

Recall that time constant and aperture duration determine the SNIR in exponential averaging operation only. In linear averaging operation, SNIR equals $\sqrt{N}$, where N is the *actual number* of signal repetitions. Time Constant and aperture do, however, determine the magnitude of the volt-second signal increments. For best results, the aperture durations should be set according to the resolution requirements, after which the time constant should be set so that at the end of the analysis, the output level will be as large as possible without overload. If the analysis time (aperture duration times the number of repetitions) equals the selected time constant, exactly full-scale output will be obtained.

Aperture Duration and Duty Factor Limit: A boxcar integrator can be viewed as a modified sample-and-hold circuit. With each repetition of the input signal, a sample is taken for the duration of the aperture opening. During the intervals between aperture openings, the integrator must "hold", that is, it must retain the level reached at the end of the preceding aperture opening. Figure IV-11 illustrates the sampling effect. An input step function is assumed as shown in Figure IV-11a. Figure IV-11b shows the instrument response if an aperture opening very much longer than the time constant is positioned to bracket the step. In such a case, the observed time constant and the selected time constant are the same. Figure IV-11c shows the output response under real operating conditions, that is, where the signal is sampled by an aperture opening very much shorter than the time constant. Each time the aperture opens, the output rises towards G times the input level, with the rate of rise during the aperture opening being that expected from the selected time constant. The real-time or observed time constant is increased according to the duty factor as indicated. Note that the output "holds" during the interval between aperture openings. If the hold capabilities

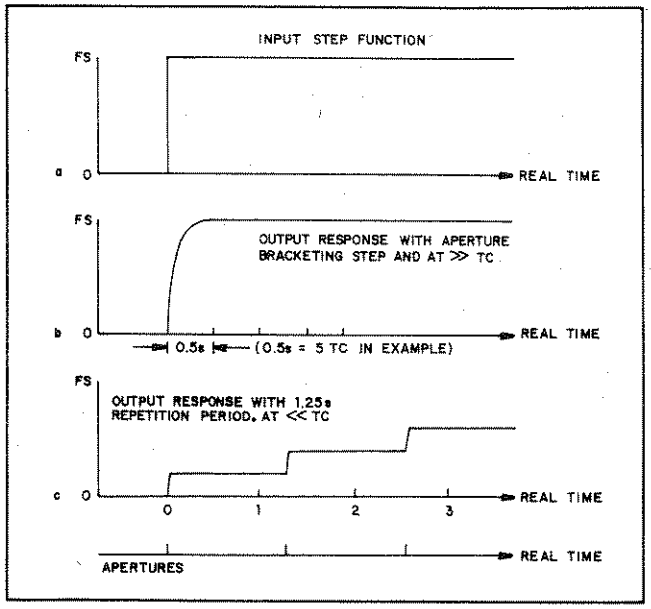


Figure IV-11. EFFECT OF SAMPLING ON INSTRUMENT RESPONSE

are good, the interval between aperture openings can be made very long without any loss of accuracy. If the hold capabilities are poor, considerable droop may occur between aperture openings with the result that instrument performance is degraded.

With each repetition of the input signal, the Model 164 averages over the aperture opening interval only. For all of the time between apertures, the output is expected to hold. It is this ability to hold (or lack thereof) that determines how small the duty factor (ratio of aperture duration to aperture period) can be without adversely affecting the accuracy of the instrument. Although the hold characteristics of the Model 164 are very good, leakage currents do exist that limit how small of a duty factor limit one can have consistent with limiting leakage effect degradation to some arbirarily acceptable level (1% in the case of the Model 164).

It is convenient to express the duty factor limit in terms of the Maximum Trigger Period, P_{MAX} (see Appendix A). For Aperture Durations less than 5 μs, $P_{MAX} = 4 \times 10^7\ C(1 - e^{-AD/\tau})$. For Aperture Durations of 5 μs or longer, $P_{MAX} = 4 \times 10^8\ C(1 - e^{-AD/\tau})$, where:

P_{MAX} is the maximum allowable trigger period in seconds,
AD is the Aperture Duration in seconds,
τ is the Time Constant selected by the Model 164 Time Constant switch, and
C is the integrating capacitor in seconds as determined by the selected Time Constant. The capacitance as a function of Time Constant is:

M164 Selected Time Constant	C, in Farads
1 μs	62×10^{-12}
10 μs	500×10^{-12}
100 μs	5×10^{-9}
1 ms	50×10^{-9}
10 ms	500×10^{-9}
SPEC.	User-determined

Gate Output: A marker pulse which tracks the aperture opening is provided at the Model 164 GATE OUT jack. There is about a 10 ns delay between the leading edge of the aperture opening and the leading edge of the marker pulse. The duration of the marker pulse equals the duration of the aperture opening for aperture openings of 100 ns or longer. The marker pulse amplitude is nominally +1 V into 50 Ω and +5 V into an open circuit. When terminated in 50 Ω, the marker pulse is accurate down to about 50 ns. The marker-pulse circuitry is not fast enough to faithfully reproduce shorter aperture durations.

Note that there is a screwdriver TRIM adjustment associated with the Gate Output. This trim adjustment allows the aperture duration to be varied over a range of 20% of the selected Aperture Duration, thereby enabling precise matching of the aperture opening duration if two Model 164's are used simultaneously to effect dual-channel operation. The selected aperture duration is obtained with the Trim adjustment set to the center of its range.

4.7K DYNAMIC RESERVE

Dynamic reserve is defined as the ratio of the maximum nonsynchronous signal that can be applied without overload to the synchronous input required to give full-scale output. In short, it indicates the level of noise and interference, relative to a full-scale signal, that can be tolerated. If higher levels are applied, non-linear operation results and valid measurements cannot be made. The Overload detect circuits in the Model 164 will cause the Overload indicator lamp to glow whenever the signal applied to the Input exceeds plus or minus 400 mV. It should be noted that this is a conservatively selected overload point. Should the overload light flash occasionally on a noise peak, no detectable signal degradation will occur. However, if the Overload light is on more or less continuously, one can assume that the noise peaks are very much higher than the detect levels and that information loss is occurring. If the input noise exceeds ±400 mV, use of an input attenuator is advised.

4.8 INPUT SIGNAL PROCESSING, MODEL 163

Like the Model 164, the Model 163 Processor Module can be operated in either the "A" or "B" position. The installation consists of sliding the Module into either of the two slots provided in the

Mainframe, followed by securing the module by means of two screws, one at the top of the module panel and one at the bottom. The Model 163 in turn takes a plug-in of its own, namely any one of several Tektronix Sampling Heads. The Sampling Head plugs into the opening in the Processor Module panel and is secured by a spring-loaded latch. Both the Processor Module and the Sampling Head take their power from the Mainframe. It is necessary to have the Mainframe power turned off whenever a Module (or Sampling Head) is being removed or installed.

4.8A INPUT IMPEDANCE, COUPLING, AND RISETIME

These parameters depend on the type of Sampling Head used. A Tektronix instruction manual covering the specific Sampling Head ordered is provided and the operator is advised to consult that manual for all information relating to operation of the Sampling Head. A table comparing the characteristics of several Sampling Heads is provided in Section II of this manual.

It should be pointed out that the overall risetime or resolution of the Model 163 is not necessarily that of the Sampling Head, although the Sampling Head risetime is a contributing factor. With the faster Sampling Heads, timebase jitter will limit the achievable resolution. With the very short aperture durations provided by the Sampling Heads, the jitter becomes appreciable compared to the aperture duration itself. In effect, because the aperture does not always open at the same time, it is "smeared" and increased in duration. The timebase jitter in the Model 163 is nominally 50 ps rms (or 0.05% of the Aperture Delay Range, whichever is greater), and the expression for the net Model 163 risetime, taking into account the risetime of the Sampling Head, is:

$$t_R = \sqrt{(\text{Sampling Head Risetime})^2 + (100\ \text{ps})^2}$$

In short, no matter how fast the Sampling Head is, the net risetime will be no shorter than 100 ps. **NOTE:** The mainframe APERTURE DURATION control has no effect at all on the M163. The control affects the M164 only.

4.8B DC BALANCE

Each Sampling Head is provided with a DC BALANCE CONTROL. This control is on the front panel of the Model S5 Sampling Head. On all other models the adjustment is located at the left side (front view). An extender supplied with the M163 must be used to make the adjustment. In some units there is another adjustment, not dc balance but unlabeled, on the right side. This adjustment absolutely is NOT TO BE DISTURBED. The DC BALANCE is adjusted for zero baseline shift as the Model 163 Sensitivity switch setting is changed. Once adjusted, it generally does not have to be disturbed again. The following procedure can be used to make the dc balance adjustment.

(1) With the Model 163 Sensitivity switch set to 1 V, and with the instrument triggering, adjust the Model 163 Zero control for zero indication on the panel meter. (ZERO should be adjusted with the signal source impedance connected to the Sampling Head but with no signal applied. Any time the source impedance changes the ZERO control must be readjusted, but *not* the DC BALANCE.) **NOTE:** The Mainframe Function switch must be set to "A" or "B" whichever corresponds to the position of the Module being adjusted.

(2) Set the Model 163 Sensitivity switch to 100 mV. Then adjust the DC BALANCE control for zero panel meter indication.

(3) Reset the Sensitivity switch to 1 V, and again adjust the Zero control for zero panel meter indication.

(4) Continue alternating between the 100 mV and 1 V sensitivity settings, while adjusting the DC BALANCE and ZERO controls respectively for zero panel meter indication, until no further improvement in the desired zero can be obtained.

(5) This completes the adjustment. Note that once the dc balance is set, the Zero control setting can be changed at any time as required *without* having to go back and readjust the dc balance. Any change in source impedance will require re-adjustment of the ZERO control.

4.8C SENSITIVITY

Unlike the Model 164 Processor Module, which has a fixed sensitivity of ± 100 mV full scale, the Model 163 has a variable sensitivity as determined by the front-panel Input Range switch that allows full-scale sensitivities of ± 100 mV, ± 250 mV and ± 1 V to be selected. For best results, the switch should be set for as much output as possible without overload.

4.8D DYNAMIC RESERVE

As a result of certain characteristics of the Tektronix Sampling Heads, the dynamic reserve of the Model 163 is limited to 30% of full scale. This means that if the non-coherent input signal (noise) exceeds 30% of full scale pk-pk, non-linear operation will occur with resultant distortion in the recovered waveform. The amount of distortion will be a function of how often the 30% limit is exceeded during the measurement. If the interference is at a single frequency, every cycle of which exceeds the 30% limit, the distortion can be

severe. On the other hand, if the input noise is broad-band, with only an occasional spike exceeding the 30% limit, the distortion will be so small as to be negligible. In absolute terms, the limits are 300 mV pk-pk on the 1 V sensitivity range, 75 mV pk-pk on the 250 mV range, and 30 mV pk-pk on the 100 mV range.

Note that this relatively low noise tolerance does not preclude the examination of extremely noisy signals. For example, assume one wished to examine a 30 mV repetitive signal masked by 300 mV pk-pk of noise. This signal could be recovered with a very great improvement in signal-to-noise ratio by operating on the 1 V sensitivity range. In an application where the input noise is greater than 300 mV pk-pk, use of an external attenuator is recommended. In some applications, it may prove helpful to use an external low-pass filter. The corner frequency of the filter should be higher than the highest frequency components of the waveform to be recovered.

One final word of caution. The OVERLOAD indicator doesn't glow unless the coherent plus non-coherent signal exceeds full scale. As a result, one could be in dynamic reserve trouble without being in overload. It is generally a good idea to use an oscilloscope to be sure the input noise does not exceed the 30% of full scale pk-pk limit. The Model 163 TRIGGER TAKEOFF connector is a convenient point for observing the input signal. The signal here is a $\times 2$ risetime-limited replica (non-inverted) of the input signal and is offset by $+2$ V. Because of the factor-of-two gain, the limits for non-coherent signal at this connector will be 60 mV, 150 mV, and 600 mV pk-pk for the 100 mV, 250 mV and 1 V sensitivity settings respectively. Again, bear in mind that an "occasional" excursion over the limit will be of no consequence.

4.8E SAMPLES AVERAGED, SNIR, AND TRIGGER RATE

The Model 163 is actually a dual-sampler. With each repetition of the input signal, the Sampling Head takes a sample which is ac coupled into the Processor Module. There, a gated integrator samples-and-holds to store the information "bit" taken at the Sampling Head. Each sampling action, the first by the Sampling Head and the second by the Gated Integrator, affects different operating parameters. The Sampling Head, down to the 100 ps limit set by the timebase jitter, determines the effective risetime and hence the resolution. The gated integrator characteristics determine the M163 SNIR and the lowest allowable trigger rate. Unlike the Model 164 in which the aperture duration is variable, the aperture opening of the Model 163 gated integrator is fixed at 0.5 μs. As a consequence of having a fixed aperture duration, some operating parameters are more simply expressed for the Model 163 than for the Model 164. Recall from the Model 164 discussions that for exponential averaging (the only kind of averaging provided in the Model 163), the output represents the average of 2TC/AD samples, providing enough repetitions have occurred to give at least five time constants of analysis time. With a fixed aperture duration, the control or switch that sets the time constant can be directly calibrated in terms of Samples Averaged. This has been done in the Model 163. The SAMPLES AVERAGED switch allows samples averaged totals to be selected in decade increments from 1 to 10^4. The SNIR varies as the square root of the number of samples of which the output is the average. In other words, the expected SNIR is simply the square root of the Samples Averaged switch setting.

As with the Model 164, there are leakage currents present in the Model 163 that limit how small the aperture duty factor can be without degrading instrument accuracy. Because a fixed aperture duration is used in the Model 163, the sole factor to consider is the interval between aperture openings, that is, the trigger repetition rate. With a trigger rate of 5 Hz without baseline Sampling, or 50 Hz with Baseline Sampling, no more than 1% leakage effect degradation will occur. With fast trigger rates, degradation from this source is negligibly small. In a sampling scope application one may be willing to accept somewhat larger aberrations, perhaps on the order of 5%, in which case the limit would be reduced by the same factor. Internal timing requirements also place an upper limit of 10 kHz on the trigger rate when operating a Model 163.

4.8F CLEAR AND ZERO

These functions are provided by a dual-concentric control, with the Zero Adjustment being provided by the outer knob and the Clear action being provided by the inner pushbutton. The Zero Control range is full scale with the Baseline Sampling OFF and 20% of full scale with the Baseline Sampling ON. The Clear pushbutton zeros all of the system integrators as well as the Digital Storage, if appropriate.

4.8G BASELINE SAMPLING

There are two gated integrators in the Model 163. The first of these, the Signal Sampling Integrator, corresponds to the Model 164 gated integrator. The position of the aperture is determined by the Model 162 Mainframe Timing controls, and can be either fixed at any point on the Aperture Delay Range, or scanned across it, in the same manner as for the Model 164. The second gated integrator, the Baseline Sampling Integrator, operates in a similar manner, except that the aperture position is determined either by the Model 163 Baseline Sample Delay controls, or by an externally derived voltage applied to the associated pin jack. In principle, one could even scan the baseline sample by applying a ramp to the external control input. The

external control requirement is +0.225 V to +4.5 V, corresponding to 5%-to-100% of the selected Aperture Delay Range. The input impedance is 5 kΩ.

This basic timing relationship is illustrated in Figure IV-12. Each input trigger is followed by an aperture delay range interval (shown as a pedestal for convenience in illustration) selected at the Mainframe. There are two separate gated integrators, with provision for separately positioning the aperture opening in each. The operator has the choice of operating with only the Signal Sampling Integrator active (Baseline Sample Delay dial fully counterclockwise) or of operating with both integrators active (Baseline Sample Delay dial not fully counterclockwise). If baseline sampling is selected, it takes place on alternate sweeps. In other words, given any succession of triggers, a signal sample will be taken after the first, a baseline sample after the second, a signal sample after the third, another baseline sample after the fourth, and so forth for the duration of the analysis. The important thing is that two separate points are being sampled, and that the "reading taken" for each sample is stored on two separate capacitors.

The voltage on the baseline storage capacitor is subtracted from that on the signal storage capacitor, with the result that the voltage at the output of the Model 163 is *not* the signal amplitude with respect to ground, but rather the signal voltage with respect to the baseline voltage at the sampled point. The utility of baseline sampling is that it renders the Model 163 immune to signal-recovery distortion brought about by baseline drift. As the signal voltage rises and falls with the drift, so does the stored baseline voltage, and the difference always accurately represents the absolute signal amplitude independent of drift effects.

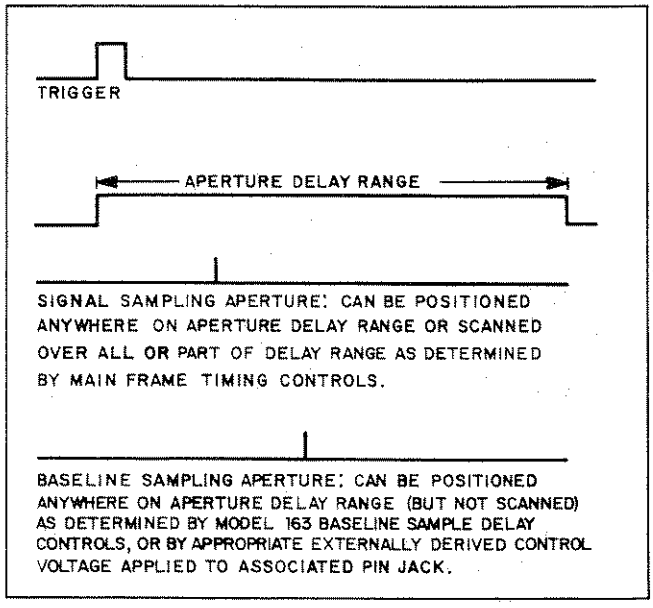


Figure IV-12. BASIC TIMING RELATIONSHIP IN MODEL 163

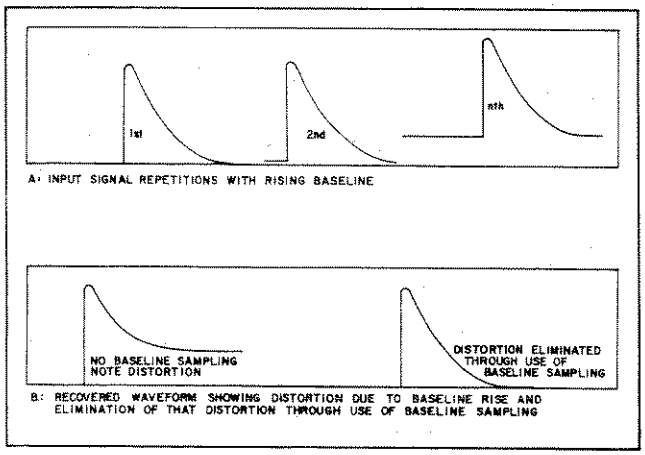


Figure IV-13. EXAMPLE OF DISTORTION CAUSED BY BASELINE DRIFT AND ITS ELIMINATION THROUGH USE OF BASELINE SAMPLING

Figure IV-13 illustrates this principle. Note from Figure IV-13A that there is a steady upwards drift of the baseline (perhaps from heating effects). Suppose one were slowly scanning with successive repetitions in order to recover the signal waveform. As the scan slowly progresses, the output rises with the rise in the baseline, producing the extreme distortion shown in the lefthand illustration of Figure IV-13B. If the same waveform were recovered using baseline sampling, the baseline drift distortion would be corrected, and the signal would be correctly recovered as shown in the righthand illustration of Figure IV-13B. The one tradeoff one makes in using baseline sampling is that the real time required to achieve the necessary five time constants of analysis time is double what it would be if baseline sampling were not used. This results from only half the sweeps being used for signal averaging in baseline sampling operation.

Use of the baseline sampling feature is not limited to drift compensation applications. Whenever baseline sampling is used, the Model 163 output represents the difference between the two sampled points. The baseline sample could as well be a signal sample, if one were interested in the difference between the levels at two different points on the same waveform. The averaging time constant for the baseline-sampling integrator is the same as for the signal-sampling integrator, and the same SNIR considerations apply. One could even scan the baseline-sampling aperture by applying the appropriate control voltage to the Ext. In pin jack, although there are probably relatively few applications for this capability.

4.8H TRIGGER TAKEOFF

This signal is a risetime-limited replica of the input signal to the Sampling Head. The amplitude is twice that of the input signal and is referenced to +2 V. The source impedance is several kilohms. This signal can be used to trigger the mainframe or peripheral apparatus.

The Model 163 front-panel GATE OUT signal allows one to determine the position of both the signal-sampling and baseline-sampling aperture openings. Marker pulses are provided for both aperture openings. The position of the signal-sampling marker pulse is determined by the Model 162 Timing controls. That of the baseline-sampling marker pulse is determined by the Model 163 Baseline Sampling Delay controls. The marker pulses are nominally 0.5 μs in duration. There is about a 10 ns delay between the leading edge of the aperture opening and the leading edge of the corresponding marker pulse.

The position of the baseline-sampling aperture can be controlled either from the Model 163 front panel or by means of an externally derived voltage applied to the associated pin jack. The control is dual-concentric. The inner "knob" is a pushbutton switch that allows the choice of internal or external control. The outer knob sets the actual aperture position. When the control is fully counterclockwise, the baseline sampling feature is turned off. When the control is not fully counterclockwise, the baseline sampling feature is operational, and the delay between triggering and sampling of the baseline is proportional to the control rotation. Fully clockwise corresponds to a delay of 100% of the selected Aperture Delay Range. However, the control is uncalibrated and the precise position of the baseline-sampling aperture must be determined by observing the Gate Out signal. To control the aperture by means of an externally derived voltage, the inner knob is pulled out and the control voltage is applied to the associated pin jack. Plus 4.5 volts applied results in a delay of 100% of the selected Aperture Delay Range. Lower inputs result in lower but proportional amounts of delay. Note that the baseline delay, whether programmed by the external voltage or by the control, will equal that programmed PLUS the minimum achievable delay, nominally 75 ns.

4.8I OUTPUT PIN JACK

This output connector is located just beneath the Model 163 Input Range switch. The Model 163 Output is provided at this connector. The impedance is 1 kΩ. This signal is inverted relative to the signal applied to the M163 Input.

4.9 APERTURE DELAY RANGE

The Aperture Delay Range control defines the interval over which the leading edge of the aperture opening can be positioned. In addition to providing 18 ranges in 1-2-5 sequence from 100 ns to 50 ms, a SPECIAL position is provided in which the Range is determined by a resistor mounted on reserved terminals of the Aperture Delay Range switch. (For safety, resistor to be installed by qualified service technician only.) Figure IV-14 identifies these terminals. The special range is

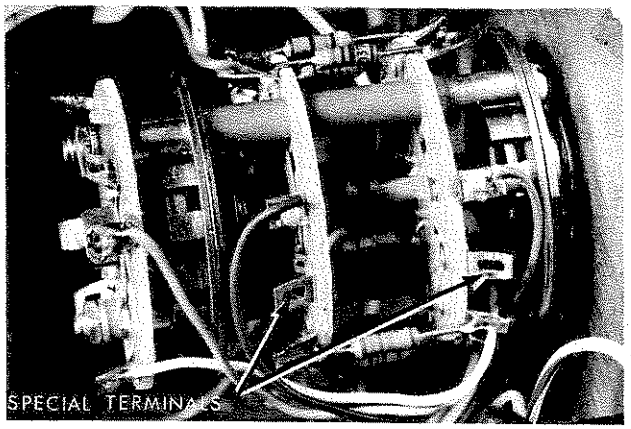


Figure IV-14. SPECIAL RANGE TERMINALS OF APERTURE DELAY RANGE SWITCH

used to obtain Aperture Delay Range intervals intermediate to, or longer than, those provided. The formula relating Aperture Delay Range and the value of this resistor is:

$$R = ADR \div 2.11 \times 10^{-4}$$

where R is the resistance in ohms, and ADR is a dimensionless number equal numerically to the number of ms or ns of ADR desired.

For example, if one desired an Aperture Delay Range of 100 ms, the correct resistor would be $100 \div 2.11 \times 10^{-4} = 474$ kΩ. The inner knob would be set to mSEC.

The choice of Aperture Delay Range bears directly on the ability of the instrument to recover a given waveform. Ideally, the selected Aperture Delay Range should be as short as possible to minimize the effects of aperture delay jitter (50 ps rms or 0.05% of Aperture Delay Range, whichever is greater). At the same time, the time base should not be so short as to cause important signal information to be "lost" because that information falls beyond the end of the selected Aperture Delay Range interval.

4.10 APERTURE POSITION

The position of the aperture opening on the selected Aperture Delay Range interval is determined by the Scan Select controls and also by the % Initial A and % Initial B dials. The Model 162 can perform both single-point and scanned analysis, as selected by the Scan Select pushbuttons. If neither the Scan Select "A" nor Scan Select "B" pushbutton is depressed, single-point analysis takes place at both processor modules. If one of these two pushbuttons is depressed, scanned analysis is performed at the corresponding Processor Module (single-point analysis continues to be performed at the module corresponding to the released pushbutton). If both pushbuttons are depressed, scanned analysis takes place

at both processor modules. Note that depressing the EXT. pushbutton is a convenient way of "releasing" both the A and B pushbuttons to do single point analysis. As long as no external program is applied to the rear-panel SCAN IN/OUT connector, the aperture position is set by the % Initial Delay dials. With regard to the Model 163, only the signal-sampling aperture can be scanned as determined by the Mainframe controls. The baseline-sampling aperture is controlled from the front panel of the Model 163 as described previously.

4.10A SINGLE-POINT ANALYSIS

In single-point analysis, the aperture position is determined by the % Initial A and % Initial B dials. These dials are calibrated directly in % of the selected Aperture Delay Range. For example, suppose the % Initial A dial is set to 40% and the % Initial B dial to 60%. Further suppose the selected Aperture Delay Range to be 20 ms. An examination of the Gate Outputs of the two Processor Modules would show the Processor Module A aperture to be located 8 ms after the trigger (40% $\times$ 20 ms = 8 ms), and the Processor Module B aperture to be located 12 ms after the trigger (60% $\times$ 20 ms = 12 ms). As long as the aperture duration is short relative to the Aperture Delay Range, one can simply speak of the aperture position. However, if the aperture opening is long (a few percent of the Aperture Delay Range or longer), it becomes apparent that the % Initial A and % Initial B dials really set the position of the leading edge of the aperture opening. The position of the trailing edge of the aperture opening depends on the Aperture Duration. It should be mentioned again that the Gate outputs are a good indication of the aperture duration and position for "slow" apertures only. In both the Model 163 and 164 there is about a 10 ns delay between the leading edge of the actual aperture opening and the leading edge of the gate output signal. In the Model 164, the Gate Output (if terminated in 50 Ω) follows the aperture opening for apertures down to about 50 ns. With narrower openings, the Gate Out signal just can't follow. In the Model 163, the Gate Out signal is always 0.5 μs, reflecting the fixed 0.5 μs aperture duration of the gated integrator. (The sampling head is faster, of course, with the sampling-head sample duration varying according to the type of sampling head used.)

Single-point analysis is done when one is interested in the amplitude at one point only of the signal, where the point is defined as the average value of the signal over the aperture duration interval.

4.10B SCANNED ANALYSIS, INTERNAL

In scanned operation, the aperture position is determined by an internally generated scan ramp (except for EXT operation as explained later) and also be the setting of the % Initial A and % Initial B dials. The duration of the scan ramp is set by the Scan Time controls, which allow scan times from 10 ms to 100,000 s to be selected. The selected scan time is the time required to scan the aperture over the entire Aperture Delay Range interval. Frequently it may be desirable to scan over some smaller interval, which is also possible. Figure IV-15 illustrates the basic scanning time relationships. As indicated, a great many repetitions of the basic timing sequence are presumed to occur for one scan ramp. With each repetition, the delay between triggering and the aperture opening increases, linearly tracking the ascent of the ramp. The scan time is normally selected so that many repetitions of the input signal are required for the delay to increase by a single aperture-duration interval. In this way, each point on the signal is sampled many times. (To achieve a resolution commensurate with the aperture duration, it is necessary that each point of the input signal be sampled enough times to be averaged for at least five time constants.)

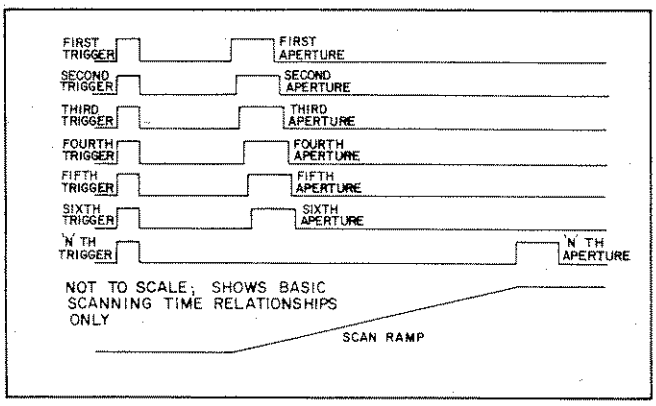


Figure IV-15. INCREASE IN APERTURE DELAY WITH SCAN RAMP

There may be instances where it is unnecessary, or even undesirable, to scan over the entire Aperture Delay Range. Where this is the case, the % Initial A and % Initial B dials can be used to confine the scan to a restricted portion of the Delay Range. In scanned operation, the aperture position at the beginning of each scan is that set by the % Initial Delay dials. A scan always ends when the aperture position (either channel) reaches 100% of the Delay Range. The following example should serve to illustrate these relationships.

Suppose one had a signal for which all of the information of interest fell in the 60% to 100% of Delay Range interval. Assume the instrument was to be operated "single-channel", with the signal to be processed in Channel A. To scan this signal, the "A" pushbutton should be depressed, but not the "B" pushbutton. The % Initial A dial should be set to 60% so that the scan will begin at 60% of the Delay Range. Since Channel B is not being used, and the "B" Scan Select pushbutton is released,

the setting of the % Initial B dial is immaterial. The Scan Time selected is assumed to be 100 s. To begin the analysis, one would probably first depress the Scan Select RESET pushbutton to zero the scan ramp, and then, at some convenient time, release it. While the Reset pushbutton is depressed, the aperture position will be that set by the % Initial A dial, namely 60% of the Delay Range. When the Reset pushbutton is released, the scan ramp will begin rising, and the aperture delay in Channel A will be observed to increase. With a selected Scan Time of 100 s, the rate of aperture delay increase will be 100% of the Aperture Delay Range per 100 s. However, because the initial aperture position is 60%, only 40% of the Delay Range remains to be scanned, and the time required will be 40% of 100 s, or 40 s. After 40 s of scanning, that is, as soon as the aperture reaches 100% of the Delay Range, either of two things could happen. If the SINGLE pushbutton were depressed, the final point sampled would continue to be sampled indefinitely. The aperture position would simply remain at 100% of the Aperture Delay Range. If the Single pushbutton were in the released state, the scan ramp would automatically reset and then start again. In terms of aperture position, the aperture would jump back to 60% as determined by the % Initial A dial, and then slowly scan across the Aperture Delay Range again at the same rate as before. By restricting the scan to that portion of the Delay Range which brackets the signal of interest, the time required to conduct the experiment is reduced from 100 s to 40 s.

It is also possible to scan both channels, if desired, by depressing both the "A" and "B" Scan Select pushbuttons. Note, however, that the scan will end when either channel's aperture reaches 100% of the selected Delay Range. For example, suppose the % Initial A dial were set to 60% and the % Initial B dial to 80%. Further suppose that the selected Scan Time, as before, is to be 100 s. When the Reset pushbutton is depressed, the Channel A aperture will be positioned at 60% of the Delay Range and the Channel B aperture will be positioned at 80% of the Delay Range. When the Reset pushbutton is released, both aperture delays will gradually increase, tracking the ramp. After 20 s, the Channel B aperture will reach 100% of the Delay Range, and the scan will end immediately (hold or reset), even though the Channel A aperture only reached 80%.

This characteristic of terminating the scan as soon as either channel's aperture reaches 100% of Delay Range can be used to advantage in single-channel operation to restrict the scan range. For example, suppose all of the signal of interest fell between 50% and 70% of the Delay Range, and, to conserve operating time, only the 50% to 70% interval was to be scanned. Assuming the signal is to be processed in Channel A, the % Initial A dial would be set to 50%. Because the scan is to cover an interval of only 20% of the Delay Range, the % Initial B dial is set to 80% so that the scan will end at the proper time. Both the "A" and "B" Scan Select pushbuttons should be depressed (it matters not a whit whether there is actually a Processor Module in the "B" Channel slot). When the scan is started, the Channel A aperture will scan from 50% to 70% of the Delay Range, as the Channel B aperture scans from 80% to 100% to terminate the scan.

Note, however, that unless one deliberately intends to limit the scan range in this manner, it is generally advisable to have the Scan Select pushbutton depressed for the active channel only, thereby reducing the likelihood of a short-scan surprise.

A scan in progress can be suspended at any time by depressing the HOLD pushbutton. For the duration that the pushbutton is depressed, the aperture position will not change. Samples will, however, continue to be taken. When the HOLD pushbutton is returned to the released state, the scan will resume and the aperture delay will increase again in the normal manner until completion of the analysis.

4.10C SCANNED ANALYSIS, EXTERNAL

When the Scan Select EXT pushbutton is depressed, the aperture position is determined by a voltage applied to the rear-panel SCAN IN/OUT connector and by the % Initial Delay dials. The sensitivity is 10% of the selected Aperture Delay Range per + 1 V applied. The external voltage will scan either channel or both channels depending on the state of the Scan Select "A" and "B" pushbuttons in the same manner as for scanned operation controlled from the front panel. The % Initial A and % Initial B dials remain active. The aperture delay is given by the sum of the applied voltage and the % Initial Delay dial setting. For example, if the % Initial Delay dial were set to 50%, and + 3 V were applied to the Scan In/Out connector, the resulting aperture delay would be 80% of the Aperture Delay Range. Complex aperture position programs can be applied, the only restrictions being that one must keep the resolution requirements in mind, and that the net effect (dials plus control voltage) should never be such as to try to force a negative delay.

4.11 REAR-PANEL SCAN FUNCTIONS

Three BNC connectors having scan functions are located at the rear panel. The first, the SCAN IN/OUT connector, acts as either an input (Z_{IN} = 10 kΩ) or as an output (Z_{OUT} = 600 Ω) according to the selected scan mode. If the front-panel Scan Select EXT pushbutton is depressed, then this connector serves as an input as described in the previous paragraph. If the Scan Select EXT pushbutton is in the released state, this connector

serves as an output. When the scan is reset (RESET pushbutton depressed), there is 0 V at this connector. As soon as the Reset pushbutton is released and the scan begins, the voltage at the connector rises linearly. The ramping rate is + 10 V per the selected Scan Time. (**NOTE:** The *duration*, as opposed to *rate*, of a scan that goes to completion will nominally be 5-to-10 percent longer than indicated by the panel symbolization, and the final voltage will therefore be proportionally higher.) If the scan is cut short due to the action of the % Initial Delay dials, the final voltage reached will be less than + 10 V. For example, consider a single-channel analysis where Channel A only is to be scanned over the interval of 75%-to-100% of the Delay Range. The Scan Select "A" pushbutton should be depressed and the % Initial A dial set to 75%. (Because the Scan Select "B" pushbutton is not depressed, the setting of the % Initial B dial is immaterial.) Assume a selected Scan Time of 100 s. When the Reset pushbutton is released, the voltage at the SCAN IN/OUT connector will rise linearly from 0 V to + 2.5 V (only 25% of the Delay Range is being scanned, and 25% of + 10 V is + 2.5 V), at which point it would either reset or hold as determined by the state of the SINGLE pushbutton. A single scan will require 25 s (the rate is 10 V per 100 s, but since only 2.5 V is to be scanned, the time required is 25 s). It might be noted that, if neither the Scan Select "A" nor the Scan Select "B" pushbutton is depressed, the voltage at the connector will be + 10 V (assuming previous scan has had time to go to completion). If a scan reset is done under these conditions, the voltage will go to 0 V, and then ramp to + 10 V when the Reset pushbutton is released. The time required will be that selected by the Scan Time controls, independent of the % Initial Delay dials. The Scan output is useful for driving the "X" axis of a recording device, such as an X-Y plotter.

The other two rear-panel scan function connectors provide the CHANNEL A SCAN and CHANNEL B SCAN outputs. The voltage at these connectors is always indicative of the aperture position. In single-scan analysis, the voltage is proportional to the % Initial A and % Initial B dial settings, with + 5 V corresponding to 100% dialed delay. In scanned analysis, the voltage is the sum of the dial setting and control voltage, whether that control voltage is the internally generated scan or the externally derived voltage applied to the SCAN IN/OUT connector. If the scan in progress ends, the scan voltage sets or holds as appropriate.

4.12 SCAN TIME AND RESOLUTION

4.12A INTRODUCTION

In single-point analysis with a Model 164, the resolution is equal to the selected Aperture Duration. In single-point analysis with a Model 163, the resolution equals the Sampling Head risetime, down to the limits imposed by aperture jitter (50 ps rms or .05% of the selected Aperture Delay Range, whichever is greater).

In scanned operation, the aperture duration does not give the resolution directly, but rather sets the maximum resolution that can be achieved. Whether this resolution *is* achieved depends on the choice of Scan Time. If the scan is too fast, detail in the processed output will be lost. The method of determining the minimum scan time differs according to whether the Processor Module is a Model 163 or a Model 164. If two Processor Modules are used, and both are being scanned, the scan time should be no faster than the slower of the two computed minimum scan times.

4.12B MODEL 164

The Minimum Scan Time (MST) of a Boxcar Integrator is determined by the Effective Time Constant (ETC) and by the ratio of the Time Base (TB) to a Resolution Element (RE). The relation between these two parameters and MST is:

$$MST = 5ETC \times TB/RE$$

For the Model 164, ETC has two components. The first is the Signal Processing Time Constant (SPTC), which is selected by the *Mainframe* Time Constant switch. This time constant sets the response time of the Mainframe output circuits. The second component of ETC is the observed time constant (OTC), which sets the response time of the Processor Module. OTC is the time constant selected at the Model 164 divided by the aperture duty factor. OTC is computed by dividing the selected Model 164 Time Constant by the product of the Aperture Duration times the repetition rate. ETC, the time constant used in the scan rate formula, is computed by taking the square root of the sum of the squares of SPTC and OTC.

The TB/RE factor is also easily computed. The Time Base is the selected APERTURE DELAY RANGE, and the Resolution Element is the APERTURE DURATION.

Incorporating these considerations into the above expression for MST, the following expression is obtained.

$$MST = 5[(SPTC)^2 + (OTC)^2]^{1/2} \times \frac{ADR}{AD}$$

Note that if one of the two time constants, SPTC and OTC, is a factor of three or more larger than the other, the effect of the smaller decreases to where it can generally be neglected in the MST computation.

4.12C MODEL 163

The Minimum Scan Time formula (MST = 5ETC × TB/RE) is the same for the Model 163 as it is for the Model 164. However, the parameters ETC and TB/RE are defined differently. For the Model 163, RE = t_R, where t_R is the risetime of the Sampling Head. If t_R is less than 100 ps, substitute 100 ps for t_R in the formula. As with the M164, TB is simply the selected APERTURE DELAY RANGE.

ETC = $[OTC)^2 + (SPTC)^2]^{1/2}$, where OTC is the Observed Time Constant of the Model 163 and where SPTC is the Mainframe Time Constant. OTC, for the Model 163, is given by the formula:

$$OTC = \frac{SA}{2rr}$$

where OTC is in seconds, rr is the trigger repetition rate in repetitions per second, and where SA is the setting of the Samples Averaged switch.

Incorporating these considerations into the general expression for MST, the following expression for the Minimum Scan Time is obtained.

$$MST\ (seconds) = 5[(SA/2rr)^2 + (SPTC)^2]^{1/2} \times ADR/t_R$$

Bear in mind that the minimum value for t_R is 100 ps.

4.13 SIGNAL PROCESSING (MAINFRAME)

4.13A INTRODUCTION

The mainframe Function and Time Constant switches allow further processing of the module output signals. The inner knob of the dual-concentric switch allows the digital storage option, if installed, to be switched on or off. This switch is properly kept in the OFF position if the unit in question is not equipped with the digital storage option or if conditions are such as to make digital storage operation unwarranted. The outer knob, in addition to providing for the selection of the three standard functions provided in all units, also allows any of four optional functions to be selected. Unless the unit is equipped with these options, the switch setting must be limited to the three standard functions.

The response time of the output circuits is determined by the mainframe Time Constant switch, which allows time constants from .1 ms to 100 s to be selected. The mainframe Time Constant affects the overall response time of the instrument and also the signal-to-noise ratio improvement.

4.13B STANDARD FUNCTIONS

(1) A: With the Function switch set to "A", the signal at the output of the Channel A Processor Module is applied to the Mainframe Signal Processing circuits (Buffer Amplifiers, Time Constant, and Output circuitry).

(2) B: As above, but for the Channel B Processor Module.

(3) A – B: As above, but for the difference between the Channel A Processor Module Output and the Channel B Processor Module Output.

4.13C OPTIONAL FUNCTIONS

Three Optional Functions are available. The circuitry for each is contained on a small plug-in circuit card. Two cards can be accommodated at a time, and it makes no difference which option card is plugged into which option connector; the selected option is electrically interposed between the Processor Module Outputs and the Mainframe Processing circuits. If an option is selected for which the circuit card has not been selected, the OPTION light will glow. Figure IV-16 shows a Model 162 with two options installed. It should be noted that none of the options except Digital Storage requires adjusting before being placed in operation.

WARNING!

TO AVOID DANGEROUS, POSSIBLY LETHAL, ELECTRIC SHOCK, DISCONNECT THE M162 FROM ALL SOURCES OF POWER BEFORE REMOVING THE M162's COVER. COMPONENTS AT DANGEROUS LIVE POTENTIALS ARE EXPOSED WHEN THE COVER IS REMOVED. ALLOW SEVERAL MINUTES FOR CAPACITORS TO DISCHARGE BEFORE PROCEEDING.

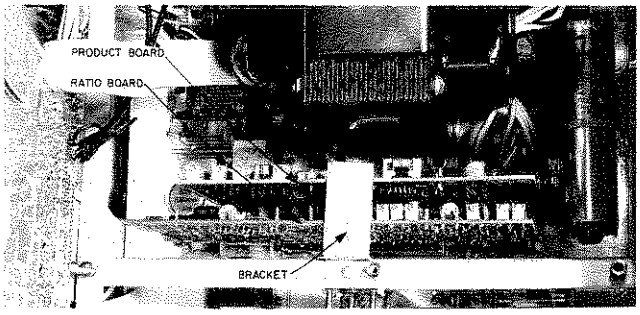


Figure IV-16. MODEL 162 EQUIPPED WITH PRODUCT AND RATIO OPTIONS

If the options are ordered at the same time as the Model 162, they are shipped installed. If ordered at a later date, the customer will usually have to install the options himself. This should prove no problem since the installation in each case is straightforward and can be accomplished in a few minutes. However, for safety, the actual installation should only be performed by a qualified service technician. With the exception of the Digital Storage Option, the option circuitry in each case

is located on a small plug-in board which mounts in either of two special connectors that are directly in front of the power transformer. If two options are to be installed at the same time, it doesn't matter which option plugs into which of the two connectors. When a given option is selected at the front panel, that same option is selected internally, independent of the connector the option is plugged into. The Digital Storage Option is a special case in that its circuitry is located on a large circuit board that mounts above the upper mainframe board and in parallel with it. Installation of the Digital Storage Option is treated in detail further on. The instructions that follow describe how to install one (or two) of the plug-in option cards.

(1) The first step is to remove the top cover, which is secured by two screws on the underside of the top-cover overhang at the rear of the instrument.

(2) Notice whether the instrument is fitted with a Digital Storage board. If it is, the Digital Storage board must be removed temporarily. This board is secured by six screws. The cable interconnecting it and the mainframe circuitry simply unplugs.

(3) If the instrument does not have a Digital Storage board, or if it does have one and it has been removed as described in the preceding step, remove the four screws (two will be standoffs if the unit has digital storage) that secure the upper mainframe board. With the four screws removed, the board can be rotated up and to the left. (The hinges are located at the left edge of the board facing the unit from the front.) Once the board is up, a short length of string or wire can be used to tie it in position so that it will be out of the way.

(4) It should now be possible to see and gain access to the two option board connectors located immediately in front of the transformer. The next step is simply to plug the option board(s) into the connector(s). It doesn't matter which board plugs into which connector. The component side of the boards should face the transformer.

(5) Next secure the board(s) with the small bracket provided for this purpose. The bracket is fastened to a cross-rail by a single screw. There are two other screws in the bracket as can be seen from the photograph. Each of these screws passes through the bracket and threads into a small securing block on each option board. With the screws installed, there is no possibility of the option boards vibrating loose.

(6) Lower the upper mainframe board into place and secure it with the screws removed earlier.

(7) If a Digital Storage board was removed in step 2, return it to its proper position and secure it. Do not forget to reconnect the cable. Last of all, return the cover, completing the procedure.

Before considering the individual options, note that all three can be used for ratio measurement. In doing ratio measurements, one must take care to consider the relative response time of the two channels. If a single-point analysis is being performed, with sufficient time given for both A and B to reach their final value, the response time of one channel relative to the other is not important. On the other hand, if the output data is being examined before either or both channels reach the final value, then care must be taken to make the observed time constant the same in both channels. Otherwise gross errors in interpreting the data could occur. The situation is the same in scanned operation. If one is scanning so slowly that both A and B follow the equivalent input waveform, the relative response time is no problem. However, if one channel or the other is being scanned a bit too fast for "good fidelity", it becomes critical that the observed time constant in both channels be the same.

The characteristics of the individual options are described in the following paragraphs.

(1) log (A/B): this option significantly extends the versatility of the system. In particular, it is well suited for use in optical density studies because it allows the density to be plotted directly, where density is defined by the relationship:

$$\text{Density} = \log_{10}(I_O/I)$$

Also, this option is well suited to fluorescence and phosphorescence decay studies where multiple decay times exist. Because the transfer function of such a reaction is $E_O/E_{IN} = 1 - e^{-t/\tau}$, the various decays may plot as a series of connected straight lines segments of decreasing slope, with the inflection points marking the decay rate transitions.

Best accuracy is obtained with B as large as possible. The actual transfer function for the log ratio option is:

$$E_O/E_{IN} = 4.00 \log_{10}(|A|/|B|)$$

(2) A/B: This is the ratio option for which full specifications are provided in Section II. The transfer function is:

$$E_O/E_{IN} = 10(A/|B|)$$

(3) A × B: This is a dual-function option. It can operate as a multiplier (FUNCTION switch to A × B and mode switch on Option board to A × B) or as a ratio computer (FUNCTION switch to SPEC and mode switch on Option board to A/B). Thus this option offers extended versatility at the expense of slightly degraded performance in the ratio mode (ratio accuracy is better for the ratio only option). The specifications for this option are provided in Section II. The transfer functions for the two modes are:

As a multiplier: $E_O/E_{IN} = 0.1\ A \times B$

As a ratio computer: $E_O/E_{IN} = 10(A/|B|)$

(4) SPEC: In this position, a special option constructed by the operator on a suitable circuit board (blank boards can be purchased from EG&G Princeton Applied Research Corporation) can be selected. This is also the proper setting to obtain ratio operation with the Multiplier board, providing the mode switch on the multiplier option board is set to A/B.

The chassis Wiring Diagram on page VII-17 shows the connections to the two option connectors, which are wired in parallel. The FUNCTION switch simply selects the proper output lines. As shown in the diagram, the output of processor module A is applied to pin 22 and the output of processor module B is applied to pin 24. With the FUNCTION switch set to SPEC, pin 26 (output of "special" circuit) of the Option connectors is routed to the mainframe Signal Processing circuitry. Pins 36, 38, 40, 42, and 44 control the OPTION light. Each Option board applies ground to one of these lines (any special board should be constructed so that ground is applied to pin 42). The Option light circuitry is arranged such that the OPTION light will glow if the ground is missing for the selected board (ground would normally be missing only if the board itself were missing). Recall that with the Multiplier Option installed, ratio operation can be obtained in the SPEC position if the switch on the option board is set to A/B. Consequently, one cannot select special board operation if a multiplier board having its mode switch in the A/B position is installed. In wiring a special option then, the A and B inputs respectively will be taken from pins 22 and 24. The output must be made available at pin 26, and ground should be furnished to pin 42. + 15 V will be available at pin 2, − 15 V at pin 6, + 5 V at pin 10, and ground at pins 14 and 18 (high quality gnd). Do not use pins 22, 24, 28, 30, 32, 36, 38, 40, and 44.

Situations may arise where, even though only a single Processor Module is in use, it may nevertheless be desirable to operate in an option mode. Where this is the case, it will be necessary to synthesize the B Processor Module output by applying a dc voltage (+ 10 V is best for ratio operation) to either pin 1 or pin 50 of the rear-panel 50 pin interface connector, P101. Ground is available at pins 23, 24, 27, and 28. A mating connector and cable are supplied with the system to facilitate operating in this manner.

4.13D OUTPUTS

Providing sufficient processing time has elapsed for a Processor Module to completely respond to an applied signal, the signal at its output will be an inverted replica of the average value of the input signal over the aperture interval. This signal is either applied directly to the mainframe output circuits (standard functions) or passed through optional processing circuits first (option installed and selected). In any case, the signal applied to the output circuit is first inverted. After inversion, the signal branches into two paths, one to provide the f(t) Output signal, and the other to provide the $\dot{f}(t)$ Output signal. Both outputs are affected by the Mainframe Time Constant. The panel meter indicates the f(t) Output only. The transfer functions for the two outputs are discussed below.

(1) f(t): This is the "normal" output, that is, it is at this output that the scan-time replica of the input signal is made available, with reduced noise content as determined by the operating parameters. Taking either the Processor Module output, or the Option board output, whichever is appropriate, as E_{IN}, the transfer function for this output is:

$$f(t)/E_{IN} = 1/(1 + j\omega\tau)$$

where $\omega = 2\ \pi f$, and τ = mainframe time constant.

(2) $\dot{f}(t)$: This is a "pseudo-derivative" output, that is, it is proportional to the time rate of change of the Processor Module output or Option output. With E_{IN} defined as indicated above, the transfer function for this output is:

$$\dot{f}(t)/E_{IN} = (kA/9)[1/(1 + 1/j\omega\tau)]$$

where ω and τ are as defined above; A is a multiplying factor dependent on the setting of the inner knob of the Time Constant control, which allows values for A from × 10 (CAL. setting) to × 1 (× 10 setting) to be selected; and k is another multiplying factor

dependent on the setting of R128A, the RATE adjustment. This adjustment is located on the lower M162 circuit board immediately behind the $\dot{f}(t)$ connector. It is the adjustment at the right-front corner of the board, next to the METER adjustment, and is accessible from above when the top cover is removed. The RATE adjustment provides a $\times 1$ to $\times 50$ adjustment range for k. Units are shipped with $k = 10/2\pi$.

It should be noted that the setting of the inner Time Constant control knob has a dual effect with respect to the $\dot{f}(t)$ output. Not only does it act as a kind of gain control as described above, but it also works together with the outer knob to determine the time constant in the same manner as for the f(t) output.

4.13E SIGNAL-TO-NOISE AND MAINFRAME

As explained previously, the Processor Module provides an improvement in signal-to-noise ratio, with the improvement varying with the square root of the number of samples of which the Processor Module output is the average. In the mainframe, a low-pass filter is interposed between the Processor Module output and the f(t) output. The passband of the filter is set by the mainframe Time Constant, with the 3 dB down frequency being $1/2\pi\tau$. This filter provides additional noise reduction, that is, the noise content of the signal at the f(t) output is less than at the Processor Module output. (**NOTE:** The $\dot{f}(t)$ exhibits a high-pass characteristic with the 3 dB down frequency equal to $1/2\pi\tau$.)

The analysis of the relationship between the Processor Module operating parameters and the mainframe time constant (MTC) as it relates to noise reduction is complex, and no simple expression defining the net signal-to-noise ratio improvement can be given. Nevertheless, some general guidelines can be offered. A key parameter is the trigger repetition frequency. The most important noise components out of the Processor Module are concentrated in a frequency band having the trigger repetition frequency as its upper limit. If the 3 dB down frequency of the MTC filter is below the trigger repetition frequency, the MTC filter will provide additional noise reduction. If the 3 dB down frequency is above the trigger repetition frequency, there will be no significant additional noise reduction. In most experiments, significant additional noise reductions can be achieved, and, in fact, the noise reduction provided by the mainframe filter can equal or surpass that achieved in the Processor Module. However, if the MTC is of the same order as, or larger than, the Processor Module observed time constant, then the real time required to make a measurement is increased. In terms of scanned operation, a slower scan is required to maintain the same resolution. The following example illustrates how the MTC can be used to significantly improve the noise reduction without degrading the scan time requirement.

Given: M162 equipped with a M164. Critical parameters are: $AD = 10^{-5}$ s, $f_{TR} = 10^3$ Hz; and PMTC = 10 ms (maximum).

Problem: To determine the largest MTC that can be used without requiring increased scan time and to estimate the additional noise reduction that can be achieved with MTC computed.

Solution: The OTC of the Processor Module = $PMTC/(AD \times f_{TR}) = 1$ s. Therefore, as long as the MTC selected is a factor of three or more smaller than 1 s, slower scanning will not be necessary. Let us assume then that a MTC of 100 ms is selected.

The 3 dB down frequency of the mainframe filter with a 100 ms time constant will be 1.6 Hz, well below the f_{TR} of 10^3 Hz. Thus a significant additional noise reduction can be expected. To a VERY ROUGH approximation, with the filter corner frequency being so much lower than the f_{TR} frequency, the mainframe noise reduction will vary as the square root of the ratio of f_{TR} to f_{3dB}, approximately 25. The processor module noise-reduction factor $(2\tau/AD)^{1/2}$ is 45. the overall noise-reduction factor will be the product of the two factors, about 1100. Although the computed additional noise reduction achieved in the mainframe may differ considerably from that estimated, it is nevertheless clear that use of the MTC allows a noise reduction to be achieved that is very much greater from what one would expect from the maximum M164 Time Constant of 10 ms, and without increased scan time.

4.14 DIGITAL STORAGE OPTION

4.14A OPERATION

One characteristic of a perfect boxcar integrator is that its output level does not change between aperture openings. Such a boxcar integrator is described as having an infinite hold time. One resulting benefit is that the signal-recovery capabilities of the instrument would be independent of the aperture duty factor. Expressed another way, for any aperture duration, the trigger repetition rate could be made low without limit and still not have an adverse effect on the instrument's signal recovery capabilities.

Unfortunately, real instruments seldom equal the projected performance of a perfect "model" and the Model 162 is no exception. Leakage currents

from various sources cause the voltage at the output to change between aperture openings. Whereas the output changes that occur during aperture openings due to input signal tend to bring the instrument output level to $G \times E_{IN}$ (G is the gain), the output changes that occur between aperture changes as a result of leakage currents tend to bring the instrument output level away from $G \times E_{IN}$. Depending on the relative amplitude of the two effects, there will always be some degree of error. By properly choosing the operating parameters, the error can usually be made negligibly small.

Consider the case where a full-scale input (single point) is to be recovered by exponential averaging (M163 or M164 in EXP. mode). For the early aperture openings, the output change per aperture opening will be large because the RC charging curve initially has a rapid rise. By the time enough aperture openings have occurred to give a total open-aperture time of one time constant, the output will be at 63%, and the incremental output change per aperture opening will be less due to the decreasing slope of the RC curve. As the experiment continues, the output will continue to rise towards $G \times E_{IN}$, but the incremental change per aperture opening will continue to decrease. The limit is reached when the incremental output change per aperture opening due to signal is exactly equal to that which occurs between aperture openings due to leakage. No matter how many more times the aperture opens, the output level will simply "sawtooth" about the equilibrium point. If the operating parameters are selected such that the equilibrium point is very near $G \times E_{IN}$, leakage effect errors will be negligibly small. What this means practically is that as long as the hold-time limits for the Processor Module are not exceeded, error due to leakage effects will be no greater than 1% of full scale. In other words, assuming a full-scale input, the equilibrium point will occur within 1% of full scale. If the hold-time limitations are exceeded, larger errors will occur. In fact, under extreme conditions, the error can be so great as to render the instrument virtually useless unless it is equipped with the digital storage option.

In most applications, leakage effect degradation can be greatly reduced by use of the digital storage option. Two digital channels are provided, allowing two Processor Modules to be accommodated at once. However, there are operating restrictions. First, a Model 163 cannot be operated in the Baseline Sampling Mode when the Digital Storage Option is activated. Second, the Digital Storage Option must be aligned to match the Processor Module with which it is to be used. As a result, the two digital storage channels are specific with regard to processor module position. If the digital storage option is aligned to operate with a specific Processor Module in slot "A", and another in slot "B", the two modules cannot be interchanged (unless, of course, one operates with the digital storage OFF).

The digital storage option itself exhibits a short-term drift (±0.2%/minute, or less). This drift can produce total deviations of ±4% of full scale, but no more. Even though this drift stops when it reaches 4% of full scale, it nevertheless limits the hold-time performance (minimum trigger rate commensurate with no more than 4% of full-scale error).

With the specified drift rate of 0.2%/minute, the 4% hold time of the digital storage unit can be stated as 20 minutes or 1200 s. Thus, whenever the hold time of the processor module is less than 1200 s, the digital storage can be switched on to achieve an overall hold time of 1200 s. In short, the minimum trigger rate commensurate with no more than 4% of full-scale error can be extended down to 1/1200 Hz by use of the digital storage.

At trigger frequencies below 1/1200 Hz (digital storage operating), the situation is exactly analogous to that without digital storage. There is an output level change between aperture openings (always 4%) that tends to bring the output level away from $G \times E_{IN}$. During each aperture opening, there is an output level change due to the applied signal that tends to bring the output towards $G \times E_{IN}$. As before, there will be an equilibrium point somewhere on the RC curve where the two effects balance, and that point will be where the signal increment is exactly 4% of full scale. No matter how many more aperture openings occur, the output will move no closer to $G \times E_{IN}$. The error can be small (equilibrium reached near the asymptotic part of the curve) or large (equilibrium reached near the beginning "steep" part of the curve).

One technique that can sometimes be used to good advantage when working at an extremely low repetition rate is to use linear averaging, in which the output change per aperture opening is always the same. This way, if the aperture duration and time constant are selected to give greater than 4% output change during each aperture opening, there is no limit in how low the trigger rate can be. There will, however, still be an error equal to N%, where N is the number of repetitions. By noting the *direction* of the error, it can easily be allowed for in evaluating the final output level. Note that pseudo-linear averaging can be accomplished with a Model 163 by operating only on the early "linear" portion of the RC curve. Providing the number of repetitions is kept low enough so that, with a full-scale input applied, the output (ignoring leakage) doesn't exceed 63% (nominally) of $G \times E_{IN}$, the situation is analogous to LIN. averaging with a Model 164 and the same principles apply.

It should be noted that digital storage does not occur for the entire interaperture interval. Figure IV-17 shows the digital storage timing relationships. Note that each time the unit is triggered, a Delay Range Frame is generated. The frame duration equals the selected Aperture Delay Range plus a few percent. If the digital storage is activated, a 1 ms ENCODE command is produced at the end of the Delay Range Frame. During the ENCODE command, the digital storage circuitry reads the analog stored level, and does an A-to-D-to-A conversion. At the end of the ENCODE command, the encoded data is fed back to the analog integrator in such a way as to hold the instrument output unchanged (except for 4% of f.s. short-term drift) until the next trigger. Note that the trigger repetition rate can be no faster than allowed by the sum of the Delay Range Frame and ENCODE, and, in fact, a small settling time in addition should be provided. Generally speaking, if the situation is such that the Digital Storage prevents one from triggering as rapidly as desired, it is almost certain that digital storage need not be used in the application. Furthermore, if digital storage *need* not be used, it *should* not be used. In situations that don't really call for digital storage, better results will be obtained with it turned off.

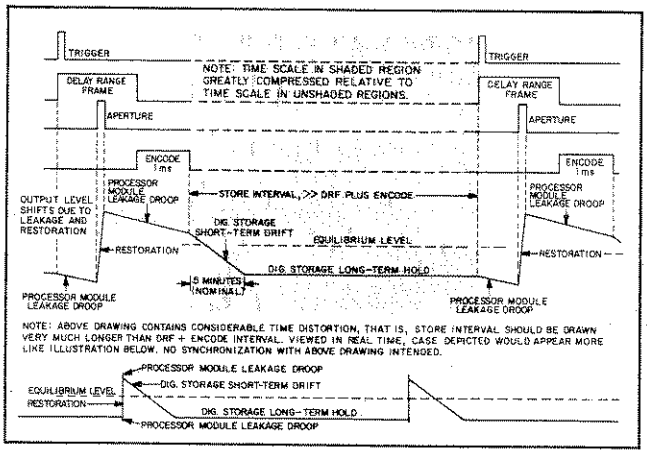


Figure IV-17. DIGITAL STORAGE OPTION TIMING

No digital storage takes place over the interval bounded by the sum of the Delay Range Frame plus the ENCODE command. Thus even with the digital storage option installed and active, there is a portion of each cycle when the hold-time characteristics of the Processor Module dominate. For optimum performance, this portion should be kept as small as possible. Practically speaking, this means that the selected Aperture Delay Range should be no longer than necessary.

Operation with digital storage can be summarized as follows.

(1) MODEL 163: If the trigger rate is faster than 5 Hz, do not use digital storage. If the trigger rate is lower than 5 Hz, use digital storage. It should be possible to achieve trigger rates as low as 1/1200 Hz without leakage errors exceeding 4% of full scale (nominal). Errors will be larger with lower trigger rates. In certain applications it may prove advantageous to use the pseudo-linear averaging technique. Bear in mind that one cannot use digital storage in conjunction with baseline sampling (no harm will result but the digital storage option will not improve the instrument's performance).

(2) MODEL 164: If the trigger period is shorter than P_{MAX}, do not use digital storage. If the trigger period is longer than P_{MAX}, use digital storage. It should then be possible to trigger as low as 1/1200 Hz without leakage errors exceeding 4% of full scale (nominal). Errors will be larger with lower trigger rates. In certain applications involving very low trigger rates, it may prove advantageous to use linear averaging instead of exponential averaging.

(3) Any time digital storage is used, be sure that the selected APERTURE DELAY RANGE is no longer than necessary.

It should be noted that the hold-time characteristics of some processor modules will be much better than specified. Similarly, the short-term drift rate of some digital storage units will be much better than the specified 4% in 1200 s rate. As a result, one may find that the minimum trigger rate commensurate with 4% leakage degradation will be much lower than specified for some Processor Modules, or that a given digital storage option will actually hold the leakage error to 4% for trigger rates lower than 1/1200 Hz.

4.14B DIGITAL STORAGE INSTALLATION

The Model 162 can be purchased with or without the Digital Storage Option. If purchased with the option, the option is installed at the factory. If the Digital Storage Option is not purchased initially, but rather at some later date, the installation would ordinarily be done in the field. Those options to be installed in the field are prealigned as much as possible. However, some adjustments have to be made in the field to match the option characteristics to the specific Processor Module with which it is to be used. The installation procedure follows. For safety, the installation should only be performed by a qualfied service technician.

(1) Check to be sure that the Model 162 line cord is unplugged. Then remove the top cover, which is secured by two screws on the underside of the overhang at the rear of the instrument.

(2) Remove the four screws that secure the mainframe upper circuit board in place. With the screws removed, it should be possible to rotate the board upwards (hinges are at left edge of board).

(3) Take four of the six standoffs supplied and mount them with nuts in the four holes indicated in Figure IV-18. Note that these are NOT the four holes from which the screws were removed in the preceding step.

(4) Rotate the board back to its original position and secure it, using two of the screws removed in step 2. Figure IV-18 indicates where the screws are to be located.

(5) Take the remaining two standoffs and screw them into the front pair of holes as indicated in the figure.

(6) Position the Digital Option board, component side up, and with the cable extending to the left, above the mainframe upper circuit board such that each of the six option-board mounting holes is directly above the corresponding mounting post (standoff) installed in the preceding steps.

(7) Secure the Digital Option board to the six mounting posts, using the six 9/16" long standoffs/screws provided.

(8) Plug the option-board cable into the sixteen pin matching connector located towards the left-hand edge of the mainframe upper circuit board. **NOTE:** Do not "twist" the cable. Just fold it naturally and plug it in. Pay no attention to any "mismatch" of connector-pin numbers.

This completes the Option board installation. The alignment (zero and gain adjustments) follows.

4.14C MATCHING DIGITAL STORAGE OPTION TO PROCESSOR MODULE

The following procedure (to be performed by qualified service technician only) sets the zero and gain for both Digital Storage Channels. Four adjustments are involved; the others should be left undisturbed. This procedure should be used whenever it is necessary to match the digital storage option to a Processor Module. Once matched to a given Processor Module operating in a given channel, the adjustments need not be disturbed again, except possibly as part of a regular maintenance program. However, if any other Processor Module is to be operated in the same channel, with the digital storage turned on, the alignment will have to be repeated for that channel if proper operation is to be obtained.

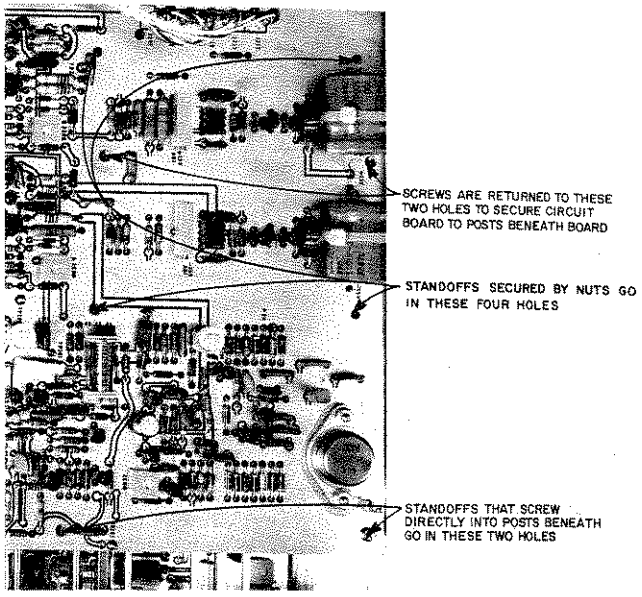


Figure IV-18. MODEL 162 UPPER CIRCUIT BOARD SHOWING DIGITAL STORAGE OPTION MOUNTING HOLES

(1) Prelimnary Steps

(a) Plug in the line cord, turn on the power, and allow a half-hour warmup. **NOTE:** The assumption is made that the Processor Modules to which the Digital Storage Option is to be matched have been installed. If there is but one Processor Module, place it in the Channel A position and do the Channel A adjustments only. The Channel B adjustments can be performed later if a second Processor Module becomes available. If a Model 163 is involved, the Sampling Head should be installed and the DC BALANCE adjusted.

(b) Set the mainframe controls as follows.

Aperture Delay
  % Initial A: 10%
  % Initial B: 10%
  Range: 5 mSEC
Aperture Duration: 5 μSEC and CAL
Scan Time: setting immaterial
Scan Select pushbuttons: EXT depressed; all others released
Trigger Mode pushbuttons: LINE depressed; all others released
Trigger Level: Adjust for proper triggering as indicated by steady glow of TRIGGERED light
Function switch
  Outer knob: A
  Inner knob: DIG. STORAGE ON
Time Constant: 0.1 mSEC

(c) Set the controls of Model 164 Processor Module(s) as follows.

Time Constant: 1 μSEC
Pushbuttons: Select EXP, GROUND, DC, and 50 Ω

(d) Set controls of Model 163 Processor Module(s) as follows.

Sensitivity: 1 V
Samples Averaged: 10
Baseline Sample Delay
Outer knob: fully counterclockwise
Inner pushbutton: pressed IN

(2) Zero Adjustments (Figure IV-19)

(a) Set the Channel A Processor Module ZERO control (M163 or M164; it makes no difference) for "0" panel meter indication.

(b) Connect the oscilloscope to the Channel A Processor Module OUTPUT pin jack. The scope sensitivity should be 10 mV/cm, and the sweep rate should be 2 ms/cm. The oscilloscope should be LINE triggered and it should be DC coupled.

(c) Set the CHANNEL A ZERO adjustment (Dig. Storage Option board) for minimum pedestals in the oscilloscope display.

(d) Set the mainframe FUNCTION switch to B. Then adjust the Channel B Processor Module ZERO control for "0" panel meter indication.

(e) Connect the oscilloscope probe to the Channel B Processor Module OUTPUT pin jack. Then set the CHANNEL B ZERO adjustment (Dig. Storage Option board) for minimum pedestals in the oscilloscope display.

(f) Set the FUNCTION switch back to A.

(g) Make provision for measuring the voltage at the f(t) mainframe output.

(h) Press CLEAR at the front-panel of the "A" Processor Module.

(i) While continuing to press CLEAR, adjust R9954 (left-front corner of Digital Storage circuit board facing unit from front) for 0 V at the f(t) Output connector.

(j) Set the FUNCTION switch to "B".

(k) Then press CLEAR at the front panel of the "B" Processor Module.

(l) While continuing to press CLEAR, adjust R9997 (left-rear corner of Digital Storage circuit board facing unit from front; see page VII-24 if there is any doubt as to the identity of R9997) for 0 V at the f(t) Output connector.

(m) Set the FUNCTION switch ack to A and go on to step 3.

(3) Gain Adjustments (Figure IV-19)

(a) Change the oscilloscope to ac coupling.

(b) Turn the Digital Storage OFF (inner knob of FUNCTION switch).

(c) If Channel A Processor Module is a Model 164, release GND pushbutton and depress CAL pushbutton. Then set the CAL screwdriver adjustment for exactly full-scale panel meter indication.

If Channel A Processor Module is a Model 163, connect + 1 V to the Model 163 Input. Then trim value of applied dc as required to obtain exactly full-scale panel meter indication.

(d) Turn the Digital Storage Option ON (inner knob of FUNCTION switch).

(e) Connect the oscilloscope probe to the Channel A Processor Module Output pin jack. Then set the CHANNEL A GAIN adjustment (Dig. Storage Option board) for minimum pedestals in the oscilloscope display.

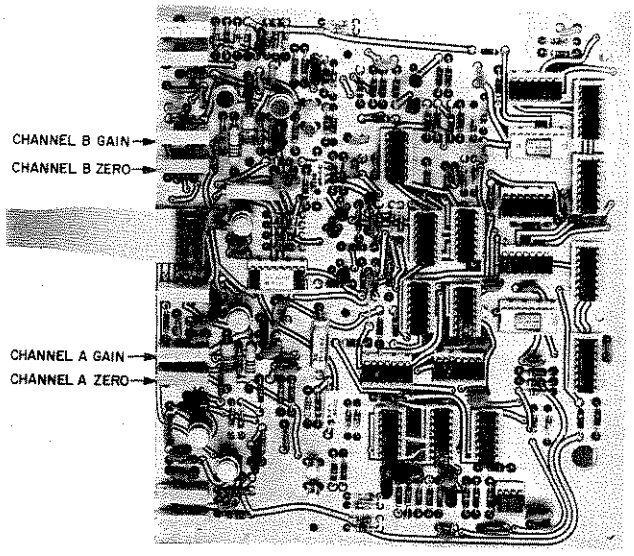


Figure IV-19. DIGITAL STORAGE ZERO AND GAIN ADJUSTMENTS

(f) Set the FUNCTION switch to B and turn the Digital Storage OFF (inner knob of FUNCTION switch).

(g) If the Channel B Processor Module is a Model 164, release GND pushbutton and depress CAL pushbutton. Then set the CAL screwdriver adjustment for exactly full-scale panel meter indication.

If the Channel B Processor Module is a Model 163, connect +1 V to the Model 163 Input. Then trim value of applied dc as required to obtain exactly full-scale panel meter indication.

(h) Turn the Digital Storage Option back ON.

(i) Connect the oscilloscope probe to the Channel B Processor Module OUTPUT pin jack. Then set the CHANNEL B GAIN adjustment (Dig. Storage Option board) for minimum pedestals in the oscilloscope display.

(4) Final Checks

(a) The panel meter indication at this point should be full scale. Press in the EXT Trigger Mode pushbutton. The panel meter indication should not change.

(b) Set the FUNCTION switch back to A. The panel meter indication should be full scale.

(c) Momentarily depress the Channel A Processor Module CLEAR pushbutton. The panel meter indication should go to zero.

(d) Set the FUNCTION switch back to B. The panel meter indication should be "0".

(e) Ground the input of the Processor Module(s). In the case of a Model 164, this is done by depressing the GND pushbutton. In the case of a Model 163, the dc source should be removed and a grounding plug connected to the input in its place.

(f) Depress the LINE Trigger Mode pushbutton. Then vary the Channel B Processor Module ZERO control over its entire range. The output indication should smoothly track the Zero Control setting. The range of the control should be nominally full scale, though not necessarily symmetrical with respect to "0".

(g) Set the FUNCTION switch to A. Then repeat the Zero Control check described in the previous step, this time using the Channel A Processor Module ZERO control.

THIS COMPLETES THE ALIGNMENT STEPS NECESSARY TO MATCH THE DIGITAL STORAGE OPTION TO THE PROCESSOR MODULES WITH WHICH IT IS TO BE USED. NOTE THAT IN EVERY APPLICATION REQUIRING DIGITAL STORAGE, THE PROCESSOR MODULES WILL HAVE TO BE OPERATED IN THE SAME POSITION AS FOR THE PRECEDING ALIGNMENT. IF A DIFFERENT PROCESSOR MODULE IS USED, THE ALIGNMENT WILL HAVE TO BE REPEATED WITH THAT MODULE.

4.15 READOUT AND RECORDING

In single-point analysis, the panel meter allows accurate readings to be taken of the average signal level over the aperture duration interval. Better readout resolution can be obtained by monitoring the output with a differential or digital voltmeter. This better resolution is provided automatically in units equipped with a digital panel meter.

For reading out a scanned analysis, any of several different type devices can be used. Strip-chart recorders, X-Y plotters, oscilloscopes, and scope monitors are all suitable in particular applications. Probably the most important single factor to consider in the choice of recording device is the intended scan speed. Assuming the scan time is of the order of the resolution requirements of the signal being analyzed, important detail will be lost if the scan is too fast for the readout device. Excessively slow scan times can cause other troubles with some readout devices. Generally speaking, a strip-chart or X-Y recorder is used with a slow scan. Oscilloscopes and scope monitors are used with a fast scan.

If an X-Y plotter is used, the X axis drive is best developed from one of the rear-panel outputs. The signal at the SCAN IN/OUT connector is probably best suited to this application because it begins at 0 V. Note that access to pen-lift relay contacts is provided at the rear-panel Interface connector (see Table IV-1). Operation in conjunction with scope monitor such as the Tektronix type 604 is facilitated by making use of the internally generated scope retrace-blanking signals, also provided at P101 as indicated in Table IV-1.

SECTION V
ALIGNMENT

5.1 SAFETY NOTICE

WARNING!

POTENTIALLY LETHAL VOLTAGES ARE PRESENT INSIDE THIS APPARATUS. These service instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Any adjustment, maintenance and repair of the opened apparatus under voltage shall be avoided as far as possible and, if unavoidable, shall be carried out only by a skilled person who is aware of the hazard involved. When the apparatus is connected to a power source, terminals may be live, and the opening of covers or removal of parts is likely to expose live parts. The apparatus shall be disconnected from all voltage sources before it is opened for any adjustment, maintenance, or repair. Note that capacitors inside the apparatus may still be charged even if the apparatus has been disconnected from all voltage sources. Service personnel are thus advised to wait several minutes after unplugging the instrument before assuming that all capacitors are discharged. If any fuses are replaced, be sure to replace them with fuses of the same current and voltage rating and of the same type. The use of makeshift fuses and the short-circuiting of fuse holders are prohibited.

5.2 INTRODUCTION

This section contains procedures for aligning the Model 162 Mainframe, the Models 163 and 164 Processor Modules, and the various options. Even though this instrumentation is conservatively designed with only the highest quality components used throughout, alignment may be advisable after a long period of heavy use to be assured of continued high confidence in measurement data obtained with the system. Also, should a malfunction occur that requires instrument repair, alignment after the repair is advised.

Any of the principal components (Mainframe, M163, M164) can be independently aligned. However, to align the Processor Modules, it is necessary that one first have a properly functioning M162 Mainframe. The Mainframe is aligned without the Processor Modules. In aligning a given system component, it is suggested that the adjustments be made only in the indicated sequence, and that any decision to make a partial alignment be reserved to someone having sufficient knowledge of the circuitry to fully understand all possible interactions.

Note that the procedures that follow are not intended to be used for troubleshooting. If the instrument is suspected of malfunctioning, go directly to Section VI, which gives procedures for isolating faulty circuits. Each system component must be troublefree before it can be aligned.

5.3 REQUIRED EQUIPMENT

(1) Oscilloscope having dual-channel and sampling capabilities in addition to single-channel real time operation—TEKTRONIX 7000 series Mainframe with appropriate plug-in modules.

(2) Sine wave oscillator having accurate amplitude and frequency output—KROHN-HITE Model 4022.

(3) Sine wave oscillator to provide 1 V rms sine waves over range of 1 MHz to 12 MHz—TEKTRONIX Model 191.

(4) General-purpose Digital Voltmeter—FAIRCHILD Model 7000A.

(5) Precision Voltage Source (10 V ± 1 mV, either polarity).

(6) Fast, clean, square-wave source—E. H. Model G710.

(7) Accurate ac voltmeter—HP Model 400 EL.

(8) General-purpose counter with start/stop capabilities—HP 5325B.

(9) High-speed Pulse Generator—GR 1394-A.

(10) AC Voltmeter—HP 400D.

(11) Ohmmeter—SIMPSON 260.

(12) Extender Cable(s) that allow Processor Modules to be operated outside the Mainframe. Note that two cables are required for the M163—EG&G PARC #6020-0093 (required for both M163 and M164); EG&G PARC #6020-0098 (required for M163 only).

(13) Sampling Head Extender board (required only if M163 is to be aligned)—EG&G PARC #1710-0017.

5.4 MAINFRAME (M162) ALIGNMENT

5.4A PRELIMINARY STEPS

(1) Remove the top cover (secured by two screws on the underside of the rear "overhand").

(2) Note that there are two parallel circuit boards, one above the other. The upper board, which is secured by four screws, is hinged on the left side (front view) so that it can be lifted up out of the way to give access to the lower board. Remove the four screws that secure the upper board. Then rotate it upwards as far as it will go and tie it in that position with some string. **NOTE:** If the unit is equipped with a digital storage option, the Digital Storage board, secured by six screws and a cable, must be removed first.

(3) Check the position of the rear-panel Line Voltage Selector. Be sure it is set to the nominal line voltage. Then plug in the line cord, turn on the M162 power, and allow a 15 minute warmup.

(4) Set the M162 controls as follows.

Aperture Delay Controls
% Initial A: 10%
% Initial B: 10%
Range: 10 mSEC
Trigger Level: midrange
Aperture Duration: 50 μSEC and CAL
Scan Time: 10 SEC and CAL
Function: A
Time Constant: .1 mSEC and CAL
Trigger Mode pushbuttons: EXT depressed; all others released
Scan Select: A depressed; all others released
Power: ON (from step 3)

5.4B POWER SUPPLY CHECKS AND ADJUSTMENTS (Refer to Figures V-1 and V-2 for location of indicated points)

(1) + 15 V ADJ (R216A, upper board): Connect the digital voltmeter (hereafter referred to as DVM) to the positive end of capacitor C265. **NOTE:** All upper-board components have "200" series numbers. Lower-board components have "100" series numbers. Then adjust R216A (+ 15 V ADJ) for a DVM indication of + 15.00 V.

(2) − 15 V ADJ (R212A, upper board): Connect the DVM to the negative end of capacitor C266. Then adjust R212A (− 15 V ADJ) for a DVM indication of − 15.00 V.

(3) 5 V and 50 V Checks (upper board)

(a) Connect the DVM to the positive end of capacitor C262. The voltage should be + 50 V ± 2 V.

(b) Connect the DVM to the negative end of capacitor C258. The indicated voltage should be − 50 V ± 2 V.

(c) Connect the DVM to the positive end of capacitor C255. The indicated voltage should be + 5 V ± 0.2 V.

(d) Connect the DVM to the positive end of capacitor C110A (lower board). The indicated voltage should be + 5 V ± 0.2 V. Remove the DVM.

5.4C TRIGGER CIRCUIT ADJUSTMENTS

(1) Frequency Response (C115A and C121A; lower board)

(a) Verify that the EXT trigger pushbutton is depressed and that the SLOPE pushbutton is released.

(b) Remove the wire that attaches to quick-disconnect terminal P138 on the lower board. Tape the terminal at the end of the wire so that it won't accidentally short against some other component.

(c) Set up the controls of the square wave generator to provide a 200 mV (zero-to-peak) square wave at 500 kHz. Connect the square wave to the Trigger INPUT connector of the Model 162. Use a BNC "Tee" at the INPUT connector and terminate the applied square wave in 50 Ω.

(d) Be sure the compensation on the oscilloscope probe is properly adjusted. Then monitor the signal at TP108A. **NOTE:** The test points are small terminals identified by "foil" lettering on the boards, and by callouts in Figures V-1 and V-2.

(e) Adjust the M162 TRIGGER LEVEL control until the display is centered between the clipped limits. Then adjust trim-capacitors C121A and C115A for the best observed square wave response (flat top with minimum overshoot).

(2) Trigger Symmetry (R153A; lower board)

(a) Connect the DVM to the wiper of the TRIGGER LEVEL control. Then adjust the control for a DVM indication of 0.00 V. Remove the DVM.

(b) Set the controls of the sine wave generator to provide a 1 V pk-pk 1 kHz sine wave. Connect this signal to the Trigger INPUT connector and to the vertical input of the oscilloscope.

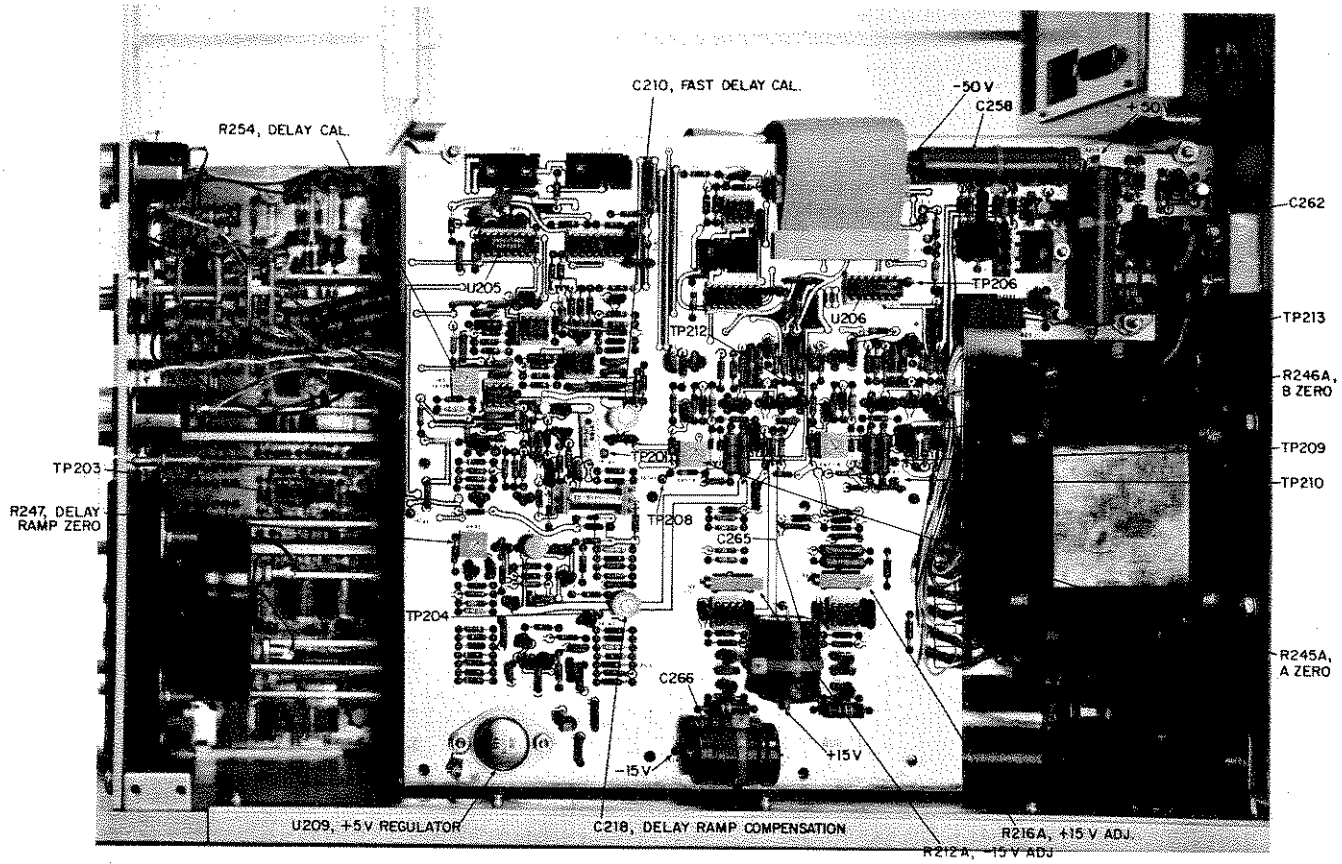


Figure V-1. LOCATION OF MODEL 162 UPPER BOARD ADJUSTMENTS AND TEST POINTS

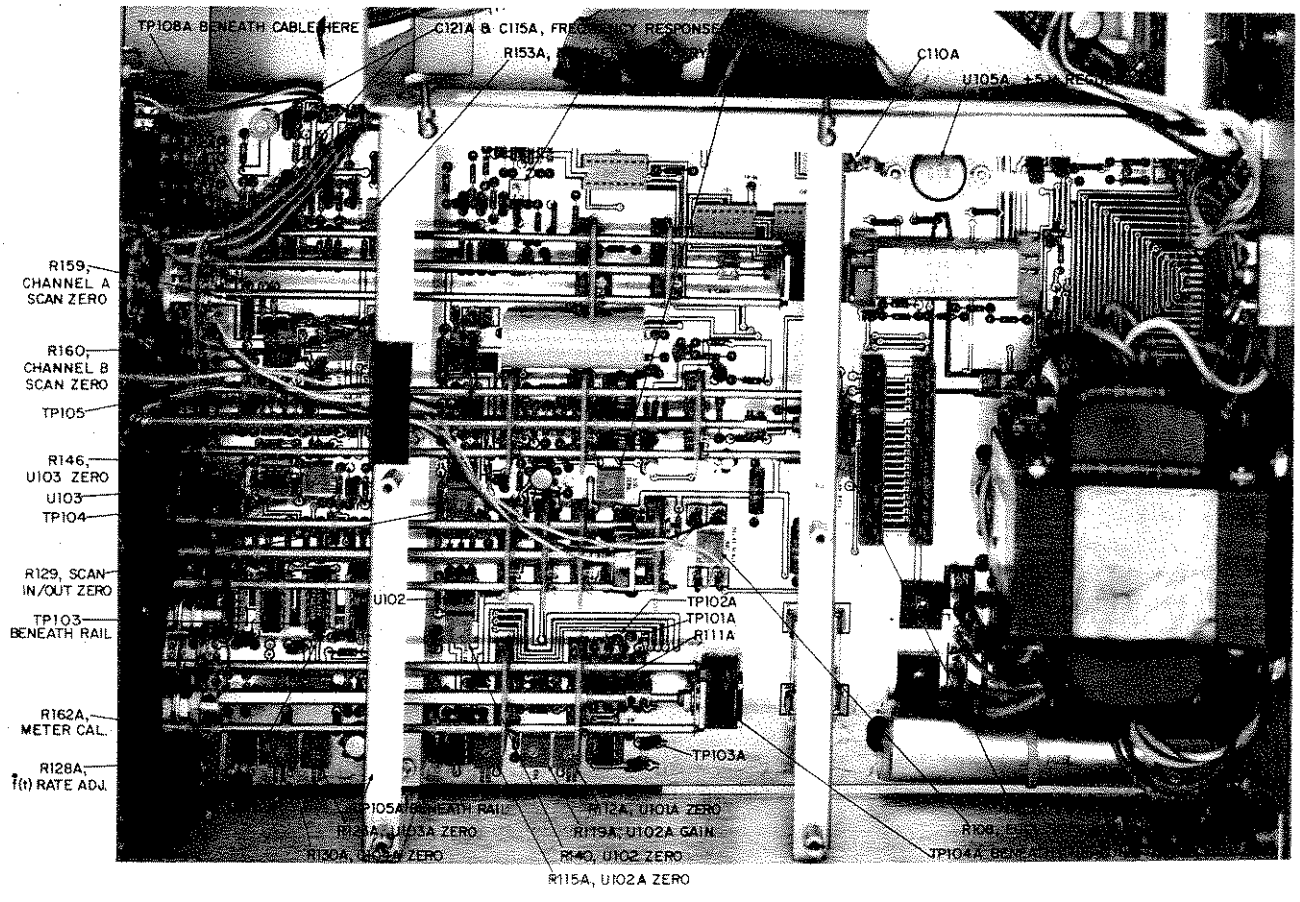


Figure V-2. LOCATION OF MODEL 162 LOWER BOARD ADJUSTMENTS AND TEST POINTS

(c) Trigger the oscilloscope externally from the negative edge of the signal at quick-disconnect terminal P138. P138 is the board connector. Do not attempt to trigger the scope from the signal or the end of the wire (removed in earlier step) that normally connects to P138. In some instances it might be necessary to adjust R153A (TRIGGER SYMMETRY) to get a trigger signal at P138. Then monitor the input signal with the oscilloscope. Carefully set the display baseline on the center of the display graticule (scope coupling to GND). Then, with the scope dc coupled, display the sine wave signal.

(d) Vary the setting of R153 A (TRIGGER SYMMETRY) and note that it determines the vertical separation between the start of the displayed sine wave and the center line (ground) of the graticule. Note also that as the Model 162 SLOPE pushbutton is alternately pressed and released, the vertical offset of the signal start shifts with respect to the ground reference. The objective is to find that setting of R153A for which the signal start offset magnitude is the same, but the polarity opposite, as the SLOPE pushbutton is alternately pressed and released.

Remove the line carrying the external triggering signal from P138 to the oscilloscope and change the oscilloscope over to internal triggering.

(3) Clipping Level Checks

(a) Set the amplitude of the sine wave generator output to 100 mV pk-pk (frequency to remain at 1 kHz). Then transfer the oscilloscope from the signal generator to TP108A. The observed signal should be a sine wave with an amplitude of 200 mV pk-pk. **NOTE:** In some instances, it may be necessary to adjust the front-panel TRIGGER LEVEL control to obtain this signal.

(b) Increase the amplitude of the input signal to 3 V pk-pk. Clipping should be observed with a pk-pk amplitude of nominally 1 V. The peaks, though clipped, will be somewhat rounded. Remove the scope from TP108A.

(4) Line Trigger Checks

(a) Press in the LINE Trigger pushbutton. Then monitor the signal at Quick Disconnect Terminal P138 with the oscilloscope. The observed signal should be a 60 Hz (50 Hz where the power frequency is 50 Hz) square wave with an amplitude of 3 V pk-pk.

(b) Reverse the position of the SLOPE pushbutton. The waveform should remain unchanged. **NOTE:** If the oscilloscope were synchronized from the line, one would observe a 180° phase shift with the change in selected slope.

(5) Trigger Risetime Check

(a) Remove the sine wave generator from the Trigger INPUT. Connect in its place the square wave generator, terminated in 50 Ω. Set the generator controls to provide a 1 V zero-to-peak square wave at 1 MHz. Depress the EXT Trigger pushbutton.

(b) Set up the oscilloscope for sampling operation. Then monitor the signal at quick-disconnect terminal P138. Measure the 10% to 90% risetime of the negative transition. It should be in the range of 2 ns to 4 ns.

(c) Remove the generator. Then reconnect to quick-disconnect terminal P138 the wire that was disconnected earlier.

5.4D SIGNAL PROCESSING CIRCUIT ADJUSTMENTS

(1) U101A Zero (R112A; lower board)

(a) Verify that the Function switch is set to "A", and that the Time Constant is set to .1 mSEC and CAL.

(b) Connect a short clip lead from TP101A to that end of R111A that is closest to TP101A.

(c) Connect the DVM to TP103A. Then adjust R112A (U101A ZERO) for a DVM indication of 0.00 V. Remove the clip lead installed in the previous step.

(2) U102A Zero (R115A; lower board)

(a) Connect a clip lead from TP106A to the end of R111A nearest TP101A.

(b) Connect a second clip lead from TP103A to the same end of R111A.

(c) Connect the DVM to TP104A. Then adjust R115A (U102A ZERO) for a DVM indication of 0.00 V. Remove the two clip leads and the DVM.

(3) U103A ZERO (R123A; lower board)

(a) Connect a clip lead from TP104A to the end of R111A nearest TP101A.

(b) Connect a second clip lead from TP105A to TP106A.

(c) Monitor the front-panel f(t) OUTPUT connector with the DVM. Then adjust R123A (U103A ZERO) for a DVM indication of 0.00 V.

(d) Remove the clip lead interconnecting TP105A and TP106. Do not disturb the other clip lead.

(4) U104A ZERO (R130A; lower board)

(a) Rotate R128A (RATE) fully clockwise.

(b) Transfer the DVM to the front-panel $\dot{f}(t)$ OUTPUT connector. Then adjust R130A (U104A ZERO) for a DVM indication of 0.00 V.

(c) Remove the clip lead interconnecting TP104A and R111A.

(5) U102A Gain (R119A; lower board)

(a) Set the controls of the precision dc source to supply – 10.00 V. Then connect the – 10.00 V level to TP101A.

(b) Transfer the DVM back to the f(t) OUTPUT connector. Then adjust R119A (U102A GAIN) for a DVM indication of + 10.00 V.

(6) Meter Cal. (R162A; lower board)

(a) In units having mechanical meters, connect a jumper across the meter terminals. Then check, and, if necessary, adjust the mechanical zero. Remove the jumper.

(b) The DVM should still be connected to the f(t) OUTPUT connector and – 10.00 V should still be applied to TP101A. The next step is to adjust R162A (METER CAL) for exactly full-scale panel meter indication.

(7) Differential Zero Check

(a) Set the FUNCTION switch to A – B. Then, with – 10.00 V still applied to TP101A, connect a jumper from TP101A to TP102A.

(b) Note the DVM indication (monitoring f(t) OUTPUT connector). The indication should be no more than 20 mV, either polarity.

(c) Remove the 10 V source and the DVM. Set the FUNCTION switch to "A".

(8) Time Constant Checks

(a) Set the sine wave generator controls to provide a 10 kHz sine wave with an amplitude of 6.3 V rms. Apply this signal to TP101A.

(b) Measure the signal at the front panel f(t) connector with the ac voltmeter. Check to be sure the M162 Time Constant is set to 0.1 mSEC and CAL. The ac voltmeter indication should be 1 V ± .15 V rms.

(c) Rotate the inner knob of the Time Constant control to the × 10 position. The ac voltmeter indication should decrease to 100 mV ± 15 mV rms.

(d) Return the Time Constant inner knob to CAL and set the outer knob to 1 mSEC. The ac voltmeter indication should be 100 mV ± 25 mV rms.

(e) Set the Time Constant to 10 mSEC and CAL. The ac voltmeter indication should decrease to 10 mV ± 2.0 mV rms.

(f) Decrease the frequency of the applied signal to 10 Hz. Then set the Time Constant to .1 SEC and CAL. The ac voltmeter indication should increase to 1 V ± .20 V rms.

(g) Set the Time Constant to 1 SEC and CAL. The ac voltmeter indication should decrease to 100 mV ± 20 mV rms.

(h) Set the Time Constant to 10 SEC and CAL. The ac voltmeter indication could decrease to 10 mV ± 2.0 mV rms.

(9) $\dot{f}(t)$ Rate Adj. (R128A; lower board)

(a) Set the Time Constant to .1 mSEC and CAL. Then increase the frequency of the applied signal to 1 kHz and adjust the amplitude of the applied signal as required to obtain an ac voltmeter indication of 1 V rms.

(b) Rotate the inner knob of the Time Constant control clockwise as required to obtain an ac voltmeter indication of 0.707 V rms.

(c) Transfer the ac voltmeter to the $\dot{f}(t)$ OUTPUT connector and adjust R128A ($\dot{f}(t)$ RATE ADJ) for an ac voltmeter indication of 0.707 V rms.

(d) Remove the sine wave source and voltmeter.

5.4E SCAN RAMP ADJUSTMENTS

(1) Set the front-panel controls as follows.

% Initial A and % Initial B: fully counterclockwise
Scan Time: .01 SEC and CAL
Scan Select pushbuttons: EXT and HOLD depressed; all others released

(2) CHANNEL A SCAN ZERO; U105 ZERO (R159; lower board)

(a) Connect the DVM to the rear-panel CHAN A SCAN BNC connector.

(b) Adjust R159 (CHANNEL A SCAN ZERO) for a DVM indication of 0.00 V.

(3) CHANNEL B SCAN ZERO: U106 ZERO (R160; lower board)

(a) Connect the DVM to the rear-panel CHAN B SCAN BNC connector.

(b) Adjust R160 (CHANNEL B SCAN ZERO) for a DVM indication of 0.00 V.

(4) FULL-SCALE DELAY ADJUST; DELAY SCAN ADJ (R108; lower board)

(a) Rotate the % INITIAL A and % INITIAL B dials ten full turns (setting of 10.00).

(b) Transfer the DVM back to the CHAN A SCAN connector. Then adjust R108 (FULL-SCALE DELAY ADJ) for a DVM indication of +5.000 V.

(c) Transfer the DVM to the CHAN B SCAN connector. The voltage indication should be +5 V ±20 mV.

(5) SCAN IN/OUT ZERO; U104 ZERO (R129; lower board)

(a) Rotate the % INITIAL A and % INITIAL B dials fully counterclockwise.

(b) Ground the SCAN IN/OUT connector (rear panel).

(c) Transfer the DVM to TP105. Then adjust R129 (SCAN IN/OUT ZERO) for a DVM indication of 0.00 V.

(6) SCAN ZERO (R132; lower board)

(a) Remove the short from the SCAN IN/OUT connector and release the SCAN EXT pushbutton.

(b) Hold in the SCAN RESET pushbutton, and, while it is held in, adjust R132 for a DVM indication of 0.00 V (DVM should still be connected to TP105). Release the pushbutton when the adjustment is completed.

(7) U103 ZERO (R146; lower board)

(a) At Integrated Circuit U103, short together pins 2 and 3. **NOTE:** This is probably most easily done by connecting a clip lead to resistors that return to pins 2 and 3. Two suitable resistors are R155 and R142. Facing the unit from the front, a clip lead can be connected from the front-most end of R155 to the front-most end of R142.

(b) Transfer the DVM to TP 104. Then hold down the SCAN RESET pushbutton and, while the pushbutton is held down, adjust R146 (U103 ZERO) to the "switch point" of the voltage at TP104. The voltage at TP104 will be either "high" or "low". The purpose of the adjustment is to set R146 to where the voltage just switches from "high" (nominally +7 V) to "low" (nominally −0.3 V).

(c) Release the SCAN RESET pushbutton and remove the clip lead connected in step a.

(8) U102 ZERO (R140; lower board)

(a) Connect together pins 2 and 3 of IC U102. **NOTE:** As in the previous step, this is most easily done by connecting a clip lead between specific resistors, in this case R137 and R139. Facing the unit from the front, connect a clip lead from the right-hand end of R137 to the right-hand end of R139.

(b) Transfer the DVM to TP103. Then hold down the SCAN RESET pushbutton and, while the pushbutton is depressed, adjust R140 to where the transition from "high" (nominally +6 V) to "low" (nominally −1 V) occurs.

(c) Release the SCAN RESET pushbutton. Also, remove the clip lead and DVM.

(9) SCAN RATE TRIM (R117; lower board)

(a) Release the SCAN HOLD pushbutton and press the SCAN A pushbutton. Then check that the SCAN TIME is set to .01 SEC and CAL.

(b) Monitor the signal at TP105 with the oscilloscope. Then adjust R117 (SCAN

RATE TRIM) so that the ramping rate of the observed repetitive ramps is 1 V/ms.

(c) Set the center knob of the SCAN TIME control to ×10. The observed ramping rate should slow to 0.1 V/ms ± 15%. Note the baseline and peak levels. The ramp should start at 0 V ± 30 mV and the peaks should fall in the range of −10.5 V to −11.0 V. **NOTE:** It is difficult to check the level from which each ramp starts because the oscilloscope sensitivity must be increased to where scope overload and resultant zero-shift error occurs. This problem can be avoided by connecting a network as shown in Figure V-3 between TP105 and the scope input. With the network installed, the scope sensitivity can be increased to where the 0 V ±30 mV ramp-start potential can be checked. The network should not be "in" when checking the peak amplitude levels.

(d) Reset the center knob of the SCAN TIME control to the CAL position.

(10) Scan Time Checks

(a) Set the outer knob of the SCAN TIME control to .1 SEC.

(b) Note the ramping rate at TP105. It should be 0.1 V/ms ± 10%.

(c) Set the SCAN TIME to 1 SEC and CAL.

(d) Note the ramping rate at TP105. It should be 10 mV/ms ± 10%.

(e) Remove the oscilloscope from TP105 and connect the DVM to the rear-panel CHANNEL A SCAN connector. Then depress the SCAN A pushbutton.

(f) Set the SCAN TIME to 10 SEC and CAL. Hold down the SCAN RESET pushbutton. At some convenient time, release the SCAN RESET pushbutton. After ten seconds, depress the SCAN HOLD pushbutton and note the DVM indication. It should be +5 V ± 0.5 V. Release the SCAN HOLD pushbutton.

(g) Set the SCAN TIME to 100 SEC and CAL. Hold down the SCAN RESET pushbutton. At some convenient time, release the SCAN RESET pushbutton. One hundred seconds later depress the SCAN HOLD pushbutton and note the DVM indication. It should be +5 V ±0.5 V. Release the SCAN HOLD pushbutton.

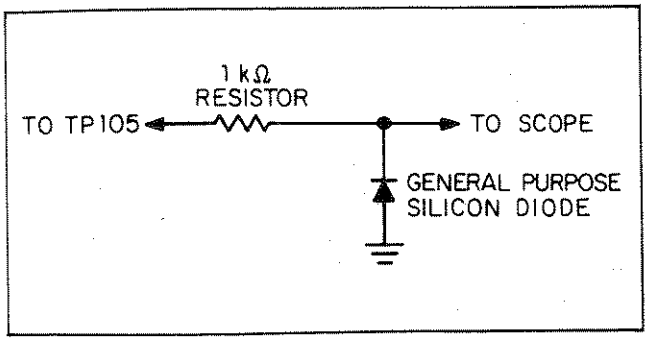


Figure V-3. START-POTENTIAL NETWORK

(h) Set the SCAN TIME to 1k SEC and CAL. Hold down the SCAN RESET pushbutton. At some convenient time, release the SCAN RESET pushbutton. One hundred seconds later depress the SCAN HOLD pushbutton and note the DVM indication. It should be 0.5 V ±50 mV. Release the SCAN HOLD pushbutton.

(i) Set the SCAN TIME to 10k SEC and CAL. Hold down the SCAN RESET pushbutton. At some convenient time, release the SCAN RESET pushbutton. One hundred seconds later depress the SCAN HOLD pushbutton and note the DVM indication. It should be 50 mV ±5 mV.

(j) Set the SCAN TIME back to 10 SEC and CAL. Also, release the HOLD pushbutton and remove the DVM.

(11) Blanking Output Checks

(a) Depress both the SCAN A and SCAN B pushbuttons. Also, depress the SINGLE pushbutton.

(b) Press in the SCAN RESET pushbutton and, while it is depressed, use the DVM to measure the voltage at pin 14 of rear-panel connector P101 and also at pin 13 of the same connector. The voltage at pin 14 should be nominally 0 V. That at pin 13 should be nominally +50 V. At a convenient time, release the RESET pushbutton, the voltage states at the two connector pins will reverse for 10 seconds, i.e., for the duration of the scan (ten seconds), pin 14 will go to +50 V and pin 13 will go to zero. At the end of the scan, the voltages will reverse back to their initial state. Remove the DVM.

(12) Penlift Relay Checks

(a) Set the SCAN TIME to .01 SEC and CAL. The SINGLE pushbutton should be depressed.

(b) Connect the ohmmeter between pins 18 and 16 of rear-panel connector P101. The ohmmeter should indicate an open circuit.

(c) Depress the SCAN RESET pushbutton. As long as this pushbutton is held down, the ohmmeter should indicate a short between pins 18 and 16.

(d) Set the SCAN TIME to 10 SEC and CAL. Then hold down the RESET pushbutton. The resistance indication will be zero ohms. At some convenient time, release the SCAN RESET pushbutton. The zero indication will last another ten seconds (scan in progress). At the end of that time, the ohmmeter will indicate an open circuit.

(e) Remove the ohmmeter.

5.4F APERTURE DELAY RANGE ADJUSTMENTS

(1) Set the controls as follows.

% Initial A: fully counterclockwise
% Initial B: fully counterclockwise
Aperture Delay Range: 1 mSEC
Scan pushbuttons: A and B depressed; all others released
Scan Time: 0.1 SEC and CAL
Trigger Mode pushbuttons: EXT depressed; all others released

(2) DELAY CAL (R204; upper board)

(a) Connect a 1 V pk-pk square wave at 500 Hz to the Trigger INPUT connector. Then adjust the Trigger Level control as required for proper triggering as indicated by the TRIGGERED lamp.

(b) Monitor TP204 with the oscilloscope. The observed signal should be a negative ramp with an amplitude of nominally −6 V.

(c) Adjust R204 (DELAY CAL) for an observed ramping rate of 5 V/ms.

(3) FAST DELAY CAL (C210; upper board)

(a) Change the selected Aperture Delay Range to 1 μSEC.

(b) Adjust trim-capacitor C210 (FAST DELAY CAL) for an observed ramping rate of 5 V/μSEC.

(4) DELAY RAMP COMPENSATION (C218; upper board)

(a) Set the Aperture Delay Range to 100 nSEC and increase the trigger frequency to 100 kHz.

(b) Set up the oscilloscope for sampling operation. Then monitor the signal at TP204.

(c) Adjust trim-capacitor C218 (RAMP COMPENSATION) for minimum ringing in the observed ramp with minimum rounding at the beginning and end of the ramp. Restore the oscilloscope to non-sampling operation.

(5) DELAY RAMP ZERO (R247; upper board)

(a) Construct a network from a 1 kΩ resistor and an ordinary silicon diode (IN482B) connected in series, with the cathode of the diode connected to the resistor. Connect the free end of the resistor to TP204 and the free end of the diode to ground.

(b) Reduce the frequency of the input trigger square wave to 100 Hz. Then set the oscilloscope sensitivity to 10 mV/cm and monitor the signal at the junction of the resistor and diode.

(c) Carefully establish ground on the display. Then alternate the inner knob of the dual-concentric Aperture Delay Range control between mSEC and μSEC. The offset from ground of the ramp reset level will be observed to be different for the two positions of the knob.

(d) Adjust R247 (DELAY RAMP ZERO) so that the two levels of offset are equal and of opposite polarity with respect to ground.

(e) Remove the network from TP204.

(6) % Initial Delay Checks

(a) Connect the oscilloscope to TP208. With the % INITIAL A dial fully counterclockwise, the observed waveform should be a positive 0-to-6 V (nominal) ramp having a slope of 5 V/100 ms.

(b) Increase the % INITIAL A dial setting to 2.00. The reset level of the ramp will shift upwards to 1 V. The peak should still be

the same potential as in the preceding step. In effect, the ramp is shortened but the slope remains constant.

(c) Successively set the % INITIAL A dial to 4.00, 6.00, 8.00, and 10.00, observing that the ramp reset level rises proportionally to the dial setting with the corresponding reset levels being 2 V, 3 V, 4 V, and 5 V. Then return the % INITIAL A dial to the fully counterclockwise position.

(d) Transfer the oscilloscope probe to TP209 and check the reset level of the observed ramp as a function of the % INITIAL B dial setting. The checks are performed in the same manner as for the % INITIAL A checks just completed. When finished, set the % INITIAL B dial to the fully counterclockwise position and remove the scope probe.

(7) Internal Trigger Checks

(a) Remove the square wave trigger from the Trigger INPUT connector and then press in the INT Trigger pushbutton.

(b) Set the Aperture Delay Range to 0.1 μSEC. Then connect the oscilloscope to TP204.

(c) Leaving the inner knob of the Aperture Delay Range switch set to μSEC, rotate the outer knob through all positions except SPEC. Repetitive ramps should be observed for each position. The reset time for all positions should be nominally 100 ns.

(d) Set the inner knob of the Aperture Delay Range switch to mSEC. Then rotate the outer knob through all positions except SPEC. Repetitive ramps will be observed for all positions. The reset time for all positions will be nominally 100 μs.

(e) Transfer the oscilloscope to pin 11 of integrated circuit U205. The observed signal should be a logic 0 pulse at the delay-ramp repetition rate and having a width in the range of 100 μs to 300 μs.

(f) Continuing to monitor pin 11 of U205, set the inner knob of the Aperture Delay Range switch to μSEC. If the observed signal should disappear (internal triggering stops), alternately release and depress the INT trigger pushbutton to reestablish internal triggering. The duration of the observed pulse should decrease to where it is in the range of 180 ns to 250 ns. Remove the oscilloscope probe.

(8) High Trigger Rate Holdoff Checks

(a) Connect a 1 V pk-pk 1 MHz sine wave source to the Trigger INPUT connector and select EXT triggering. If necessary, adjust the TRIGGER LEVEL control to establish external triggering.

(b) Set the Aperture Delay Range to .1 μSEC. Then monitor TP204 with the oscilloscope and adjust the Trigger Level control for proper M162 triggering as indicated by the TRIGGERED lamp and by the observed ramps.

(c) Begin increasing the frequency of the input sine wave. The interval between successive ramps will become shorter and shorter, tracking the increasing trigger frequency. However, a point will be reached where the interval between ramps reaches a minimum, and further increases in the input trigger frequency will not alter the ramp spacing. Check this feature up to a trigger frequency of 12 MHz. No "broken" or "partial" ramps should be observed if the HIGH TRIGGER RATE HOLDOFF circuits are functioning normally.

(d) Remove the trigger source and disconnect the scope probe from TP204.

(9) A & B Zero Adjustments (R245A & R246A; upper board)

(a) Set the Aperture Delay Range to 10 μSEC. Then set the % INITIAL A and % INITIAL B dials to 1.00 (one turn from fully counterclockwise position). Select EXT scan and INT triggering with the appropriate pushbuttons.

(b) Monitor TP203 with the oscilloscope and internally trigger the scope from the positive going edge of the observed waveform. Then monitor the signal at TP212 (scope must have dual channel capabilities).

(c) Adjust R245A (A ZERO) so that the negative going edge at TP212 occurs exactly one microsecond after the positive going edge at TP203.

(d) Transfer the scope probe connected to TP212 to TP213. Then adjust R246A (B ZERO) until the negative going slope at TP213 is coincident with the negative going slope at TP212. **NOTE:** Some transferring back and forth between TP212 and TP213 may be required.

(10) Aperture Delay Range Final Calibration (R254, C210, R245A, & R246A; upper board)

(a) Make preparations for incorporating the counter into the test setup. The twisted-pair cables will be required. One will extend from TP203 to the counter START input. The other will extend from TP212 to the STOP input. A 100 Ω resistor should be connected in series with the signal lead of each cable, the resistor to be installed at the signal (test point) end. The other lead of each cable simply interconnects the grounds.

(b) Set the % INITIAL A dial to 1.00 and the Aperture Delay Range to 10 mSEC. The Model 162 should still be operating in the INT Trigger mode.

(c) Note and *record* the counter reading. Then change the % INITIAL A setting to 9.00. Note and *record* the new counter reading.

(d) Alternate between % INITIAL A dial settings of 1.00 and 9.00, adjusting R254 after each set of readings, until the difference between the two counter indications is exactly 8.00 ms ± 5 μs.

(e) Set the % INITIAL A dial to 1.00 and adjust R245A for a counter indication of exactly 1.00 ms ± 5 μs.

(f) Set the % INITIAL A dial to 10.00 and note the counter indication as the Aperture Delay Ramp is rotated through the following positions.

Aperture Delay Range	Counter Reading
.1 mSEC	100 μs ± 4 μs
.2 mSEC	200 μs ± 8 μs
.5 mSEC	500 μs ± 20 μs
1 mSEC	1 ms ± 40 μs
2 mSEC	2 ms ± 80 μs
5 mSEC	5 ms ± 200 μs
10 mSEC	10 mSEC (calibrated position)
20 mSEC	20 ms ± 800 μs
50 mSEC	50 ms ± 1 ms

(g) Set the % INITIAL A dial to 9.00 and the Aperture Delay Range to 10 μSEC. Then adjust trim-capacitor C210 for a counter indication of 9.00 μs. Remove the counter.

(h) Set the Aperture Delay Range to .1 μSEC and monitor TP204 with the oscilloscope. Set the % INITIAL A and % INITIAL B dials to 10%. A negative ramp should be observed with a slope of − 5 V/100 ns. The tolerance is + 15 ns, − 0 ns.

(i) Set the Aperture Delay Range to 10 μSEC. Then trigger the oscilloscope from the positive trigger pulse at pin 10 of U206 and display the pulse. The observed signal should be a positive 10 ns "spike" with an amplitude of nominally + 1.5 V (upper frequency limit of scope may limit observed amplitude). While triggering from pin 10, monitor the signal at pin 4 of U206 as well. The observed pulse should be similar to that at pin 10. Adjust R246A as required to bring the signal at pin 4 (also available at TP206) into exact coincidence with that at pin 10. Remove the oscilloscope probes from the monitored points.

This completes the M162 alignment. Remove all cables before proceeding to the M163 alignment. Return the upper board to its proper position. Return the digital storage board to unit where appropriate.

5.5 MODEL 163 ALIGNMENT

5.5A PRELIMINARY STEPS

(1) With the mainframe power off, plug the two Extension Cable Assemblies (#6020-0093 & 6020-0098) into slot "A" of the mainframe. Then plug the M163 into the free ends of the cable assemblies. Note that the two circuit boards of the Model 163 are mounted on rails extending from the front to the rear panels. The larger of the two boards is the Signal board and the smaller is the Logic board. For convenience in doing the following alignment, the screws securing the upper Logic board rail should be removed from the panel and the screws that secure the lower Logic board rail should be loosened. When this is done, the Logic board can be rotated 90° so that it rests on the bench. If the lower rail screws are then tightened, the Logic board will help to stabilize the M163. Take the Sampling Head Extender Card (#1710-0017) supplied with the Model 163 and modify it as follows. Connect a jumper from pin 3 to pin D. Connect another jumper from pin D to pin F. Then take a short stiff wire (a resistor lead will do nicely) and solder one end of it to pin 4. Leave the other end free. It will be used as an input in later steps. When the modifications are complete, plug the extender into the Model 163. The Sampling Head is not installed until a later step. Before proceeding, take care that there are no test-equipment connections "left over" from the preceding mainframe alignment. **NOTE:** When the Model 163 alignment is complete, be sure to remove the modifications made on the extender card.

(2) Turn on the mainframe power and allow a fifteen minute warmup.

(3) Set the mainframe controls as follows.

Aperture Delay Range: 1 μSEC
% Initial A: 1.00
Aperture Duration: setting immaterial
Scan Time: outer knob to .01 SEC; inner to CAL
Scan Select pushbuttons: A depressed; all others released
Trigger Mode pushbuttons: EXT depressed; others released
Function: A
Time Constant: .1 mSEC; CAL

(4) Set the M163 controls as follows.

Sensitivity: 100 mV
Samples Averaged: 10
Zero: do not disturb
Baseline Sample Delay: fully counterclockwise

5.5B SUPPLY LEVEL CHECKS

Note the connector which interfaces to the Sampling Head when it is installed. There are two sets of contacts. Facing the connector from the rear, the left-hand set, reading from top to bottom, extends from A to F. The right-hand set extends from 1 to 6. Most of the following voltage checks are made at this connector.

(1) Connect the DVM to pin A of the Sampling Head Interface connector. The voltage should be −12.5 V ±0.2 V.

(2) Transfer the DVM to pin E. The voltage should be +50 V ±2 V.

(3) Transfer the DVM to pin 1. The voltage should be +15 V ±20 mV.

(4) Transfer the DVM to pin 5. The voltage should be −50 V ±2 V.

(5) Connect the DVM to the positive end of capacitor C3225 on the M163 Logic board (small board). The voltage should be +5 V ±0.2 V.

(6) Remove the DVM.

5.5C AMPLIFIERS 1 AND 2 GAIN CHECKS AND ZERO ADJUSTMENT

(1) Amplifier 1 Gain Checks

(a) Connect the signal generator ground to the Model 163 Sampling-Head connector plate. Then connect the signal generator output to the short wire connected earlier to pin 4 of the Sampling-Head Extender Card. Adjust the signal generator controls to provide an 8 mV rms 10 kHz sine wave when loaded with 460 Ω. Connect the ac voltmeter ground to the Model 163 Signal board ground plane. (The Signal board is the board that is *not* rotated downwards.)

(b) Monitor the signal at TP2 with the ac voltmeter. The indicated signal level should be 100 mV ±5 mV rms. **NOTE:** Be sure the M163 Sensitivity switch is set to 100 mV.

(c) Adjust the applied signal level as required to obtain exactly 100 mV at TP2. Then set the M163 Sensitivity switch to 250 mV. The output should decrease to 40 mV ±2 mV.

(d) Set the M163 Sensitivity switch to 1 V. The output should decrease to 10 mV ±1 mV.

(2) AMPLIFIER 2 ZERO ADJUSTMENT (R3028; Signal board)

(a) Remove the ac voltmeter from TP2 and connect a clip lead from TP2 to ground.

(b) Connect the DVM to TP3. Then adjust R3028 (AMPLIFIER 2 ZERO) for a DVM indication of 0.000 V. Remove the DVM. Also, remove the clip lead grounding TP2 and set the M163 sensitivity to 100 mV.

(c) Monitor the signal at TP3 with the ac voltmeter. The indicated signal level should be 2500 mV ±125 mV rms.

(d) Remove the signal generator and the ac voltmeter.

5.5D SIGNAL AND BASELINE INTEGRATORS

(1) ZERO (R3049 and R3177; Signal board)

(a) Connect the DVM to the wiper of R3043 (SIG. HOLDING TIME) and adjust R3043 for a DVM indication of 0.00 V.

(b) Connect the DVM to J3002 and set the front-panel ZERO control for a DVM indication of 0.00 V.

(c) Connect the DVM to the wiper of R3093 (BASELINE HOLDING TIME) and adjust R3093 for a DVM indication of 0.00 V.

(d) Connect the DVM to TP5. Then press CLEAR and adjust R3049 (ZERO) for a DVM indication of 0.00 V.

(e) Connect the DVM to TP8. Then press CLEAR and adjust R3177 (BASELINE ZERO) for a DVM indication of 0.00 V.

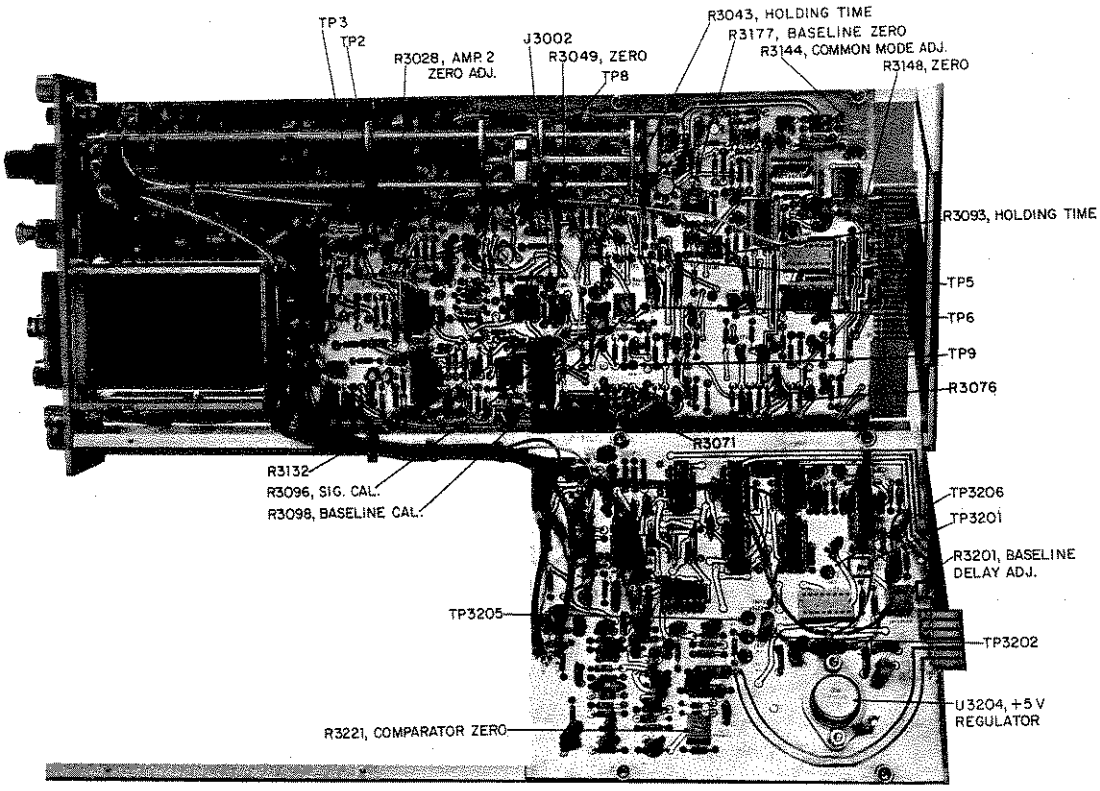


Figure V-4. MODEL 163 ADJUSTMENTS AND TEST POINTS

(b) Connect the DVM to TP5. Then depress the CLEAR pushbutton and, at a convenient time, release it. The TP5 voltage will be observed to begin drifting away from zero. Adjust R3043 (HOLDING TIME) for minimum drift rate. Each time the voltage drifts far enough from zero to make the adjustment difficult, depress CLEAR again to re-establish zero and continue the procedure.

(3) HOLDING TIME (R3093; Signal board)

(a) Transfer the DVM to TP8. Then depress CLEAR and, upon releasing, adjust R3093 (HOLDING TIME) for a minimum dc drift in the voltage at TP8. As in the preceding adjustment, it may be necessary to periodically press and release the CLEAR pushbutton to re-establish zero.

(b) Remove the DVM from TP8.

(4) ZERO (R3148)

(a) Connect the DVM to the front-panel pin jack (J3009).

(b) Then press CLEAR and adjust R3148 (ZERO) for a DVM indication of 0.00 V. Remove the DVM.

5.5E STROBE PULSE CHECKS

(1) Locate the Strobe Output transformer, a small toroidal transformer with three windings located towards the front of the larger board.

(2) Trigger the M162 at 5 kHz.

(3) Monitor the signal at the ungrounded end of the one-turn winding. The signal should appear as shown in Figure V-5.

5.5F OVERLOAD CHECKS

(1) Reduce the M162 Trigger rate to 1 Hz.

(2) Connect an external dc source (adjustable to ± 10 V; high accuracy not required). Then connect the dc source, set initially to some low positive voltage, to TP2.

(3) Monitor the applied voltage with the DVM and begin to increase the voltage gradually. Note the level applied when the OVERLOAD light begins to glow. The applied voltage should be in the range of +8.3 V to +8.8 V.

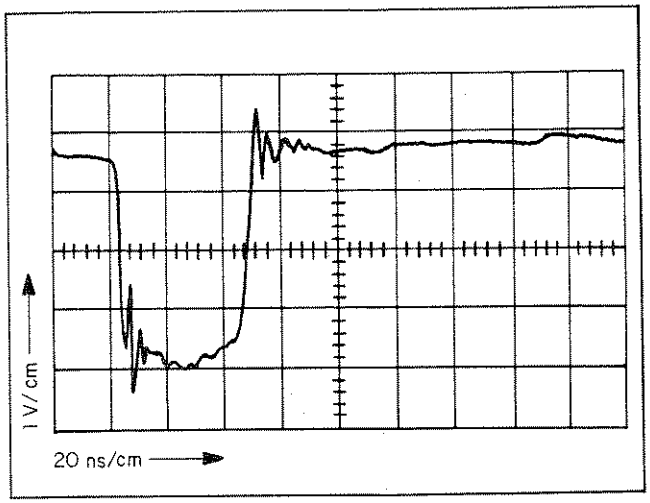


Figure V-5. STROBE PULSE

(4) Reverse the polarity of the applied voltage and again note how much is required to cause an overload indication. This time the voltage should be in the range of −8.3 V to −8.8 V.

(5) Monitor the signal at that end of resistor R3132 that is towards the rear of the board. The observed signal should be a positive pulse appearing at one second intervals and having a duration of between 0.1 and 0.4 seconds.

(6) Remove the oscilloscope and external dc source.

5.5G SIGNAL CHANNEL GATE-LEVEL CHECKS

(1) Increase the M162 trigger rate to 10 kHz.

(2) Rotate the Baseline Sample Delay control about half a turn clockwise.

(3) Monitor the signal at the ungrounded end of resistor R3071. The observed signal should be a 0.5 μs wide negative going pulse. The baseline should be at +4 V and the "peak" should be at −7 V.

(4) Transfer the oscilloscope to the ungrounded end of resistor R3076. The observed signal should be the same as in the preceding step.

(5) Monitor the signal at test points TP6 and TP9 with the oscilloscope. At both points the observed signal should be a symmetrical square wave with a period of nominally 200 μs. The upper level should be at 0 V and the lower at −13 V.

5.5H LOGIC BOARD ADJUSTMENTS

(1) BASELINE DELAY ADJ (R3201; Logic board)

(a) Set the controls as follows.

% Initial A and % Initial B: 5%
Aperture Delay Range: 20 μs
Baseline Sample Delay: fully clockwise
Baseline Int/Ext pushbutton (inner knob of Delay Control): in

(b) Connect the DVM to TP3201. Then adjust R3201 (BASELINE DELAY ADJ) for a DVM indication of +4.50 V.

(2) COMPARATOR ZERO (R3221; Logic board)

(a) Trigger the M162 from a 10 kHz 2 V pk-pk square wave.

(b) Connect the DVM to TP3202. Then adjust the front-panel BASELINE SAMPLE DELAY control for an indicated voltage of +2.25 V. Remove the DVM.

(c) Trigger the oscilloscope from the negative going edge of the signal at TP3206.

(d) With the oscilloscope triggered from the signal at TP3206, monitor the signal at TP3205. Then adjust R3221 (COMPAR. ZERO) such that the negative edge of the signal at TP3205 occurs exactly 10 μs ± 0.2 μs after the negative edge at TP3206.

(3) TRIGGER HOLDOFF CAL (R3258; Logic board)

(a) Transfer the oscilloscope to the lower end of resistor R3241.

(b) Adjust R3258 (TRIGGER HOLDOFF CAL) for an observed logic 0 gate with a duration of 90 μs. The leading (negative going) edge of this gate should be coincident with the positive going edge of the signal at TP3206.

(c) Remove the oscilloscope and trigger source.

5.5I FINAL ADJUSTMENTS (Sampling Head Installed)

(1) Sampling Head Adjustments

(a) Set the M163 controls as follows.

Input Range: 1 V
Samples Averaged: 10^3
Zero: mid-range
Baseline Sample Delay: fully counter-clockwise
Baseline Sample Int/Ext: INT

(b) Unplug the Sampling Head Extender board (EG&G PARC #1710-0017). Then TURN THE M162 MAINFRAME POWER

OFF and plug the Sampling Head into the M163. **NOTE:** Do not disturb any of the Sampling Head adjustments.

(c) Connect a shorting plug to the Input of the Sampling Head so that its input is grounded.

(d) Connect the DVM to the M163 OUTPUT pin jack.

(e) Set the M163 Sensitivity switch to 100 mV. Then adjust the Sampling Head BALANCE adjustment for a DVM indication of 0.00 V. **NOTE:** In the case of a Model S5 Sampling Head, this adjustment is on the front panel of the Sampling Head. For all other Sampling Heads, it is located on the left side (facing the unit from the front).

(f) Set the M163 Sensitivity switch to the 1 V position. Then adjust the M163 ZERO control for a DVM indication of 0.00 V.

(g) Set the Sensitivity switch back to 100 mV, and again set the Sampling Head BAL adjustment for 0.00 V at the DVM.

(h) Continue alternating between the ZERO adjustment (Sensitivity to 1 V) and the Sampling Head adjustment (Sensitivity to 100 mV) until no further improvement in the zero setting procedure can be obtained. It should be possible to achieve better than ±2 mV with the 1 V sensitivity and better than ±20 mV with the 100 mV sensitivity. LEAVE THE SENSITIVITY SET TO 1 V.

(2) SIG. CAL (R3096; Signal board)

(a) Connect the DVM to TP5. Then note and record the DVM indication.

(b) Remove the ground from the Sampling Head input and apply instead an externally derived source of + 1.000 V.

(c) Adjust R3096 (SIG. CAL) for a DVM indication 10.00 V more negative than that recorded in step (a). Record the final voltage indication.

(3) COMMON MODE ADJUST (R3144; Signal board)

(a) Transfer the DVM to the front-panel OUTPUT pin jack.

(b) Adjust R3144 (COMMON MODE ADJ) so that the indicated voltage is the same as that recorded in step 2(c) above.

(4) BASELINE CAL (R3098; Signal board and BASELINE ZERO; Signal board)

(a) Ground the Sampling Head input with an appropriate grounding plug and adjust the M163 front-panel ZERO control for 0.00 V at the M163 front-panel OUTPUT pin jack.

(b) Set the Baseline Sample Delay control to about the center of its range. Then adjust R3177 for 0.00 V at the M163 front-panel OUTPUT pin jack.

(c) Transfer the DVM to TP8 and set the M163 Sensitivity to 1 V. Note and record the DVM indication.

(d) Remove the ground from the Sampling Head Input and apply + 1.000 V to the Sampling Head Input instead.

(e) Adjust R3098 (BASELINE CAL) so that the voltage at TP8 is exactly 10.00 V more negative than that recorded in step (b).

(f) Remove the DVM.

This completes the M163 alignment. After turning off the power, the M163 can be returned to its proper position in the M162.

5.6 MODEL 164 ALIGNMENT

5.6A PRELIMINARY STEPS

(1) With the mainframe power off, plug the Extension Cable Assembly (#6020-0093) into slot "A" of the mainframe. Then plug the M164 into the free end of the cable. When the connections are made, turn the mainframe power back on and allow a fifteen minute warmup before proceeding.

NOTE: When aligning a M164, there should not be a M163 plugged into the "unused" channel. With a M163 installed, the maximum trigger rate is limited to 10 kHz. Also, in the case of a unit equipped with the Digital Storage Option, the "flat-ribbon" cable that interconnects the Digital Storage board and the "upper" board should be disconnected. This cable should be unplugged at the end that plugs into the upper board.

(2) Set the mainframe controls as follows:

Aperture Delay Range: 10 μSEC
% Initial A: 1.00
Aperture Duration: outer knob to 5 μSEC; inner to CAL
Scan Time: outer knob to .01 μSEC; inner to CAL

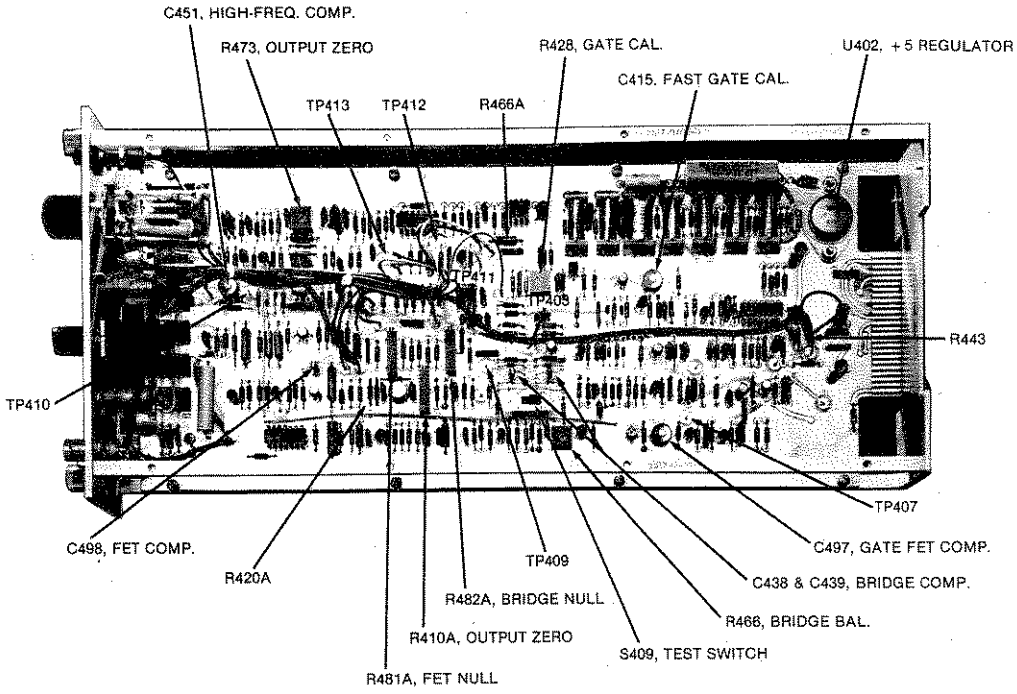


Figure V-6. MODEL 164 ADJUSTMENTS AND TEST POINTS

Scan Select pushbuttons: EXT depressed; others released
Trigger Mode pushbuttons: EXT depressed; others released
Function: A
Time Constant: .1 mSEC; CAL

(3) Set the M164 controls as follows.

Pushbuttons: Select 50 Ω, DC, GND, and EXP
Time Constant: 1 μSEC
Zero: Mid-range
Gate Trim: Mid-range
Calibrate: Mid-range
Test switch (mounted on PC board): Test position (forward position)

5.6B APERTURE DURATION ADJUSTMENTS AND CHECKS

(1) GATE CAL (R428)

(a) Connect a 1 V rms sine wave at 50 kHz to the Trigger INPUT connector and set the Trigger Level control for proper triggering as indicated by the TRIGGERED lamp.

(b) Connect the counter to TP403. The counter cable should be a twisted pair with a 100 Ω resistor in series with the signal lead at the source end. Set the counter controls so that the counter will start on the positive going edge and stop on the negative going edge.

(c) Monitor TP403 with the oscilloscope. The observed signal should be a positive pulse with a −3 V (nominal) baseline and a +1.2 V (nominal) peak. The pulse width should be approximately 5 μs. Remove the oscilloscope.

(d) Observe the counter indication, adjust R428 (GATE CAL) for an indicated pulse duration of 5.0 μs. Then remove the counter and reconnect the oscilloscope to TP403.

(2) FAST GATE CAL (C415)

(a) Set the outer knob of the Aperture Duration switch to 5 nSEC and the inner knob to X10.

(b) Adjust C415 (FAST GATE CAL) so that the duration of the pulse at TP403 is 55 ns.

(3) Aperture Duration Checks

(a) While continuing to monitor the signal at TP403, rotate the Aperture Duration switch (outer knob only; inner knob at ×10) through each of its positions. The duration as a function of the switch setting should be as follows. **NOTE:** To prevent overlap, it may prove convenient to increase the Aperture Duration Range as required to keep the Aperture Duration Range longer than the gate width. Reducing the input trigger frequency is also advisable.

Switch Position	Approximate Pulse Width
50 nSEC	550 nSEC
.5 μSEC	5.5 μSEC
5 μSEC	55 μSEC
50 μSEC	550 μSEC
500 μSEC	5500 μSEC

(b) Transfer the oscilloscope to TP407. Then set the Aperture Duration switch to 5 μSEC (vernier to CAL). The observed signal should be a negative-going 15 V pulse with its baseline at 0 V.

(c) Successively set the outer knob of the Aperture Duration switch to 50 μSEC and to 500 μSEC. The duration of the observed pulse should increase, matching the selected Aperture Duration in each case.

(d) Check that no pulse is observed with the Aperture Duration switch set to 5 nSEC, 50 nSEC, or .5 μSEC. Instead, there is a continuous – 15 V dc level at TP407.

(4) GATE OUT Checks

(a) Terminate the GATE OUT connector in 50 Ω and monitor the GATE OUT signal with the oscilloscope. Set the trigger frequency to 5 kHz and the Aperture Delay Range to 1 μSEC.

(b) Set the Aperture Duration to 50 nSEC and CAL. The pulse at the GATE OUT connector should have an amplitude of approximately 0.25 V.

(c) Set the Aperture Duration to 5 nSEC and CAL. The GATE OUT signal will not be able to track this fast an aperture but nevertheless should still have an amplitude of about 200 mV.

(5) OVERLAP Check

(a) Set up the oscilloscope controls to monitor two waveforms at once. Connect the scope input to either end of resistor R443. Connect the other to the GATE OUT connector (still terminated in 50 Ω).

(b) Set the Aperture Delay Range to .5 μSEC. Then set the Aperture Duration switch to 50 nSEC and CAL. A negative going TTL pulse will be observed at R443. A positive pulse will be observed at the GATE OUT connector.

(c) Begin rotating the inner knob of the Aperture Duration control clockwise. The GATE OUT pulse will be observed to increase in width. When its width exceeds that of the 500 ns pulse at R443, the OVERLAP indicator lamp will glow. Return the inner knob of the Aperture Duration control to CAL.

(d) Remove the oscilloscope from the monitored points. Also remove the 50 Ω termination from the GATE OUT connector.

5.6C SIGNAL CHANNEL ADJUSTMENTS AND CHECKS

(1) OUTPUT ZERO (R473)

(a) Connect the DVM between TP410 and ground. Connect a jumper between TP411 and ground.

(b) Adjust R473 (OUTPUT ZERO) for 0.000 V at TP410.

(2) HIGH-FREQ. COMPENSATION (C451)

(a) Release the front-panel EXT/SUM and GND pushbutton.

(b) Monitor TP413 with the DVM and adjust the front-panel ZERO OFFSET control for an indicated voltage of 0.000 V.

(c) Transfer the DVM back to TP410 and press in the front-panel CAL pushbutton. The DVM voltage indication should be 580 mV ± 25 mV. Release the CAL pushbutton.

(d) Set the controls of the fast pulse generator to provide a 50 ns 1 MHz pulse with an amplitude of 100 mV. Then connect this pulse to the M164 INPUT connector. The pushbuttons should be set for dc coupling, 50 Ω.

(e) Set the oscilloscope for sampling operation and monitor the signal at TP410. The DVM should be removed from TP410.

(f) Observing the displayed signal, adjust C451 (HIGH-FREQ. COMPENSATION) for a correctly compensated waveform.

(g) Remove the oscilloscope and pulse generator.

(3) BRIDGE BAL (R466)

(a) Increase the Aperture Duration to 500 nSEC (CAL) and set the Aperture Delay Range to 1 μSEC. Connect the oscilloscope to TP409.

(b) Adjust R466 (BRIDGE BAL) so that the sampled area is even with the line. Remove the oscilloscope from TP409.

(4) OUTPUT ZERO (R410A)

(a) Connect the DVM to the M164 OUTPUT pin jack.

(b) Connect a jumper from the upper end of resistor R420A to ground.

(c) Press CLEAR and adjust R410A (OUTPUT ZERO) for a DVM indication of 0.00 V.

(d) Remove the jumper extending from R420A to ground and also that extending from TP411 to ground. Leave the voltmeter connected to the front-panel pin jack.

(5) ZERO and CAL ADJ (front-panel adjustments)

(a) Set S409 (switch mounted on the PC board) to the OPERATE (rear) position.

(b) Depress the GND and EXP/SUM pushbuttons.

(c) Set the M164 Time Constant to 10 mSEC and the Aperture Delay Range to 10 μSEC.

(d) Set the Aperture Duration to 5 μSEC and CAL.

(e) Adjust the front-panel OUTPUT ZERO adjustment for 0.000 V at the pin jack.

(f) Release the GND pushbutton and depress the CAL pushbutton. Then adjust the front-panel CAL screwdriver adjustment for -10.000 V ± 3 mV at the pin jack.

(g) Release the CAL pushbutton and remove the DVM from the pin jack.

(6) Time Constant Checks

(a) Select CONT. GATE and 1 MΩ with the front-panel pushbuttons.

(b) Supply a 10 mV rms sine wave at 16 Hz to the M164 Input and set the M164 Time Constant to 10 mSEC.

(c) Monitor the signal at the front-panel pin jack with an accurate ac voltmeter. Then adjust the frequency of the input sine wave (keeping the input amplitude constant) until the indicated output amplitude is .707 V rms. The frequency of the applied sine wave should be 16 Hz $\pm$ 2 Hz.

(d) Set the M164 Time Constant to 1 mSEC. Then increase the frequency of the input sine wave (keeping the input amplitude a constant 10 mV rms) until the indicated output amplitude is 0.707 V rms. The frequency of the applied signal should be 160 Hz $\pm$ 20 Hz.

(e) Set the M164 Time Constant to 100 μSEC. Then increase the frequency of the input sine wave (keeping the input amplitude a constant 10 mV rms) until the indicated output amplitude is again 0.707 V rms. The frequency of the applied signal should be 1.6 kHz $\pm$ 200 Hz.

(f) Set the M164 Time Constant to 10 μSEC. Then increase the frequency of the input sine wave (keeping the input amplitude a constant 10 mV rms) until the indicated output amplitude again is 0.707 V rms. The frequency of the applied sine wave should be 16 kHz $\pm$ 2 kHz.

(g) Release the CONT. GATE pushbutton and remove the signal generator.

(h) Connect the DVM to the M164 front-panel OUTPUT pin jack. Then, while alternating the M164 Time Constant switch between the 1 μs and 10 μs positions, adjust C497 (GATE FET COMP.) for less than 20 mV change in the DVM indication.

(7) Bridge Switching Offset (C438 and C439)

(a) Set the M164 Time Constant to 1 μSEC.

(b) Adjust C438 and/or C439 so that the DVM change is less than 20 mV while switching the Aperture Duration between 5 nSEC and 5 μSEC. (Adjustment made in 5 nSEC position.)

(8) BRIDGE NULL & FET NULL (R482A, R481A)

(a) Disconnect the trigger signal applied to the Trigger INPUT connector.

(b) Set the Aperture Duration to .5 μSEC and CAL.

(c) Set the M164 Time Constant to 1 μSEC.

(d) Hold down the M164 CLEAR pushbutton. The panel-meter indication will go to zero. At some convenient time, release the CLEAR pushbutton. The meter indication will drift away from zero. Adjust R482A (BRIDGE NULL) so that the rate of drift is minimum. If the output should reach full scale while the adjustment is in progress, momentarily depress the CLEAR pushbutton to restore the zero indication and continue the adjustment procedure.

(e) Set the Aperture Duration switch to 5 μSEC and CAL.

(f) Momentarily depress the CLEAR pushbutton to establish a zero indication. Then adjust R481A (FET NULL) for minimum drift in the zero indication. As before, if the output indication should reach full scale, restore the zero indication with the CLEAR pushbutton and continue the procedure.

(9) Overload Checks

(a) Select SUMMATION averaging, DC coupling, and a 1 MΩ input impedance with the M164 front-panel pushbuttons.

(b) Place test-switch S409 in the TEST (forward) position.

(c) Connect a jumper from TP411 to ground.

(d) Press in the M162 INT. Trigger Mode pushbutton.

(e) Apply a 20 Hz sine wave having an amplitude of 820 mV pk-pk to the M164 Input. The OVERLOAD light should glow.

(f) Monitor TP410 with the oscilloscope. The observed signal should be a 20 Hz sine wave with a pk-pk amplitude of 4.1 V pk-pk.

(g) Make provision to simultaneously monitor the signal at TP412. The signal at TP412 should be a TTL rectangular waveform that goes to logic 0 each time the TP410 signal exceeds plus or minus two volts.

(h) Reduce the input frequency to 1 Hz. Then transfer the oscilloscope to the rear-most end of resistor R466A. The observed signal should be a + 14 V pulse (nominal) with a duration of nominally 300 ms.

(i) Remove the oscilloscope, the applied input signal, and the jumper (TP411).

(10) FET COMPENSATION (C498)

(a) Press in the EXT Trigger Mode pushbutton and apply a 100 Hz 1 V trigger input signal to the Trigger INPUT connector. Establish proper triggering with the Trigger Level control. In the case of a unit equipped with the Digital Storage option, be sure that the cable extending from the Digital Storage board to the upper M162 board is disconnected at the upper-board end.

(b) Set the Aperture Delay Range to 5 mSEC.

(c) Set the % INITIAL A and B dials to 30%.

(d) Set the Aperture Duration switch to 5 μSEC and CAL.

(e) Press in the EXT Scan Select pushbutton.

(f) Set S409, the PC board test switch, back to OPERATE (rear position).

(g) Select Digital Storage ON with the inner knob of the Function switch. The outer knob should still be set to "A".

(h) Set the M164 Time Constant to 1 μSEC.

(i) Select EXP averaging and GND with the M164 Input pushbuttons.

(j) Monitor the signal at the M164 front-panel pin jack with the oscilloscope. The scope should be ac coupled, the sweep rate should be 5 mSEC/cm, and the vertical sensitivity should be 50 mV/cm.

(k) Adjust C498 (FET COMPENSATION) and the M164 front-panel ZERO control together as required to achieve minimum amplitude pedestals in the observed waveform. It should be possible to reduce the pedestals to less than 10 mV.

This completes the M164 alignment. The test equipment can be removed. If the digital storage board cable was removed in an earlier step, reconnect it now.

5.7 ALIGNMENT PROCEDURES FOR 162/95, 162/96 AND 162/97 OPTIONS

5.7A EQUIPMENT REQUIRED

(1) Two adjustable power supplies, each capable of furnishing voltages anywhere in the range of 0 V to 10 V, either polarity.

(2) A general-purpose digital voltmeter, hereafter referred to as DVM.

(3) A Model 162 mainframe known to be in good working order. Plug-in Processor Modules are not required.

(4) An Option-Board Extender (#1710-00-1601).

(5) Cables, clip leads, etc. as required. **NOTE:** When the Model 162 is shipped, it is provided with a connector/cable assembly that gives access to P101 (rear panel of 162). This assembly will be required.

5.7B PROCEDURE STEPS THAT APPLY FOR ALL OPTIONS

(1) If the option board to be aligned is already installed in the mainframe, unplug it, install the extender card (#1710-0016) in its place, and plug the option board into the extender with the component side of the option board facing the rear of the instrument. For instructions on the option board installation, see the paragraphs entitled OPTIONAL FUNCTIONS in Subsection 4.13C.

(2) Examine the connector/cable assembly that interfaces to P101 at the rear of the Model 162. Identify those wires of the flat-ribbon cable that terminate in pins 1, 25, and 49. Strip the end of each of these wires so that connections can be made to them. Channel B "output" voltages will be applied to pin 49. Ground connections will be made at pin 25.

(3) Set the Model 162 controls as follows.

Aperture Delay Range: 10 μs
% Initial A and B: 50%
Aperture Duration: setting immaterial
Scan Time: setting immaterial
Trigger Mode: INT
Scan/Select: EXT
Function: will be set in later step
Mainframe Time Constant: 0.1 mSEC and CAL
Power: ON

5.7C PROCEDURE FOR A MODEL 162/95 PRODUCT OPTION

(1) U9501 ZERO (R9507) and U9502 ZERO (R9511)

(a) Set the FUNCTION switch to A × B.

(b) Check the position of the slide switch on the option board itself. It should be in the A × B position.

(c) At the Option board, connect a jumper from TP9507 to ground.

(d) Monitor the voltage at TP9502 with the DVM. Then adjust R9507 (U9501 ZERO) for a DVM indication of 0.00 V.

(e) Transfer the DVM to TP9503. Then adjust R9511 (U9502 ZERO) for a DVM indication of 0.00 V.

(f) Repeat steps (d) and (e) until no further improvement in the two zero adjustments can be made.

(g) Remove the jumper from TP9507.

(2) U9503 ZERO (R9522)

(a) Connect a jumper from TP9504 to ground.

(b) Monitor the voltage at TP9506 with the DVM and adjust R9522 (U9503 ZERO) for a DVM indication of 0.00 V.

(c) Remove the jumper from TP9504.

(3) X_o (R9516), Y_o (R9517), and Z_o (R9518) Adjustments

(a) At the rear-panel connector/cable assembly, connect the output of one of the power supplies to pin 1 and the output of the other to pin 49. Use pin 25 for ground. The polarity should be such that negative voltages will be applied to pins 1 and 49, although the actual initial level applied should be 0 V.

(b) Set the slide switch on the Option board to the A/B (Ratio) position. Also, set the front-panel FUNCTION switch to SPEC.

(c) Set the voltage applied to pin 49 of P101 to 0 V and that applied to pin 1 to −1 V.

(d) Monitor the voltage at TP9506 with the DVM. Then vary the voltage applied to pin 1 of P101 over the range of −1 V to −10 V. Adjust R9518 (Z_o) so that the smallest possible voltage change takes place at TP9506 as the voltage at pin 1 of P101 is varied over the range of −1 V to −10 V.

(e) Leave the voltage applied to pin 49 at 0 V and set that applied to pin 1 at −10.000 V.

(f) While continuing to monitor the voltage at TP9506, adjust R9517 (Y_o) for a DVM indication of 0.00 V.

(g) Disconnect that power supply which is connected to pin 49 of P101. Then jumper pin 1 to 49 so that the voltage applied to pin 1 will also be applied to pin 49.

(h) Vary the voltage applied to pins 1 and 49 over the range of −1 V to −10 V. While so doing, adjust R9516 (X_o) as required to achieve the smallest possible change in the TP9506 voltage.

(i) Repeat steps (c) through (h) once more.

(4) A/B SCALE FACTOR (R9515)

(a) While observing the DVM, which should still be connected to TP9506, vary the voltage applied to pins 1 and 49 over the range of −1 V to −10 V.

(b) Set R9515 (A/B SCALE FACTOR) such that, as the applied voltage is varied from −1 V to −10 V, the DVM indication varies no more than ±10 mV around −10 V.

(5) A × B SCALE FACTOR (R9526)

(a) Set both the A × B FUNCTION switch and the Mode switch on the Option board to A × B.

(b) Set the level of the voltage applied to pins 1 and 49 to −10.000 V.

(c) Adjust R9526 (A × B SCALE FACTOR) for a DVM indication (TP9506) of −10 V ±10 mV.

(6) POLARITY COMPENSATION(R9528)

(a) Change the power supply connections such that +10.000 V is applied to both pins 1 and 49.

(b) Adjust R9528 (POLARITY COMPENSATION) such that the indicated voltage at TP9506 is −10.00 V ±10 mV.

(7) Product Checks

(a) Change the power supply connections such that one supply drives pin 1 (Channel B) and the other pin 49 (Channel A). The polarity should be such as to supply positive voltages to both points.

(b) Apply +10 V to both pins 1 and 49. The voltage at TP9506 should be −10 V ±0.1 V.

(c) Apply +1 V to pin 49 and +10 V to pin 1. The voltage at TP9506 should be −1.00 V ±0.1 V.

(d) Apply +200 mV to pin 49 and +10 V to pin 1. The voltage at TP9506 should be −200 mV ±100 mV.

(8) Ratio Checks

(a) Set the FUNCTION switch to SPEC and the Option Board Mode switch to A/B.

(b) Apply −10.00 V to both pins 1 and 49. The DVM indication should be −10.00 V ±100 mV.

(c) Apply −10.00 V to pin 1 and −1.00 V to pin 49. The DVM indication should be −1.00 V ±100 mV.

(d) Apply −10.00 V to pin 1 and −200 mV to pin 49. The DVM indication should be −200 mV ±100 mV.

(e) Apply +1.00 V to pin 1 and −1.00 V to pin 49. The DVM indication should be −10.00 V ±100 mV.

(f) Apply +1.00 V to pin 1 and −200 mV to pin 49. The DVM indication should be −200 mV ±100 mV.

This completes the alignment and checks for the product option board. Turn off the power, disconnect the power supplies, and return the Option board to its proper connector. Unless immediate operation in the ratio mode is intended, it is probably better to leave the Option Board Mode switch in the A × B position.

5.7D PROCEDURE FOR A MODEL 162/96 LOG RATIO OPTION

NOTE: Underlying assumption is that the steps in Subsection 5.7B have been performed.

(1) 1 kHz Oscillator Checks

(a) Set the FUNCTION switch to LOG (A/B).

(b) Set the voltage applied to pin 1 of P101 to −10.00 V. Set the voltage applied to pin 49 to −1.00 V.

(c) Monitor the signal at each end of R9621 (AC BAL) with the oscilloscope. The signal at one end should be 180° out of phase with that at the other end. Otherwise they should be the same. The waveform shape should be as indicated in Figure V-7.

(2) CHANNEL A ZERO (R9605)

(a) Connect the DVM to TP9602.

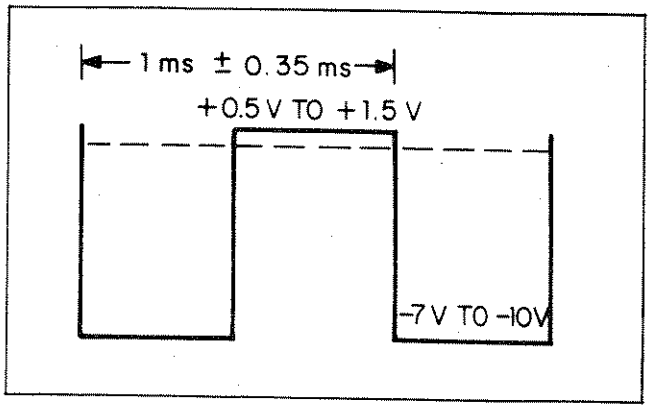


Figure V-7. OSCILLATOR OUTPUT SIGNALS

(b) Alternate the voltage applied to pin 49 of P101 between +1.00 V and −1.00 V. While so doing, note the change in the voltage at TP9602 (nominal level should be −4 V). Adjust R9605 (CHANNEL A ZERO) so that the observed *change* caused by alternating the voltage is less than 2 mV. LEAVE THE APPLIED VOLTAGE (pin 49) SET AT −1 V.

(3) CHANNEL B ZERO (R9612)

(a) Switch the voltage applied to pin 1 between +10 V and −10 V, and note the effect on the voltage at TP9602 (nominal voltage level should be −4 V).

(b) While alternating the pin 1 voltage between +10 V and −10 V, adjust R9612 (CHANNEL B ZERO) such that the observed voltage change is less than 4 mV. Leave the voltage applied to pin 1 at −10 V.

(4) OUTPUT ZERO (R9624)

(a) Make provision for applying the same voltage to both pins 1 and 49. Set the voltage to −10 V.

(b) Adjust R9624 (OUTPUT ZERO) so that the voltage at TP9602 is 0 V ±1 mV.

(5) AC BALANCE (R9621)

(a) Vary the applied voltage over the range of −10 V to +1 V, noting the effect on the voltage at TP9602.

(b) Adjust R9621 (AC BALANCE) such that the observed change at TP9602 as the applied voltage is varied from −10 V to +1 V will be less than ±50 mV.

(6) OUTPUT ZERO (R9624)

(a) Set the potential applied to both pins 1 and 49 to −10 V.

(b) Adjust R9624 (OUTPUT ZERO) for 0 V ±1 mV at TP9602.

(7) OUTPUT SCALE (R9617)

(a) Change the power supply connections such that +1.00 V is applied to pin 49 and +10.00 V is applied to pin 1.

(b) Adjust R9617 (OUTPUT SCALE) for −4.000 V at TP9602.

(8) LOG ∞ ADJUST (R9622)

(a) Set the voltage applied to pin 49 to +31.6 mV (the voltage applied to pin 1 should still be +10.00 V).

(b) Adjust R9622 for −10.00 V at TP9602.

(9) Log Ratio Final Checks

(a) Set the voltage applied to pin 1 to −10.00 V and that applied to pin 49 to −10.00 V. The voltage at TP9602 should be 0 V ±4 mV.

(b) Set the voltage applied to pin 1 to −10.00 V and that applied to pin 49 to −1.00 V. The voltage at TP9602 should be −4 V ±10 mV.

(c) Set the voltage applied to pin 1 to −10.00 V and that applied to pin 49 to −100 mV. The voltage at TP9602 should be −8 V ±20 mV.

(d) Set the voltage applied to pin 1 to −1.00 V and that applied to pin 49 to −100 mV. The voltage at TP9602 should be −4 V ±40 mV.

(e) Set the voltage applied to pin 1 to −1.00 V and that applied to pin 49 to −1.00 V. The voltage at TP9602 should be 0 V ±40 mV.

(f) Set the voltage applied to pin 1 to −1.00 V and that applied to pin 49 to −10 mV. The voltage at TP9602 should be −8 V ±400 mV.

This completes the alignment and checks for the log ratio option board. Turn off the power, disconnect the power supplies, and return the Option board to its proper connector.

5.7E PROCEDURE FOR A MODEL 162/97 RATIO OPTION

NOTE: Underlying assumption is that the option board is mounted on an option board extender card and that the component side of the option board faces the rear of the instrument. The mainframe control settings should be as given in Subsection 5.7B. Also, note that there are two versions of this option, easily distinguished by the number of adjustments. In one version there are eight adjustments. In the other there are five. The five adjustments discussed apply to both versions. The three additional adjustments in the first version should never require field alignment.

(1) Modulator Check

(a) Set the Model 162 FUNCTION switch to A/B.

(b) Set the voltage applied to pin 49 to − 3.2 V and that applied to pin 1 to − 10.00 V.

(c) Trigger the oscilloscope from the leading edge of the pulse at TP9709,

(d) Monitor the signal at TP9702. The observed signal should be as indicated in Figure V-8.

(2) A.G.C. ZERO ADJUST (R9741)

(a) Connect a clip lead from TP8711 to TP9701.

(b) Monitor the voltage at TP9704 with the DVM and adjust R9741 (A.G.C. ZERO) for 0 V. (Adjustment may drift quickly. This is normal.)

(c) Remove the clip lead.

(3) DC RESTORER ADJUST (R9724)

(a) Connect the oscilloscope to TP9708. The waveform should be as indicated in Figure V-9.

(b) Adjust R9724 (DC RESTORER ADJUST) so that the voltage in the "sample" interval as indicated in Figure V-9 is 0 V ± 2 mV.

(4) ABSOLUTE VALUE ADJUST (R9753)

(a) Change the voltage applied to pin 49 of P101 to − 10 V.

(b) Connect the DVM to R9739 (either end). The voltage should be about − 10 V.

(c) Alternate the voltage applied to pin 1 of P101 between + 10.00 V and − 10.00 V, noting the change in the voltage at R9739.

(d) Adjust R9753 (ABSOLUTE VALUE ADJUST) such that the observed change is

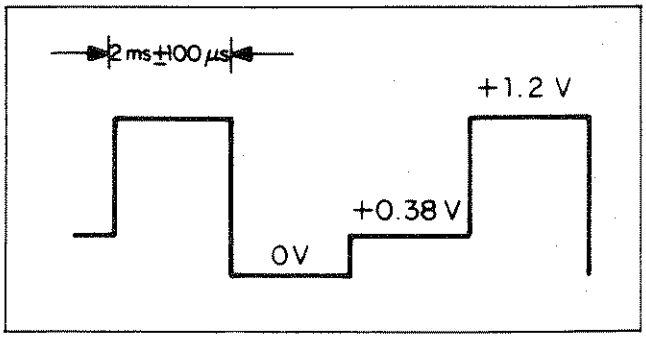


Figure V-8. INPUT MODULATOR CHECK WAVEFORMS

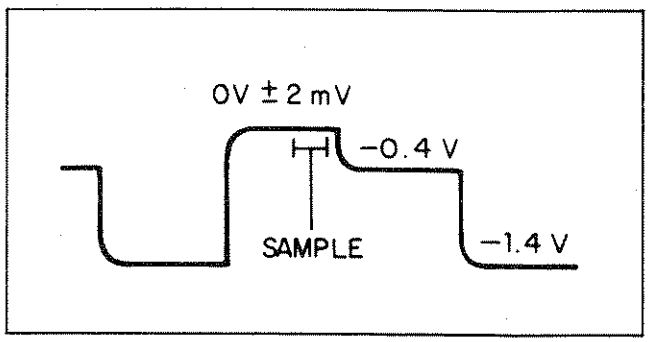


Figure V-9. DC RESTORER OUT

less than 5 mV as the voltage at pin 1 is switched between + 10.00 V and − 10.00 V. Leave the voltage applied to pin 1 at − 10.00 V.

(5) OUTPUT ZERO ADJUST (R9754)

(a) Set the voltage applied to pin 49 of P101 to 0.00 V.

(b) While continuing to monitor the voltage at R9739, adjust R9754 (OUTPUT ZERO ADJUST) for a DVM indication of 0.00 V ± 5 mV.

(6) SCALE ADJUST (R9752)

(a) Set the voltage applied to pin 49 of P101 to − 10.00 V, the same voltage as is applied to pin 1 (the same supply may be connected to both pins).

(b) Adjust R9752 (SCALE ADJUST) for a DVM indication (DVM should still be monitoring R9739) of + 10.000 V.

(7) RATIO CHECKS (DVM monitors voltage at R9739 in each case)

(a) Set the voltage applied to pin 49 to 0.00 V and that applied to pin 1 to − 1.00 V. The DVM indication should be 0.00 V ± 50 mV.

(b) Set the voltage applied to pin 49 to − 5.00 V and that applied to pin 1 to − 5.00 V. The DVM indication should be − 10.00 V ± 50 mV.

(c) Set the voltage applied to pin 49 to − 2.00 V and that applied to pin 1 to − 8.00 V. The DVM indication should be − 2.50 V ± 50 mV.

(d) Set the voltage applied to pin 49 to − 10.00 V and that applied to pin 1 to − 10.00 V. The DVM indication should be − 10 V ± 50 mV.

This completes the alignment and checks for the ratio option board. Turn off the power, disconnect the power supplies, and return the Ratio Option board to its proper connector.

5.8 ALIGNMENT PROCEDURE FOR MODEL 162/99 DIGITAL STORAGE OPTION

5.8A INTRODUCTION

The basic underlying assumptions for this alignment are that the Digital Storage Option is installed, that it works, and that the alignment is being performed as part of a periodic maintenance program, or possibly as a post-repair procedure. The digital storage board is "dual", that is, the circuitry that services Channel B is the same as, but separate from, that which services Channel A. A processor module (Model 163 or Model 164) must be installed in the channel being aligned. One can install a single module, and move it as necessity dictates, or install two processor modules if two are available. Note that certain of the Digital Storage Adjustments are outlined in Section IV of the manual. The adjustments in Section IV are those which match a given Digital Storage Module to a specific processor module or pair of processor modules. The general alignment that follows can be performed with any processor module. However, before digital storage can be used in a measurement, the Digital Storage adjustments of Section IV *must also* be performed to match the digital storage option to the specific processor module.

5.8B PROCEDURE

(1) Set the mainframe controls as follows.

Aperture Delay Range: 10 μSEC
% Initial A and B: 10%
Aperture Duration: 5 μSEC if Processor Module is M164. Setting immaterial if P.M. is M163.
Scan Time: setting immaterial
Function: Outer knob to "A". Inner knob to Dig. Stor. ON.
Time Constant: 10 mSEC and CAL
Scan Select pushbuttons: EXT depressed; others released. Make provision for triggering at 100 Hz from external trigger source. Set Trigger Level control as required for reliable triggering.
Power: ON

(2) Set Processor Module controls as follows.

Model 164
Pushbuttons: Select EXT, GND, DC and 1 MΩ
Time Constant: 1 μSEC
Zero Control: Once proper triggering is established, adjust Zero Control for 0.00 V at the M164 OUTPUT pin jack. Each time the M164 is moved (if it is moved) recheck the Zero adjustment and touch it up if necessary.

Model 163
A Sampling Head should be installed. A suitable grounding plug should be connected to the Sampling Head input.

Input Range: 1 V
Samples Averaged: 10^2
Baseline Sample Delay: outer knob fully counterclockwise; inner knob pushed in.
Zero Control: Once proper triggering is established, adjust the Zero control for 0.00 V at the M163 OUTPUT pin jack. If a single processor module is being used, which will require moving the P.M. in the course of the procedure according to which channel is being aligned, the Zero Adjustment should be checked and, if necessary, touched up each time the module position is changed.

(3) Remove the top cover (secured by two screws on the under surface of the "overhang" at the rear of the instrument).

(4) Turn the power off. Then remove integrated circuits U9915, U9916, U9925, and U9926 from their sockets, taking careful notice of the orientation in each case so that they can be correctly inserted later on.

(5) CHANNEL A D/A SUMMING AMP. ZERO (R9948)

(a) Connect a clip lead from TP9902 to ground.

(b) Monitor TP9903 with the oscilloscope and adjust R9948 for nominally 0 V. **NOTE:** This is a high-gain open-loop adjustment. The best one can do will usually be to find that setting where a slight adjustment in either direction will "snap" the voltage at TP9903 from one extreme to the other.

(c) Remove the clip lead from TP9902.

(6) CHANNEL A D/A OUTPUT ZERO (R9954)

(a) While continuing to monitor TP9903 with the oscilloscope, press and hold in the Processor Module CLEAR pushbutton. Then adjust R9954 for 0 V ±10 mV at TP9903.

(b) Release the CLEAR pushbutton.

(7) CHANNEL A ×100 ZERO ADJUSTMENT (R9943)

(a) Place Integrated Circuits U9915 and U9916 (removed in step 4) back into their sockets.

(b) Connect a clip lead from TP9905 to ground.

(c) Monitor the signal at TP9906 with the oscilloscope. Then adjust R9943 for nominally 0 V. This is another high-gain open-loop adjustment and the adjustment criteria discussed in step 5(b) will apply.

(d) Disconnect the grounding clip lead from TP9905.

(8) CHANNEL A INTEGRATOR ZERO ADJUSTMENT (R9950)

(a) Connect the clip lead from TP9906 to ground.

(b) Monitor TP9907 with the oscilloscope and adjust R9950 for a smooth 0 V dc level. A suitable oscilloscope sensitivity would be 10 mV/cm.

(c) Remove the grounding clip lead from TP9906.

(9) CHANNEL B D/A SUMMING AMP ZERO (R9991)

NOTE: If the procedure is being performed with a single processor module, it will be necessary to transfer the module from the Channel A to the Channel B position at this time. After making the transfer, touch up the processor module zero adjustment before proceeding.

(a) Connect a clip lead from TP9909 to ground.

(b) Monitor TP9910 with the oscilloscope and adjust R9991 for nominally 0 V at TP9910. Again, this is an open-loop high-gain adjustment, and the best that one can expect to do is to find that point where a slight adjustment in either direction will "snap" the voltage to one extreme or the other.

(c) Remove the clip lead from TP9909.

(10) CHANNEL B D/A OUTPUT ZERO (R9997)

(a) While continuing to monitor TP9910 with the oscilloscope, press and hold in the Processor Module CLEAR pushbutton. Then adjust R9997 for 0 V ± 10 mV on the oscilloscope.

(b) Release the CLEAR pushbutton.

(11) CHANNEL B × 100 ZERO ADJUSTMENT (R9980)

(a) Place Integrated Circuits U9925 and U9926 (removed in step 4) back into their sockets.

(b) Connect a clip lead from TP9912 to ground.

(c) Monitor TP9913 with the oscilloscope. Then adjust R9980 for nominally 0 V at TP9913. Again, this is a high-gain open-loop adjustment and the best one can expect to do is to find that point where a small adjustment in one direction or the other will "snap" the monitored voltage to the extremes.

(d) Remove the clip lead from TP9912.

(12) CHANNEL B INTEGRATOR ZERO ADJUSTMENT (R9993)

(a) Connect a clip lead from TP9913 to ground.

(b) Monitor TP9914 with the oscilloscope (use 10 mV/cm sensitivity). Then adjust R9993 for a smooth 0 V dc level.

(c) Remove the clip lead from TP9913.

NOTE: This completes the general alignment of the digital storage option board. It does not match the digital storage board to a specific processor module or modules. That operation is performed using the procedure in Subsection 4.14C (MATCHING DIGITAL STORAGE OPTION TO PROCESSOR MODULE).

SECTION VI
TROUBLESHOOTING

6.1 SAFETY NOTICE

WARNING!

POTENTIALLY LETHAL VOLTAGES ARE PRESENT INSIDE THIS APPARATUS. These service instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Any adjustment, maintenance and repair of the opened apparatus under voltage shall be avoided as far as possible and, if unavoidable, shall be carried out only by a skilled person who is aware of the hazard involved. When the apparatus is connected to a power source, terminals may be live, and the opening of covers or removal of parts is likely to expose live parts. The apparatus shall be disconnected from all voltage sources before it is opened for any adjustment, maintenance, or repair. Note that capacitors inside the apparatus may still be charged even if the apparatus has been disconnected from all voltage sources. Service personnel are thus advised to wait several minutes after unplugging the instrument before assuming that all capacitors are discharged. If any fuses are replaced, be sure to replace them with fuses of the same current and voltage rating and of the same type. The use of makeshift fuses and the short-circuiting of fuse holders are prohibited.

6.2 INTRODUCTION

This section consists of a detailed block diagram discussion of the Models 162, 163 and 164, followed by a series of procedures to be followed in troubleshooting these instruments. By making voltage and waveform checks at critical points, it should be possible to narrow the trouble down to one of the circuit boards, and in many cases even to identify the specific malfunctioning circuit. Once the problem has been localized, the operator is advised to contact the factory or the factory-authorized representative in his area for advice on how to get the instrument back into operation in the shortest possible time. In the case of units still in Warranty, it is particularly important that the factory or one of its representatives be contacted before doing any work on a circuit board, as any damages incurred from unauthorized work will not be covered by the Warranty.

6.3 BLOCK DIAGRAM DISCUSSION

6.3A INTRODUCTION

The discussion that follows is keyed to Figure VI-1. As can be seen by referring to the figure, the Mainframe and two Processor Modules are delineated by dashed lines to indicate the physical location of any given circuit. Referring to the figure, note that most of the timing circuitry and all of the output-channel signal processing circuitry is located in the Mainframe. The Processor Modules contain the input-channel signal processing circuitry and the remainder of the timing circuitry. For a more detailed look at the circuits, the reader is referred to the Schematics and Parts Location Diagrams in Section VII.

6.3B MAINFRAME TIMING CIRCUITS

Aperture Delay

The mainframe timing circuits provide the triggering, aperture delay, and scan control functions. When the instrument is operating in the External Trigger mode (most common mode of operation), an externally derived trigger applied to the External Trigger Input connector is routed through contacts of the External Trigger pushbutton switch to the Level Detector circuit. Here the trigger pulse is compared with a voltage from the Trigger Level control so that triggering at any amplitude point on the trigger signal can be accomplished. The Slope switch that follows allows the transition coincident with either the positive or negative slope of the input trigger to be applied to the next stage. From there the signal is routed through contacts of the Internal Trigger pushbutton switch to the Delay Range Frame Generator. On receipt of the trigger, this circuit initiates a Delay Range Frame pulse, which has many functions. First, and most importantly, its leading edge switches on the following current source to start the Aperture Delay Ramp. Ramping current as determined by the setting of the Aperture Delay Range switch develops a linear ramp on the ramping capacitor(s). This ramp is buffered by a gain-of-one operational amplifier, the output of which is applied to a comparator. The comparator output in turn is fed back to the Delay Range Frame Generator to effect reset when the ramp reaches its final value. The Delay Range Frame Generator then terminates the frame pulse, switching the current source off. The current source output switches to a low-impedance 0 V level, and the ramping capacitors quickly discharge, resetting the ramp back to zero. Thus each trigger initiates a Delay Range Frame equal in duration to the Aperture Delay Ramp. The ramp duration in turn depends on the setting of the Aperture Delay Range switch. In the Internal Trigger mode, no externally derived triggers are required. Aperture Delay ramps follow one another as rapidly as possible.

Besides the aforementioned function of initiating the Aperture Delay Ramp, the Delay Range Frame is applied to the Model 163 to enable either the

Signal Sampling Gate or the Baseline Sampling Gate (more about this later). Additionally, it is applied to the Trigger Light circuitry so that the TRIGGERED light flashes each time the instrument is triggered. The monostable that precedes the Light Driver assures that the light will remain on long enough to be noticed, even with a very short aperture delay. In units equipped with the Digital Storage Option, the trailing edge of the Aperture Delay Frame triggers the digital storage ENCODE generator. Note that the Delay Range Frame is combined with the Digital ENCODE command to produce a STORE GATE signal. It is this signal that causes the output of the Digital Storage Unit to appear at the Mainframe output when neither an ENCODE nor a Delay Ramp is in progress. (For the sake of simplicity, only the digital storage circuitry associated with the Model 164 is indicated in the diagram. The digital storage circuitry is actually "dual" and operates in an analogous manner with the Model 163 as well.)

The Delay Range Frame is also applied to the Overlap Detect circuit in the M164. A pulse derived from the Aperture Gate Pulse is also applied to the Overlap Detect circuit. Should an Aperture Gate Pulse initiated during a given Delay Range Frame extend beyond the end of the Frame, the Overlap Detect circuit will cause the OVERLAP light to glow. At the same time, a trigger holdoff signal is fed back to the Delay Range Frame Generator to prevent another Delay Range Frame from being triggered while the overlap condition persists; the instrument does not become trigger-sensitive again until the Aperture Gate Pulse in progress ends.

Note that the Delay Range Frame input to the Model 163 acts through a gate to trigger a 100 μs monostable, and that the output of this monostable in turn is fed back to the Trigger Holdoff Input of the Delay Range Frame Generator. By incorporating this monostable into the holdoff feedback loop in this manner, triggering faster than 10 kHz is prohibited when a Model 163 Processor Module is used. This limit is dictated by the recovery-time requirements of the Sampling Heads used with the M163.

Scan Circuits

In scanned operation, these circuits determine the position of the aperture opening with respect to the trigger. To do this, a ramp is generated whose duration can be set from .01 s to 10^5 s according to the setting of the Scan Time controls. Note from the block diagram that the ramp is produced by an operational amplifier connected as an integrator. A voltage applied through a field-effect transistor switch to a resistor in series with the integrator input sets the ramping current. The Scan Time switch setting determines the value of the input resistor and also the magnitude of the feedback capacitance around the operational amplifier. The ramp produced by the integrator is routed through some switch contacts to two summing amplifiers where it is added to the dc voltages picked off the Initial Delay A and Initial Delay B potentiometers. The ramp is also fed back to the Scan Control Logic circuits. These circuits, in addition to controlling the field-effect-transistor switch at the input to the integrator, provide the SCAN RESET, SINGLE SCAN, and STOP SCAN functions. Also, there are Scan Control Logic outputs that drive the Pen Lift Driver and Scope Blanking circuits.

Before the Scan Ramp is applied to the Summing Amplifiers, it passes through contacts of the INT/EXT, A SCAN, and B SCAN switches. When the EXT pushbutton is depressed, the output of the internal Scan Ramp Generator is dead-ended at the switch, and it is the externally derived control voltage applied to the SCAN IN/OUT connector, together with the % Initial Delay settings, that determines the position of the aperture opening. When the A SCAN pushbutton is depressed, the Scan Ramp is applied to the Channel A Summing Amplifier. Similarly, when the B SCAN pushbutton is depressed, the Scan Ramp is applied to the Channel B Summing Amplifier. Should either of these two buttons not be depressed, the ramp is not applied to the corresponding amplifier. Instead, the amplifier input is grounded.

The time position of the aperture opening is expressed as a percentage of the selected Aperture Delay Range. Each scan ramp can shift the aperture opening over a range of 0% to 100% of the Aperture Delay Range. Similarly, the % INITIAL DELAY A and % INITIAL DELAY B dials can also position the aperture opening over a range of 0% to 100% of the Aperture Delay Range. (**NOTE:** The lower limit for aperture position is actually about 3%; minimum delay of 75 ns always applies.) Inasmuch as both the Scan Ramp and the voltages picked off the potentiometers are applied to the Summing Amplifiers, the output of each amplifier equals the *sum* of the Scan Ramp and the corresponding dialed voltage, and it is this sum that determines when the aperture opens. For example, if the Initial Delay A dial is set to 40%, and at the moment of interest the Scan Ramp is at 30% of maximum, the output of the Channel A Summing Amplifier will be a voltage that will position the leading edge of the aperture opening at 70% of the selected Aperture Delay Range.

The output of each of the Summing Amplifiers is fed back through a Scan Maximum Detect circuit to the Scan Control Logic circuitry. When the output of either Summing Amplifier reaches the level corresponding to 100% delay, the Scan Control Logic ends the ramp. The ramp will either reset and begin again (SINGLE pushbutton released), or hold at the point reached (SINGLE pushbutton depressed). It is important to note that the *ramp*

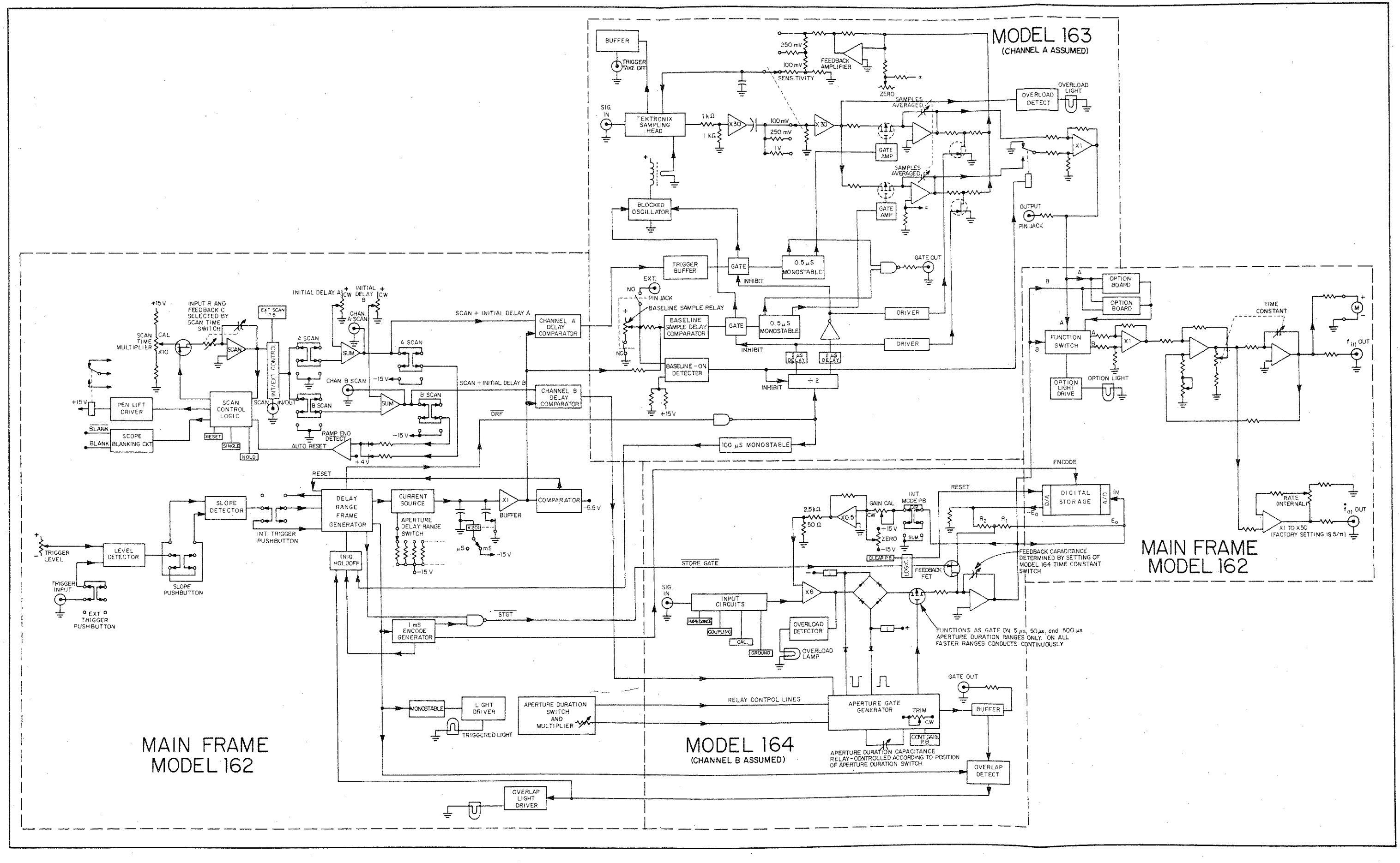


Figure VI-1. MODEL 162 SYSTEM BLOCK DIAGRAM

does not necessarily reach its maximum. For example, if the dialed initial delay were 40%, the ramp would terminate when it reached 60% of its maximum value; ramping terminates when the sum voltage reaches 100%.

Two comparators follow the Summing Amplifiers. The sum of the Scan and the Initial Delay A voltage is applied to the Channel A Delay Comparator. The sum of the Scan and the Initial Delay B voltage is applied to the Channel B Delay Comparator. Both Comparators have as a second input the Aperture Delay Ramp. Recall that each time the instrument is triggered, one Aperture Delay Ramp is produced. The Aperture Delay Ramp voltage applied to each comparator rises linearly and crosses over the sum voltage applied to the other input. When the crossover occurs, a Comparator output is generated. The time position of this output will depend on the sum voltage into the comparator, and can vary from 0% to 100% of the selected Aperture Delay Range. Assuming a Scan Ramp is in progress, the time position of the comparator output transition will occur slightly later with each successive repetition of the Aperture Delay Ramp. Thus the Comparator output is "scanned" over the selected Aperture Delay Range. The comparator outputs are routed to the corresponding Processor Modules to trigger the Aperture Gate Generator circuits, thereby determining how long after each trigger the aperture opening occurs. Note that the duration of each aperture opening is determined by circuits in the Processor Modules. Also note that the Aperture Gate Generator circuits do not respond to the comparator output reset transitions that occur as each Aperture Delay Ramp resets.

6.3C MODEL 164 TIMING CIRCUITS

The output of the Channel B Delay Comparator is applied to the input of the Model 164 Aperture Gate Generator. (The other Comparator could also drive the Model 164; it's solely a matter of module position.) The Aperture Gate Generator is a pulse generator that provides one pulse out for each input trigger (Comparator output). The duration of the pulse is set by the Aperture Duration controls, which are located on the front panel of the mainframe. The Aperture Gate Generator pulse output (or buffered equivalents thereof) is used in many ways. First, it serves to control the M164 Signal Channel Gates. Note that there are two gates connected in series, a four-diode "fast" gate, and a field-effect transistor "low-leakage" gate. The FET gate switches on the three slowest Aperture Duration Ranges only. On the faster ranges it conducts continuously. The bridge gate, which is capable of extremely fast switching times, switches on all Aperture Duration Ranges. Although the response time of the diode bridge is much faster than that of the FET gate, its leakage characteristics are not as good. Hence the use of the FET to achieve superior holding time on the slower ranges. Another output of the Aperture Gate Generator is available at the front-panel GATE OUT connector, and yet another is applied to the Model 164 Overlap Detect circuit, which functions as described previously.

6.3D MODEL 163 TIMING CIRCUITS

The timing relationships in the Model 163 are necessarily complex due to the baseline sampling and averaging features provided in this module. For each input trigger to the Model 162, either of two separate timing sequences are set in motion at the Model 163. The first, or signal-sampling sequence, is analogous to that in the Model 164. Note that the output of the Channel A Delay Comparator (it could as well be the Channel B Delay Comparator) is routed to the Model 163 and applied to a Trigger Buffer circuit. The buffer output in turn is applied to a gate, which also has an Inhibit input. In a signal-sampling sequence, no inhibit signal is applied, and gate outputs trigger the 0.5 μs Signal Monostable and also the Blocked Oscillator that causes the Sampling Head to take one sample. Outputs of the monostable control the Signal Channel Gated Integrator, and provide one input to the Gate circuit that generates the front-panel GATE OUT signal. The sample taken at the Sampling Head is ac coupled out of the Sampling Head, amplified, and applied to the Gated Integrator controlled by the earlier mentioned Signal Monostable.

A baseline-sampling sequence is similar, the main difference being that, whereas the timing of the sample in a signal-sampling sequence is coincident with the output of one of the two mainframe Delay Comparators, the timing of the sample in a baseline-sampling sequence is coincident with the output of a Comparator located in the Model 163. Like the mainframe comparators, this one has the Aperture Delay Ramp as one of its inputs. However, whereas the mainframe comparators have the sum of the scan plus dialed delay for their second input, the voltage determined by the setting of the front-panel Baseline Sample Delay Control acts as the second input to the Baseline Sample Comparator. Thus, by adjusting the Baseline Sample Delay control, the position of the baseline sample can be located anywhere over the Aperture Delay Interval.

The output of the Baseline Sample Delay Comparator is applied to a gate having an inhibit input like that of the corresponding Signal Channel gate. This gate, when not inhibited, passes the Comparator output to trigger both the 0.5 μs Baseline Monostable and the Blocked Oscillator. The Baseline Channel Monostable directly controls the Gated Integrator in the Baseline Channel, and also provides an output to the Gate which produces the front-panel GATE OUT signal. The sample taken at the Sampling Head is ac coupled out

of the Sampling Head, amplified, and applied to the Gated Integrator controlled by the Baseline Sampling Monostable.

Each time the M162 is triggered, a divide-by-two circuit triggered by an output of the Delay Range Frame Generator determines whether a given cycle will be a signal-sampling sequence or a baseline-sampling sequence. Note that the divide-by-two circuit has two outputs, each of which is delayed and then applied to the Inhibit input of the corresponding gate. At any time, one gate or the other is inhibited. Thus, during a given cycle, only one of the two monostables can be triggered. When operating in the baseline-sampling mode, the divide-by-two circuit alternately inhibits first one gate and then the other, with the result that signal-sampling sequences and baseline-sampling sequences alternate. When not operating in the Baseline Sampling mode, the divide-by-two circuit is itself inhibited in such a way that the gate following the Baseline Sample Delay Comparator is continuously inhibited while that following the Trigger Buffer is continuously on. The result is that every trigger initiates a Signal Sampling sequence.

Note that the Divide-by-Two circuit also controls two shunt FET gates, one at the output of each Gated Integrator. During a signal-sampling sequence, the output of the Baseline Integrator is shunted to ground and only the output of the Signal Integrator is applied to the feedback loop. During a baseline-sampling sequence, the output of the Signal Integrator is shunted to ground and only the output of the Baseline Integrator is applied to the feedback loop.

Not yet discussed is the Baseline-On Detector that monitors the voltage picked off the Baseline Sample Delay control and compares it with a small dc voltage. When the control is fully counterclockwise, the output of the detector supplies no current to the relay in the input circuits of the final M163 Amplifier. As a result, this amplifier "sees" the output of the Signal Channel Gated Integrator with respect to ground. With control settings other than fully counterclockwise, that is, with Baseline Sampling selected, current is supplied to the relay and it energizes, changing the input circuit configuration of the final amplifier. Instead of seeing the Signal Channel Integrator output with respect to ground, the amplifier sees the Signal Channel Integrator output with respect to the Baseline Channel Integrator output. Since dc drifts will affect both channels equally, they will not degrade instrument accuracy when operating in the Baseline Sampling mode. The Baseline-On Detector also inhibits the $\div 2$ circuit as explained previously whenever baseline sampling is *not* selected.

Note that the input Baseline Sample Delay Comparator can also be taken from an external source. The switching for this function is illustrated in the block diagram. When external control of the baseline sample position is selected, the ground supplied to the Baseline Delay potentiometer is disconnected and the EXT pin jack is routed to the Comparator input.

The M163 final amplifier drives the M163 front-panel OUTPUT pin jack, and is also routed to the mainframe for final processing.

6.3E SIGNAL PROCESSING

Model 164

The signal applied to the Signal Input connector is routed directly to the Input Coupling circuits. These circuits, which are actuated by front-panel pushbutton switches, allow the operator to choose ac or dc coupling, an input impedance of 1 MΩ or 50 Ω, or, if desired, to apply either ground or a full-scale calibrate level to the following gain-of-six amplifier. The amplifier drives the Gated Integrator, which has two gates in series with its input, a diode-bridge gate for speed, and a FET gate for low leakage with long aperture times. Because of the gating action, the Integrator only sees the signal for the selected aperture time after each trigger. The voltage at the output of the Integrator can only change over the gate-open intervals. For the entire time between apertures, the voltage at the output of the Integrator "holds". If the Model 164 is being operated in the EXP averaging mode, the Integrator output is applied to a $\times 0.5$ amplifier that feeds back to the gain-of-six preamplifier. However, due to the 50:1 attenuator at the output of the feedback amplifier, there is only 1% effective feedback, establishing the overall gain from the input of the gain-of-five to the output of the Gated Integrator at one hundred. Thus, the feedback has the effect of making the Integrator output asymptotically approach 100 E_i, where E_i is the signal amplitude at the sampled point. The circuit response is described by the characteristic RC charging curve but stretched in time by the duty factor. The selected Time Constant sets the RC product, with the involved components being the capacitance around the Gated Integrator and the resistance in series with the summing junction, including that of the gates when conducting. Because of loop-gain considerations (factor of 100 attenuation in the feedback loop together with a $\times 6$ gain in the summing line), the actual RC is about a factor of 17 less than the selected Time Constant.

If the Model 164 is operated in the SUM averaging mode, the feedback loop is broken and the circuit functions as a true integrator. A given amount of input causes a specific rate of change at the output. The duty factor and selected Time Constant determine the rate of change for any given input

level. In other words,, with an input, E_i, applied, the output does not asymptotically approach 100 E_i, but rather rises linearly until the limits are reached or the input signal changes.

Note that there is a second FET connected to the summing point of the Gated Integrator, one that extends from the summing point to the junction of two equal resistors, R1 and R2 in the block diagram. In units not equipped with the Digital Storage Option, this FET only conducts when the CLEAR pushbutton is depressed. When this is done, the FET forms a discharge path for the integrating capacitor, allowing it to be quickly discharged.

In units that are equipped with the Digital Storage Option, this second or "feedback" FET has the additional function of providing the means for connecting the output of the Digital Storage Circuitry to the summing point of the Gated Integrator. The basic timing sequence of the Digital Storage function follows.

(1) The instrument is triggered, initiating a Delay Range Frame which, in addition to its earlier described uses, is applied to the gate that controls the Feedback FET. This FET, when conducting (it does not conduct during a Delay Range Frame) connects the junction of the Digital Storage and Gated Integrator outputs to the summing junction of the Gated Integrator. As a result of the control exercised by the Delay Range Frame, the Feedback FET is *prevented* from conducting for the duration of the Delay Range Frame, and the Gated Integrator is not affected by the Digital Storage Unit over the Delay Range Frame interval.

(2) At some time during the Delay Range Frame, the aperture opens, and the voltage at the output of the Gated Integrator changes as appropriate for the input signal level and operating parameters. As soon as the aperture closes, the Gated Integrator resumes holding in the usual manner.

(3) The trailing edge of the Delay Range Frame triggers the 1 ms ENCODE generator. The encode generator output has two functions. First, it is applied to the gate that controls the Feedback FET, thereby preventing the FET from conducting during the Encode sequence. Second, it is applied to the Digital Storage Unit, which then makes an analog-to-digital conversion of E_o, the output of the Gated Integrator. The digital information is stored and reconverted to analog form. The analog voltage, which is equal to E_o but of opposite polarity, is made available at the output of the Digital Storage Circuitry.

(4) At the end of the 1 ms Encode command, by which time the analog-to-digital-to-analog conversion is complete, the gate controlling the Feedback FET switches and the Feedback FET conducts, thereby connecting the junction of R1 and R2 to the summing junction of the Gated Integrator. E_o is applied to R1 and $-E_o$ to R2. Because these resistors are equal, there is 0 V at their junction. Should the output of the Gated Integrator tend to drift, the voltage at the junction of R1 and R2 will become non-zero (except for 1% of full scale maximum short-term drift, the voltage at R2 remains $-E_o$ indefinitely because it is derived from the stored digital data), developing an input to the Gated Integrator of the polarity necessary to correct the output back to its former value. The Feedback FET continues to conduct until the instrument is triggered again, giving, in effect, an infinite hold time.

The CLEAR pushbutton has an additional function if the Digital Storage feature is being used. Besides establishing a discharge path for the Integrating Capacitor via the Feedback FET, it also resets the Digital Storage Circuitry to 0 V out.

In any case, whether or not the unit is equipped with the Digital Storage Option, the Gated Integrator output signal is routed to the Mainframe for additional processing as explained further on.

Model 163

Because of its baseline sampling capability, the Model 163 has more complicated signal processing circuitry than does the Model 164. Referring to the block diagram, note that the input signal is applied directly to the Sampling Head. The aperture circuitry, which is internal to the Sampling Head, is controlled by the Blocked Oscillator as described previously. Each time a sample is taken, either of the signal or of the baseline, the information gathered is coupled out of the Sampling Head to a $\times 0.5$ attenuator and from there to an amplifier with a fixed gain of $\times 30$. This amplifier is followed by an attenuator controlled by the Model 163 front-panel Input Range switch. Another $\times 30$ amplifier follows, and then a pair of Gated Integrators. These integrators stretch and hold the information out of the Sampling Head. The upper gated integrator is only activated during a signal-sampling sequence. The lower is only activated during a baseline-sampling sequence. The output of the Signal Sampling Integrator asymptotically approaches the average level of the input signal at the sampled point. Similarly, the output of the Baseline Sampling Integrator asymptotically approaches the average level of the baseline at the sampled baseline point. If the baseline sampling

feature is turned off, only signal samples are taken. The magnitude of the capacitance around each of the integrators is set by the Model 163 SAMPLES AVERAGED switch.

Note that a feedback loop similar to that in the Model 164 is employed. The feedback loop consists of an amplifier and an attenuator. This attenuator operates in conjunction with the Input Range switch as required to maintain the loop gain constant. Depending on whether the sequence in question is a signal-sampling sequence or a baseline-sampling sequence, the output of one Gated Integrator or the other is fed back to the Sampling Head to complete the loop. Note that there is a shunt FET ahead of the feedback point at the output of each integrator. One or the other of these FET's always conducts. Thus, when a signal-sampling cycle is in progress, the shunt gate at the output of the Baseline Sampling Integrator is fed back. The reverse is true during a baseline-sampling cycle. It is important to realize that these shunt gates are in an attenuator network, that is, they do not directly ground the output of the integrators. Thus, even when a given shunt FET is conducting, the output of the preceding integrator is not forced to 0 V, but rather continues to hold at the proper level. Only feedback signal is grounded.

The direct outputs of the two integrators are applied to a differential amplifier which provides the Model 163 signal output. When using the baseline sampling feature, the Model 163 output is a voltage proportional to the difference between the average amplitude at the sampled signal point and the average baseline level at the sampled baseline point. If baseline sampling is not used, the output is simply the average amplitude at the sampled signal point relative to ground.

Although it isn't indicated in the block diagram, the Digital Storage Option is "dual", that is, there are two sets of Digital Storage Circuitry, one for each channel, and both function as described for the Model 164. If operated in conjunction with a Model 163, the Digital Storage Circuitry only affects the Signal Sampling Integrator. The hold time of the Baseline Sampling Integrator remains the same. As a result, one cannot use the baseline sampling and digital storage techniques simultaneously.

Mainframe

The output signal from each of the Processor Modules is applied to the mainframe Function switch. This switch allows the operator to select the final mode of signal processing. Assuming none of the options are selected, either the A Channel Output signal, the B Channel Output signal, or the difference signal will be applied to the following amplifier. If one of the options is selected, other circuits, not indicated in the block diagram, come into play to perform the desired function.

In any case, the signal out of the Function switch is applied to a series of amplifiers that establish The net gain from the output of the Processor Module to the f(t) Output at $\times 1$. The f(t) signal is also developed in these amplifiers, and is routed through a final buffer to the f(t) Output connector. The gain to the f(t) Output depends on the setting of the inner knob of the Time Constant switch (inner knob affects time constant also, as indicated) and on the setting of the internal RATE adjustment. The transform functions are given in the specifications.

6.4 MAINFRAME TROUBLESHOOTING PROCEDURE

6.4A INTRODUCTION

Troubleshooting the mainframe is accomplished by making voltage and/or waveform checks at critical points. Generally speaking, the operator will be searching for gross discrepancies between the observed waveform or voltage and that indicated in the following procedure. There is some normal variation from instrument to instrument, and small differences between indicated and actual measurements are to be expected. Once the malfunctioning circuit has been identified, additional troubleshooting as decided by the operator can be performed to locate the specific faulty component. In the case of instruments still in warranty, care must be taken that no damage is done in troubleshooting as such damage would not be covered by the Warranty.

6.4B EQUIPMENT REQUIRED

(1) High-speed oscilloscope with dual-trace capabilities—TEKTRONIX 7000 series mainframe with appropriate plug-in modules.

(2) Fast square-wave source—E. H. Model G710.

(3) General purpose digital voltmeter—FAIRCHILD Model 7000A.

(4) For convenience in making contact with some of the test points, it will prove useful to have some of the special test probes specifically designed for the purpose. Two particularly well suited probes are the Rye Industries KLEP 30 "clip/probe" and the Pomona "grabber" plunger action Mini-Test clip.

6.4C PRELIMINARY STEPS

(1) With the power off, remove the Processor Modules from the mainframe.

(2) Remove the top cover (secured by two screws on the underside of the top-cover overhang at the rear of the instrument).

(3) Note whether the unit is equipped with digital storage. If it is, the digital storage circuit board will have to be removed to give access to the check points on the upper mainframe circuit board. **NOTE:** If the unit is equipped with any of the other options, the corresponding circuit boards can be left in.

(4) Note that the upper circuit board is hinged on the left side (front view) so that it can be lifted up out of the way to give access to the lower board. Remove the four screws that secure the upper board. Then rotate it upwards as far as it will go and tie it in that position with some string.

(5) Check the line fuse, located at the rear panel. Also check the two fuses mounted on the lower circuit board. If any of these fuses are blown, replace them and turn the power back on. If the fuse "holds", continue the procedure. If it blows, there is a short circuit somewhere in the mainframe that will have to be located and repaired before any further checking can be done. Good possibilities in the case of fuse failure are the electrolytic power-supply filter capacitors and the rectifiers.

(6) Set the controls as follows.

Trigger Mode pushbuttons: EXT depressed; all others released
Scan Select pushbuttons: "A" depressed; all others released
% Initial A and B: both to 10%
Aperture Delay Range: 1 μSEC
Aperture Duration: setting immaterial
Scan Time: 10 SEC and CAL
Function: A
Time Constant: 0.1 mSEC and CAL

6.4D POWER SUPPLY CHECKS

(1) Connect the DVM to the positive end of capacitor C265. The indicated voltage should be +15 V ±0.2 V.

(2) Connect the DVM to the negative end of capacitor C266. The indicated voltage should be −15 V ±0.2 V.

(3) Connect the DVM to the positive end of capacitor C255. The indicated voltage should be +5 V ±0.2 V. U209 is the upper board +5 V regulator.

(4) Connect the DVM to the positive end of capacitor C110A. The indicated voltage should be +5 V ±0.2 V. U105A is the lower board +5 V regulator.

(5) Connect the DVM to the positive end of capacitor C262. The indicated voltage should be +50 V ±2 V.

(6) Connect the DVM to the negative end of capacitor C258. The indicated voltage should be −50 V ±2 V.

If all voltages are within tolerance, go on to step 6.4E. If any voltage is in error, it will be necessary to locate and repair the malfunctioning circuit before any further checks can be made. Most of the power supply circuits are located on the upper board. The corresponding schematic is on page VII-13. In troubleshooting the regulators, bear in mind that the +15 V regulated level acts as the reference for the −15 V regulator and for the +50 V regulator. The −15 V regulated level acts as the reference for the −50 V regulator.

6.4E TRIGGER CHECKS

(1) Disconnect the wire which connects to quick-disconnect terminal P138 on the lower board. Tape the terminal at the end of the wire so that it cannot accidentally short to another circuit element.

(2) Connect a 250 kHz 0-to-1 V positive square wave to the Trigger INPUT connector. **NOTE:** The front-panel TRIGGERED lamp will not glow because the lamp drive circuit is triggered by a signal taken from beyond P138, the disconnected terminal.

(3) Monitor P138 with the oscilloscope. Then adjust the front-panel TRIGGER LEVEL control until proper triggering is obtained as evidenced by a 250 kHz square wave at P138. The lower level should be nominally −0.6 V. The upper should be nominally +3 V. If this signal is as indicated, the basic trigger circuitry is functioning normally. If the indicated waveform is not obtained, then detailed checking will be required. Note from the schematic on page VII-16 that the circuitry can be divided into three subsections. The first subsection is the Level Detector, and includes that circuitry from the Trigger INPUT connector to TP108A, a convenient monitoring point to determine whether the Level Detector circuitry is functioning normally. With a 250 kHz input, and with the TRIGGER LEVEL control properly adjusted, the signal at TP108 should be a square wave switching symmetrically about ground. The actual levels will depend on the input amplitude and the wave shape can vary considerably according to the TRIGGER LEVEL setting. Transistors Q105A and

Q106A, together with their associated components, constitute the Slope Detector. The output of this circuit is monitored at the collector of Q105A, where the observed signal should be a 500 mV pk-pk square wave with its lower level at about −6 V. Q107A is the output transistor. Its output is monitored at P138, as described at the beginning of the paragraph.

(4) If the signal at P138 is as indicated above, reconnect to P138 the wire removed earlier. **NOTE:** If the Delay Range Ramp and Delay Range Frame circuits are functioning properly, along with the Triggered Lamp Driver circuit, the TRIGGERED lamp will commence to glow when the wire is reconnected. These circuits are specifically checked in later steps.

6.4F DELAY RANGE FRAME AND DELAY RANGE RAMP GENERATOR CIRCUITS

The underlying assumption at this point is that the power supply and trigger circuits have given normal indications.

(1) With the 250 kHz trigger signal still applied, monitor the signal at TP207. The observed signal should be a 250 kHz square wave switching between nominally −0.6 V and +3 V. There should be a positive-going 100 ns wide pedestal with an amplitude of 0.2 V to 0.3 V located about one microsecond after the negative-going transition of the square wave. This "pedestal" marks the 100 ns trigger holdoff that takes place at the end of the Aperture Delay Range to allow the Aperture Delay Frame circuits time to reset. If the trigger input waveform were such as to cause this holdoff to be located on the upper level of the TP207 waveform, it would appear as a 100 ns wide "notch" having its lower level at nominally 0.3 V.

(2) Monitor the signal at TP203. With the Aperture Delay Range controls set to 1 μSEC, one should observe a logic 1 (nominally +3.5 V) pedestal. It should begin coincident with the negative-going edge at TP207, and end (return to nominally 0 V) after 1 μs plus a few percent. If this signal is as indicated, one can assume that several inter-related circuits, all schematically portrayed on page VII-11, are working normally. They are: (i) the two gates of U204 that are arranged in a flip-flop configuration and which have the Delay Range Frame (inverted) as their output (pin 12 of U204), (ii) the Ramp Generator Reset circuit, Q205-Q206, (iii) the Ramping Current Control circuit, Q202 and Q204, (iv) the Ramping Current Source, U201, Q203 and Q201, (v) the Ramp Buffer, the circuitry between TP201 and TP204, (vi) the End-of-Ramp Detect circuit, Q215, Q216 and Q217, and (vii) the Trigger Holdoff circuit, Q218 and Q212. Troubles in any of these circuits could prevent the signal at TP203 from being as indicated. If the signal is not as indicated, the following hints and discussion of how these circuits function may prove helpful in further isolating the problem.

(a) The control loop begins and ends with the U204 flip-flop. Prior to a trigger being received (negative transition coupled through C222), pin 6 will be down and pin 12 up. Pins 3, 4 and 5 should all be up. Pins 1 and 2 should be down, and pin 13 up. If these quiescent conditions are not as described, either U204 or one of the circuits affecting an input of the flip-flop is defective. Note that the pin 13 input is taken from the End-of-Ramp Detect circuit, Q215, Q216 and Q217. This circuit monitors the Ramp Buffer Output (TP204). Whenever the Buffer Output is more positive than about −6 V, the End-of-Ramp Detect circuit's output will be at logic 1. Thus, in the quiescent state, one would expect TP204 to be at 0 V, and, as a result, pin 13 of U204 to be at logic 1.

The various Trigger Holdoff inputs all act through Q212 to control the flip-flop. Normally Q212 is not conducting. When it does conduct, detected triggers (TP207) are effectively shunted to ground by Q212 and there is no trigger input to the flip-flop. Because the trigger inputs are ac-coupled through C222, a problem involving Q212 or one of its inputs would not affect the initial dc state of the flip-flop, but would instead simply make it impossible to trigger the flip-flop.

(b) The pin 12 flip-flop output is the earlier discussed Delay Range Frame. Actually, the complement of the Delay Range Frame is present at pin 12 and so is referred to as $\overline{\text{DRF}}$. When a negative transition is detected at pin 3, the flip-flop reverses state, i.e., pin 6 goes to logic 1 and pin 12 to logic 0. Pin 6 going positive turns Q206 off and Q205 on. When Q205 conducts, diodes CR201 and CR202 are biased off, unclamping the ramping capacitor C213 (capacitor C214 is only "in" when the Delay Range switch is set to "mSEC"). At the same time, the U204 pin 12 signal switches current sink Q202 off, allowing the current supplied by Q203 to flow through Q201 to the Integrating capacitor. The current magnitude is a function of the Aperture Delay Range switch setting.

(c) The ramping current causes a negative ramp to develop across C213. The gain-of-one Buffer between TP201 and TP204 buffers the ramp, and drives the comparators, one for each channel. The ramp is also applied to the End-of-Ramp Detect circuit (base of Q215).

(d) When the ramp reaches nominally −6 V, Q217 is biased into conduction, applying a logic 0 to the pin 13 input of U204. The logic 0 at pin 13 reverses the state of the flip-flop. Immediately Q205 stops conducting, clamping the Buffer input to 0 V. The Buffer output snaps back to 0 V (the ramp resets), and a logic 1 appears again at the pin 13 input of U204. Note that the pin 13 logic 0 is transient, lasting but a few nanoseconds. The logic 0 does not begin until the ramp reaches the voltage required to activate the End-of-Ramp Detect circuit. It ends as soon as the ramp-reset begins. Note also that as soon as the flip-flop resumes the quiescent state, Q202 switches on to sink the ramping current.

(3) Assuming the signal at TP203 is as indicated, that is, a logic 1 with a duration of just over a microsecond and having a repetition rate of 250 kHz, switch the Digital Storage switch (inner knob of FUNCTION switch) to the ON position. (The function to be checked does not depend on a digital storage circuit board being installed.) The repetition rate of the observed pulses will decrease to about 1 kHz, indicating that the ENCODE generator, U213 (schematic on page VII-13) is working properly, as is the ENCODE Trigger Holdoff circuit (R260 input to Q212). If the indicated behavior is observed, turn the Digital Storage OFF before proceeding.

(4) Monitor the signal at pin 8 of U205, the output of the Trigger Holdoff Monostable. One should observe 100 ns logic 1 pulses at a 250 kHz repetition rate. In External Trigger operation, these pulses are applied to the R268 input of Q212 to render the U204 flip-flop trigger insensitive long enough for the Delay Range Ramp to fully reset.

(5) Set the Delay Range to 1 mSEC. The duration of the logic 1 pulses at pin 8 of U205 will increase to 100 μs as a result of capacitor C220 being switched into the monostable time-constant circuitry. The interval between pulses will increase to 1 ms; the output of Q217 acting through pin 13 of U204 keeps the flip-flop trigger insensitive until the end of the ramp (1 ms) in progress.

(6) If the indicated behavior was observed in all of the preceding checks, one can assume that the Delay Range Frame and Ramp Generator circuits are working correctly. There are some additional checks that could be made. One could monitor TP204 to be sure there are no oscillations or noise superimposed on the ramp. Also, one could run through all possible Delay Range settings (other than SEPC) to ascertain that there is no problem with a specific setting. If such a problem is observed, check the switched component(s) associated with the switch position in question. One further point, if all checks to this point are positive, but the TRIGGERED lamp does not glow, the problem is most likely with the TRIGGERED lamp itself, or with the associated drive circuit (U203, page VII-11) which is triggered by the negative (leading) edge of the Delay Range Frame (inverted) coupled through C216 to pin 2 of U203.

6.4G DELAY RANGE RAMP COMPARATORS AND ASSOCIATED GATES

(1) Set the Delay Range back to 1 μSEC (leave trigger input frequency at 250 kHz).

(2) Referring to the schematic on page VII-13, note the Comparator circuit in the upper right-hand corner. There are actually two such circuits, one for each channel. Because they are identical, only one is shown on the schematic. Each component has two component numbers, one applying to the Channel A Comparator circuit, the other to the Channel B Comparator.

In any case, monitor the signal at TP212, the output of the Channel A Comparator. One should observe a logic 0 "pulse" (baseline at nominally +3.5 V) at 250 kHz and having a duration of nominally 0.9 μs (% Initial Delay dial set to 10%). If the dial setting is made higher, the duration of the logic 0 will become *shorter*, linearly tracking the dial setting. With the dial fully clockwise, the logic 0 portions of the displayed waveform will be reduced to a couple tenths of a microsecond. Note that if the dial is rotated fully counterclockwise, the circuit may stop working altogether, in which case the voltage at TP212 would simply remain at the upper level.

It may prove convenient to trigger the oscilloscope with the positive going edge of the Delay Range Frame (available at TP203). With the oscilloscope triggered in this manner, one could observe that, whereas the position of the TP212 signal's leading (negative going) edge varies directly with the setting of the %

Initial Delay dial, the position of the trailing edge remains fixed and coincident with the trailing (negative going) edge of the Delay Range Frame.

(3) Transfer the oscilloscope to TP213, the output of the Channel B Comparator. The behavior should be exactly the same as for the Channel A Comparator described in the preceding step, except that in this case the % Initial Delay B dial will control the signal. When the checks are completed, leave both delay dials set to 50%.

(4) With the oscilloscope triggered from the leading edge of the Delay Range Frame (positive going edge of the TP203 signal), monitor the signal at pin 10 of U206. (**NOTE:** TP205, a test point, should be in common with pin 10 of U206. If it is, use it as the monitor point. In some units TP205 is returned to pin 13 of U206 and so cannot be used to check the signal of interest.) The observed signal should be a positive spike a *few nanoseconds* in width and located at about 0.5 μs with respect to the leading edge of the Delay Range Frame. This pulse can be positioned anywhere on the Delay Range Frame (except for the first few % where the Comparators may stop working) by means of the % Initial Delay dial. This pulse is the actual trigger supplied to whatever Processor Module is in the Channel A position. If the signal is as indicated, one can assume that the Channel A Post-Comparator Trigger circuit (one gate of U205 and one of U206) is working properly.

(5) Transfer the oscilloscope to TP206. The signal should be the same as at pin 10 of U206, except that in this case the % Initial Delay B dial will determine the pulse position.

This completes the checks of the Delay Range Ramp Comparators and of the Post-Comparator Trigger circuits. Figure VI-2, a timing diagram for the circuits discussed so far, may prove helpful in isolating the malfunctioning circuit.

6.4H SCAN-RAMP GENERATOR AND ASSOCIATED CIRCUITS

Procedure

(1) Set the Scan Time to 0.01 SEC and CAL. The "A" Scan Select pushbutton should be depressed and all of the other Scan pushbuttons released. The signal previously applied to the Trigger Input connector should be disconnected and all of the Trigger pushbuttons except EXT should be in the released position. The % Initial Delay A dial should be fully counterclockwise.

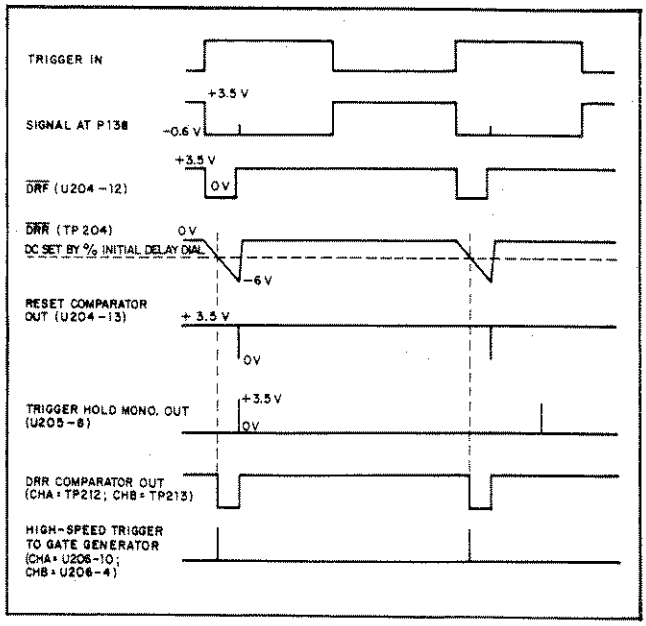


Figure VI-2. TIMING DIAGRAM FOR MAINFRAME "FAST" CIRCUITS

(2) On the lower board, monitor the signal at TP105, the output of the Scan Ramp Generator. (**NOTE:** "100" series components are located on the lower board.) The observed signal should be a negative-going repetitive ramp referenced to 0 V and reaching about −5.5 V. Its duration should be about 10 ms. This same signal should be available at the rear-panel SCAN IN/OUT connector but with opposite polarity. If these signals are absent or improper, proceed to SCAN FAULT ANALYSIS.

Note that one could try setting the SCAN TIME to other positions. The duration of the observed ramp should always exceed that selected by a few percent. It will prove impractical to check the longer scan times in this manner. However, one can still monitor the ramping rate for some arbitrarily selected time. In any case, any problems associated with a specific scan time almost certainly involved one of the integrator components (R110 through R113, and C103 or C104) or the Scan Time switch itself. Leave the Scan Time set to 10 mSEC and CAL.

(3) Transfer the oscilloscope to TP106, the output of the Channel A Summing Amplifier (sums scan ramp with dialed delay voltage). The observed signal should be a zero-based, repetitive, positive-going ramp with a peak amplitude of nominally +5.5 V.

(4) Begin rotating the % Initial Delay A dial clockwise. As the dial is turned, the baseline of the observed ramp will rise (be sure scope is dc coupled) and the duration of the ramps

will become shorter. At 100% delay, the ramp will be reduced to but a few percent of its initial value. Leave the % Initial Delay A dial set fully counterclockwise.

Next release the Scan "A" pushbutton, depress the Scan "B" pushbutton, and, while monitoring TP108 with the oscilloscope, observe the effect of adjusting the % Initial Delay B dial. If proper behavior is observed for one channel but not for the other, the problem is most likely with U105 (Channel A Summing Amplifier) or U106 (Channel B Summing Amplifier), whichever is appropriate. Leave the controls set for Channel A operation (Scan "A" depressed, "B" released, both % Initial Delay dials fully counterclockwise).

(5) While monitoring TP106, press in the SINGLE pushbutton. The ramp in progress when the pushbutton is activated will go to completion, and the TP106 voltage will remain at the final ramp level reached.

(6) Release the SINGLE pushbutton. Repetitive ramping will take place again. Increase the selected Scan Time to 10 SEC and CAL. When a given ramp in progress is at about the midway point, depress the HOLD pushbutton. The voltage at TP106 should "hold" at the level reached when the pushbutton was depressed. At some convenient time, release the pushbutton. The scan will go to completion and successive scans will follow one another in the usual way.

(7) With the Scan Time still set to 10 SEC, depress the SINGLE pushbutton. The ramp in progress should go to completion and the TP106 voltage should remain at the maximum ramp level. At some convenient time, depress and hold down the Scan RESET pushbutton. The TP106 voltage will instantly go to 0 V and remain there for as long as the RESET pushbutton is held down. When the button is released, a new ramp will begin.

(8) Release the SINGLE pushbutton. Then locate relay K100. The relay should give an audible click at ten-second intervals. Contacts of this relay are used to achieve pen-lift commands (Table IV-1). Leave the Scan Time set to 0.01 SEC and CAL.

(9) Monitor the signal at the collector of Q108. This is the Scope-Blanking signal. For the duration of the scan ramp, the level at the collector of Q108 will be at nominally +50 V. At the end of each ramp, there is a momentary reset to nominally 0 V. The complement of this signal is available at the collector of Q107.

Scan Fault Analysis
(see Figure VI-3 for Scan Timing)

The preceding checks exercise most of the Scan Control circuits, and one can be reasonably confident that if the indicated results were obtained, the Scan Circuits are functioning normally. If incorrect indications were noted, further troubleshooting to narrow the problem down to the specific malfunctioning circuit may be advised. Note that the Scan and Scan Control circuits are operated in a closed dc loop, which tends to make troubleshooting difficult. The following brief description of the circuit functions and their interrelationships may prove helpful.

(1) The actual Ramp Generator consists of U101 and its associated components. The generator output is at the emitter of Q106. Note that there are two integration capacitors, C104 (always in the circuit) and C103 ("in" for the four longest scan times only). The ramping current is given by E/R, where R is the integrating resistor (R110, R111, R112, or R113, whichever is switched in), and E is the voltage applied to the integrating resistor. When Q103 conducts, ramping current is available. When Q103 does not conduct, no ramping current is supplied. Transistor Q102 acts as a shunt switch, conducting only when the ramp is reset. When Q102 conducts, it shorts out and discharges the integrating capacitor(s). When a ramp is in progress, Q102 is held in the non-conducting state.

(2) The output of the Ramp Generator is buffered by U104 and made available at the rear-panel SCAN IN/OUT connector. It is also routed through contacts of the A SCAN and B SCAN switches to Summing Amplifiers U105 and U106. At U105 it is summed with the dialed % Initial Delay B voltage. The Summing Amplifiers in turn drive the rear-panel CH A SCAN and CH B SCAN connectors. They also drive, via diodes CR111 and CR113, U103, the End-of-Scan Detect Comparator.

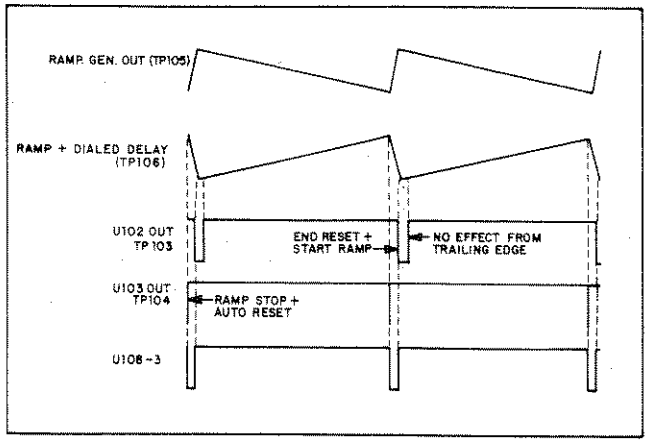


Figure VI-3. BASIC RAMP TIMING RELATIONSHIPS

(3) There are two critical comparators. They are the End-of-Ramp Detect Comparator, U103, and the Start-of-Ramp Comparator, U102. Both control the Scan Generator via the flip-flop comprising two gates of U108. The Start Comparator Output is up whenever a ramp is more than a few millivolts off its baseline, that is, its output is up almost the whole time a ramp is in progress. Only when the ramp is reset, or just getting underway, is the output of the Start Comparator down.

The End-of-Ramp Comparator monitors the sum voltage. When the scan voltage plus dialed delay of either channel reaches 100%, the output of the End-of-Ramp Comparator switches from logic 1 to logic 0. This action initiates a reset and the ramp voltage begins to fall. It need fall only a few millivolts to switch the End-of-Ramp Comparator back to its original state, that is, with the output at logic 1.

(4) The U108 flip-flop has two outputs, one at pin 3 and the other at pin 8. The pin 3 output acts through two gates to drive the base of Q105. This transistor in turn acts through Q104 to determine whether ramping current will be available. When U108-3 is up, Q103 conducts and ramping current is available. At the same time, U108-8 (down when Q108-3 is up) acts through a gate of U109 to control Q101 to the effect that Q102 is held non-conducting, allowing a ramp to be generated.

Note that the pin 3 output has two secondary functions as well. It acts through a gate of U110 to control the Blanking Signal circuitry, and it acts through a second gate of U110 to actuate the Pen Lift relay on the four slowest ramp speeds.

(5) Assume a ramp is in progress. The outputs of both U102 and U103 will be up. Pin 3 of the U108 flip-flop will be up and pin 8 down. (This state was established by a previous logic 0 at pin 2 of U108.) The pin 3 output being up will force Q103 to conduct (a necessary condition for a ramp to be in progress). The pin 8 output will force Q102 out of conduction (another necessary condition for a ramp to be in progress, that is, the integrator cannot be in a state of reset). The ramp progresses until the sum voltage applied to U103 reaches about +5.5 V, or, otherwise expressed, until the delay reaches 100%. When that happens, the output of U103 goes to logic 0, and the U108 flip-flop reverses state. Pin 3 of U108 goes to logic 0, switching Q103 off and withholding ramping current. Pin 8 of U108 goes to logic 1, switching Q102 on and resetting the ramp. The instant the ramp voltage begins to drop, U103 reverses its output again. However, this action does not reverse the U108 flip-flop, and the ramp voltage continues down to 0. When it reaches within a few millivolts of zero, the output of U102 goes to logic 0. This action does reverse the state of the U108 flip-flop, that is, pin 3 goes again to logic 1 (ramping current is again supplied) and pin 8 goes to logic 0 (reset is terminated). A new ramp begins. As soon as the ramp rises a few millivolts, the output of U102 switches back to logic 1, but this transition has no effect on the U108 flip-flop. (Only a logic 0 applied to one input or the other causes a state reversal.) This completes the basic cycle, and it will repeat indefinitely as long as either the "A" or "B" (or both) pushbutton is depressed. These basic timing relationships are illustrated in Figure VI-3.

(6) There are some secondary scan functions that might also be considered. Note that there is another flip-flop comprising two gates of U109. This flip-flop affects the Reset circuitry only. Normally (ramp circuits not in reset state) the pin 10 output of this flip-flop is at logic 1 and the pin 13 output is at logic 0. Only the pin 10 output is used and it is connected to pin 4 of U109, the output of the Reset Gate. This gate's output is also at logic 1 when the integrator is not in the reset state. If either U109-4 or U109-10 go to logic 0, Q102 is biased into conduction and the ramp generator resets. As explained previously, the U108 flip-flop initiates an automatic reset at the end of each ramp. (Note that if the Scan SINGLE pushbutton is depressed, the reset command is not applied to the Reset gate (U109-4-5-6), and no auto-reset occurs. Reset via the U109 flip-flop can be initiated either by depressing the front-panel SCAN RESET pushbutton, or by applying a logic 0 to the proper pin of the rear-panel Interface Connector, P101. Either action causes a logic 0 pulse to be generated by the monostable consisting of two gates of U107. This monostable causes the U109 flip-flop to change state. When this happens, Q102 is biased into conduction and the ramp generator resets. Note that when the ramp is reset, the output of U102 goes to logic 0. This logic 0 serves to reset the U109 flip-flop back to its original state as soon as the Scan Reset pushbutton is released (or the external command ends). Note that the end of the monostable output pulse does not reverse the flip-flop state. By controlling the reset of the flip-flop via U108-13, the reset can be maintained for as long as the Scan RESET pushbutton is depressed.

The Scan HOLD pushbutton (S114) works through a gate of U109 to switch off the ramping current when the pushbutton is depressed. Ramping current is withheld for as long as the pushbutton is held down.

This completes the description of the Scan Control circuitry. Although some of the finer points have not been discussed in detail, the information provided should be sufficient for someone experienced in solid-state logic circuitry to isolate a malfunctioning circuit.

6.4I MAINFRAME SIGNAL PROCESSING

Introduction

The mainframe signal processing circuits are straightforward, consisting of four integrated-circuit operational amplifiers and their associated components. In addition to these amplifiers, the only other active circuit is the transistor pair Q101A-Q102A that drives the OPTION light when an improper option selection has been made. With a basic understanding of how the mainframe signal processing circuits work, the experienced troubleshooter should have no difficulty, using the available test points and externally derived signals, devising simple checks that will quickly enable identification of the malfunctioning circuit. A brief description of the mainframe signal processing circuits follows. The signal-processing options are discussed in Subsection 6.5. The digital-storage option is discussed in Subsection 6.8.

Function Switch and U101A

The first active circuit is differential amplifier U101A. The FUNCTION switch determines the manner in which the Processor Module and/or option outputs are applied to this amplifier. Note from the schematic on page VII-16 that there are three switch sections. The upper section determines which signal is applied to the inverting input of the amplifier. The middle section determines which signal is applied to the non-inverting input, and the lower section controls Q101A, one of the two transistors that supplies current to the OPTIONS panel light. Note that the non-inverting input of the amplifier is returned to ground for all positions of the FUNCTION switch except A – B. The selected signal is applied to the inverting input by the switch for all positions. In the "A" position, the output of Processor Module A is applied to the inverting input. In the "B" position, the output of Processor Module B is applied to the inverting input. In the "A – B" position, the output of the Processor Module A is applied to the inverting input and the output of Processor Module B is applied to the non-inverting input. In the option positions, the output of the selected option module is connected to the inverting input. In other words, for all but the A – B position of the Function switch, the selected function is applied to the inverting input and U101A acts as a simple inverting buffer amplifier with a gain-of-one. In the A – B position, A is applied to the inverting input, B is applied to the non-inverting input, and U101A acts as a true differential amplifier. The gain is one from the output of either Processor Module to the output of U101A.

Two transistors, Q101A and Q102A, can supply current to the OPTIONS light. When no option-selection fault is present, the base of both of these transistors is returned to ground and the transistors are biased into cutoff. The return to ground for Q101A is through contacts of the Function switch and from there through a circuit on the option card. If a given option is selected with the option card plugged into either of the option board connectors, the ground path is completed. Q101A is biased off, and the OPTIONS light receives no current. If the option card is missing, the ground path will glow. Q102A works in conjunction with the Digital Storage selection switch and the Digital Storage circuitry in a similar manner. If digital storage is *not* selected, ground is supplied to Q102A via S102D, biasing the transistor off. If digital storage *is* selected, the ground path will only be completed if the digital storage board is plugged in. If it is not, Q102A will be biased into conduction via R114A and the OPTIONS light will glow.

Time Constant and Output Circuits

U102A and U103A work together to provide the mainframe time constant function and also the remaining system gain. To see how this circuit works, assume a step-function voltage, E_s, is made available at the output of U101A. Initially, pin 3 of U102A will be at ground potential (return through R118A and R119A) and pin 2 of U102A will be at virtual ground (feedback/gain network R105A-R104A). Assuming E_s is positive, the output of U102A will go negative in response, and this negative potential will be applied to U103A through one of the time constant resistors. U103A is connected as an integrator (C103A, C102A, or both provide the integrating capacitance, according to the selected time constant). The output of U103A then moves positively in response to the input step function. However, the *rate* at which it moves is determined by the selected time constant. As the output of U103A rises, this positive voltage is fed back through R121A to the pin 3 input of U102A. The voltage at pin 3 of U102A, following the RC charging curve, then rises asymptotically towards E_s, the step function level applied. After five time constants, the voltage at pin 3 of U102A will be within one percent of E_s, the output of U102A will be 0 V (as the pin 3 voltage rises towards E_s, the net differential input to U102A goes to zero). No more current will be available to integrator U103A, and the output of U103A will hold at the voltage reached. The values of R121A, R118A, and R119A are such that for a given input E_s, the voltage at the output of U103A will asymptotically approach (settle at) 10 E_s. Because the output of U103A is identically the f(t)

OUTPUT, the overall gain of the mainframe signal processing circuits is ten (inverting due to U101A). Recalling that the Processor Modules are themselves inverting, the inversion provided by U101A causes the overall system [processong module *Input* to f(t) Output] to be non-inverting.

Understand that at equilibrium, that is, five time constants or longer after applying a voltage to U101A, the output of U102A will be 0 V. In other words, the output of U102A is proportional to the rate of change of the processor module output. This pseudo-derivative signal is applied to U104A, a non-inverting amplifier that provides the f(t) OUTPUT as given in the specifications. The factory set value for the gain (k) is $5/\pi$, or nominally $\times 1.6$.

6.5 SIGNAL PROCESSING OPTIONS

6.5A INTRODUCTION

The circuits for the various signal-processing options are interposed between the outputs of the Processor Modules and the mainframe signal-processing circuits discussed in Subsection 6.4. The Processor Module A and Processor Module B outputs are applied to the selected option circuit, which then performs the selected function. The option output (always single ended) is then applied to the inverting input of U101A via the FUNCTION switch as previously described. A brief discussion of each of the modules follows. The Digital Storage Option is not involved in signal processing and so is discussed separately in Subsection 6.8.

6.5B PRODUCT OPTION (162/95)

This option gives the choice of $A \times B$ or A/B operation as selected by a slide switch on the option board. Referring to the schematic on page VII-19, note that the product option consists principally of multiplier module U9504 and its associated components. The product of the signal applied to the X_f and Y_f inputs appears at the output of the multiplier and is applied to one input of the differential amplifier. The other input of the differential amplifier is returned to Z_f. V_o is the designation for the differential amplifier output.

In multiplier operation, the B Processor Module output is applied to X_f. The multiplier output, $A \times B$, is applied to one input of the following differential amplifier (this amplifier is internal to the multiplier integrated circuit). Feedback through R9526, R9525, and R9524 interconnects the amplifier's output and "free" input, thereby setting the gain to the specified level (see specifications for transfer function). Amplifier U9503 acts as a simple output buffer.

Operation in the ratio mode is more complex. In this mode, only the B Processor Module output is applied to one of the multiplier inputs (X_f). The A Processor module output is applied to the "free" input of the differential amplifier. In other words, the differential amplifier has as one input the multiplier output signal, and for the other input the output of the A Processor Module. Because of the feedback from the output of the differential amplifier back to the Y_f multiplier input, the output of the differential amplifier will adjust its output (the feedback signal) to whatever value is necessary to make the X_fY_f product equal to A. In other words, X_fY_f will be made to equal A, and because X_f is known to be the output of the B Processor Module, $X_fY_f = A$ can be written as $BY_f = A$. Solving for Y_f, the output, one obtains $Y_f = A/B$. As before, U9503 acts as an output buffer. Integrated circuit U9501 and its associated components function as an absolute value circuit, that is, its output is the same polarity for both polarities of applied input. Thus the multiplier does not work directly on the B Processor Module output, but rather on the absolute value of the B Processor Module output. This absolute value relationship is indicated in the transfer function (see specifications). U9502 acts as a buffer between the absolute value circuit and the X_f multiplier input.

6.5C LOG RATIO OPTION (162/96)

This circuit takes advantage of a diode characteristic, namely, that each successive *decade* of change in diode current provides the same number of mV change in diode voltage. In other words, the current and voltage are related logarithmically. Note from the schematic on page VII-23 that two transistors connected as series diodes are connected between the input and output of integrated-circuit amplifier U9604. As a result of this diode feedback, the output voltage of U9604 varies as the log of the input current. The transfer function for U9604 is nominally 140 mV/decade. A 1 kHz oscillator controlling Q9601 and Q9602 alternately connects to the output of one Processor Module and then the other to the input of the log element (U9604). As a result, providing the two processor module outputs are not the same, a 1 kHz square wave is developed at the output of Q9604. The peak-to-peak amplitude of this square wave is proportional to the ratio of A/B. Note that both the A Processor Module output and the B Processor Module output are first routed through absolute value circuits so that the polarity applied to the log element is always positive. The absolute value of the U904 output is of no consequence. The ratio information is carried in the peak-to-peak level, which would be the same for inputs of 10 V and 1 V as it would be for inputs of 1 V and 100 mV. The common mode dc level would shift for the two examples of course, but would have no effect on the final output voltage.

This square wave is applied to an ac amplifier (U9605) that provides a gain of five. An associated dc restorer subtracts out the common mode dc

component, that is, the output of U9605 is a zero-referenced positive square wave. The amplitude of this square wave is five times the pk-pk amplitude at the output of the log element. U9603 and Q9603 form a simple half-wave demodulator, also driven by the 1 kHz clock, that provides the final dc voltage out. The gain is variable to compensate for differences in the log transfer function of the log diodes from one unit to another. The overall transfer function for the option is given in the specifications.

It may be instructive to take a closer look at the baseline restoration circuit. Assume that the A and B switching levels at the output of U9604 are 0.265 V and 0.545 V respectively. In other words, the signal at the output of U9604 is a square wave with a pk-pk amplitude of 280 mV (0.545 V − 0.265 V = 0.280 V). This signal is applied to ac amplifier U9605. During the B part of the cycle, that is, for that part of the cycle in which Q9602 conducts and for which the U9604 output is 0.545 V, Q9604 also conducts, connecting the output of U9605 to integrator U9606. Equilibrium is achieved when the output of U9606 is the same as the applied voltage (0.545 V). At that point, the output of U9605 will be zero. When the crossover to the A part of the cycle takes place, Q9604 cuts off. However, the "B" voltage across C9606 remains, referencing amplifier U9606 to 0.545 V and not to ground. Thus the amplifier sees the A level (0.265 V) with respect to 0.545 V and not with respect to ground. As a result, during the A part of the cycle, the output of U9605 goes to five times the *difference* potential, and not to five times the potential with respect to ground. In effect, the common mode component has been removed; the U9605 output is a zero-referenced square wave proportional in amplitude to the pk-pk amplitude of the applied signal.

6.5D RATIO OPTION (162/97)

Introduction

The Ratio Option circuit is schematically depicted on page VII-21. Referring to the schematic, note that a unijunction transistor, Q9701, is used in conjunction with an octal counter/decoder to provide the three-phase clock that controls the remaining ratio-option circuitry. Because the circuit operation is different for each of the three successive clock states, each is discussed separately.

Phase B

The nature of the operating cycle is such that the operation is most easily understood by considering the B portion of the cycle first. During "B", the output of the B Processor Module is applied to amplifier U9702 via the B channel of the input multiplexer, U9701. The gain of this stage, as established by the ratio of R9706 to R9702, is nominally ×1.2 (inverting). Thus the amplified B signal is applied to the X input of the multiplier, U9703. The multiplier is followed by two integrated-circuit amplifiers, the second of which is referenced to the output of dc restorer U9705. The dc restorer is active only during the C part of the cycle, and for the purpose of this discussion, its output (identically the non-inverting input to U9702) can be considered to be ground.

Note that the U9702 output is applied to an absolute value circuit, U9708 and its associated components. The absolute value circuit output is a positive current that is summed with the 140 μA negative current supplied through R9745 and R9761. The difference current is applied to integrator U9705, which in turn drives the Y input of the multiplier. The feedback is negative in the sense that the loop comes to equilibrium when the U9702 output voltage reaches nominally 1.4 V (either polarity). At that point the current supplied by the absolute value circuit will exactly cancel that supplied by R9745 and R9761, at which point there will be no input current to integrator U9705. With no current applied to its input, the output of U9705 will "hold". The actual U9705 output voltage will depend on the magnitude of the B voltage at the multiplexer X input. The loop sets the Y voltage at that level which, when multiplied by the B voltage at the X input, gives 1.4 V at the output of U9702. In other words, the product is constant, and this can only be so if the voltage developed at the Y input is the reciprocal of the amplified B voltage at the X input.

To summarize, during the B part of the cycle, the voltage at the Y input of the multiplier goes to 1/B, where the "B" in this case is the amplified output of the B Processor Module. There is no other action during the B part of the cycle. The demodulator, U9706-U9708, is not active during the B part of the cycle, and the option output voltage simply holds at whatever voltage it may be at.

Phase C

During the C part of the cycle, the input multiplexer applies ground to the X input of the multiplier. 1/B continues to be applied to the Y input because input current to integrator U9705 is only available during the B part of the cycle. Thus the integrator output continues to "hold" at the 1/B level. The multiplier output then has 1/B applied to one input and zero to the other. The product should be zero, and the voltage at the output of U9702 should go to zero as well. Note that integrator U9705 (dc restorer integrator section and not the Y input integrator section) is switched on during the C part of the cycle only. If there is any dc offset at the output of U9702, dc restorer integrator current will be applied through R9725. As a result, the dc restorer integrator output will ramp in the direction necessary to reduce the current. The net effect is that, during the C part of the cycle, the output of U9702 goes to 0 V, independent

of any dc offsets in the preceding circuits. Moreover, because the required correction voltage "holds" at the integrator output when the C part of the cycle ends, the offset correction will remain as well. This active compensation tracks any changes in offset that occur with time or temperature.

A Phase

During the A Phase, the input multiplexer applies the output of the A Processor Module to the X input of U9703. 1/B continues to be applied to the Y input. With A applied to one input, and 1/B applied to the other, the multiplier develops an output voltage proportional to A/B. Thus a voltage proportional to A/B is available at the output of U9702 during the A part of the cycle. This voltage is demodulated by U9706-U9708, buffered by U9704, and made available at the output. The option output then only changes during the A portion of each cycle. It is because 1/B is developed during the B part of the cycle that A/B can be provided during the A part of the cycle.

Note that the gain of the output demodulator is about seven, as established by the ratio of R9755 plus R9752 to R9759.

6.6 MODEL 163 TROUBLESHOOTING

The basic premise is that proper operation of the mainframe has been established.

6.6A PRELIMINARY STEPS

(1) With the mainframe power off, mount the two Processor Module Extender Cards (6020-0093 and 6020-0098) into the Channel A mainframe slot.

(2) Note that there are two Model 163 circuit boards. The smaller of these, the Logic board, must be lowered to gain access to test points on both boards. If the screws that secure the lower rail are loosened, the board can easily be rotated down, making the test points on both boards readily accessible. Once the Model 163 is in position with the Logic board fully lowered, the screws that secure the lower rail can be tightened, allowing the Logic board to help support the Model 163.

(3) Plug the Model 163 into the two extender cards installed in step 1. Note that the Sampling Head should *not* be installed at this time. (With the Sampling Head not installed, the Overload light will glow continuously.)

(4) Turn the mainframe power on.

6.6B +5 V REGULATOR CHECK

The +5 V power used in the Model 163 is established by an integrated-circuit regulator on the Logic board. This voltage is most easily checked at the positive end of capacitor C3225. If the measured voltage is nominally +5 V, one can assume that the Model 163 +5 V regulator, U3204, is functioning properly.

6.6C LOGIC CIRCUITS (see Figure VI-4 for timing relationships)

(1) Set the mainframe controls as follows.

Aperture Delay
% Initial A: 50%
% Initial B: 50%
Range: 10 μs
Trigger Mode: EXT (other pushbuttons released)
Scan Select: EXT and A (other pushbuttons released)
Aperture Duration: setting immaterial
Scan Time: 1 SEC and CAL
Function: A (digital storage OFF)
Mainframe Time Constant: 0.1 mSEC and CAL

(2) Set the Model 163 controls as follows.

Baseline Sample Delay dial: fully counterclockwise, concentric pushbutton to be "in"
All other M163 controls: setting immaterial at this time

(3) Delay Range Frame and M163 Trigger Holdoff Checks

(a) Connect an external trigger source to the mainframe TRIGGER INPUT connector. The trigger frequency should be nominally 8 kHz. Adjust the TRIGGER LEVEL control for proper mainframe triggering as indicated by the TRIGGERED lamp.

(b) Monitor the signal at TP3206 with the oscilloscope. The signal should be the Delay Range Frame complement, a logic 0 frame with a duration of nominally 10 μs and a repetition period of nominally 125 μs.

(c) Increase the trigger input frequency to 100 kHz. The frequency of the observed signal will increase to about 10 kHz but no more. If the indicated behavior is observed, one can conclude that the Trigger Holdoff circuit is functioning normally. If not, this circuit is malfunctioning. Note from the schematic on page VII-3 that the 100 μs holdoff pulse is generated by U3206 working together with transistors Q3209 through Q3212. The flip-flop is clocked on the trailing (positive going) edge of the Delay Range Frame signal applied to pin 3 of U3205. It is reset after nominally 100 μs by the feedback signal from the output of Q3212 to the Preset Input of the flip-flop. The Trigger Holdoff

pulse, a 100 μs logic 0, is taken from the collector of Q3210. This signal is fed back to the mainframe to prevent the Model 162 from being triggered faster than 10 kHz when operated in conjunction with a Model 163.

(d) Reduce the input trigger rate to 8 kHz again. For convenience in observing the other M163 circuits, trigger the oscilloscope externally from the beginning (negative going) edge of the signal at TP3206.

(4) Baseline Channel Detector and Mode Inhibiting

(a) Monitor the voltage level at U3202-13. A logic 0 level should be measured.

(b) Rotate the M163 BASELINE SAMPLE DELAY dial clockwise. As soon as the dial is rotated a few degrees, the voltage at pin 13 of U3202 will switch to a logic 1. At the same time, relay K3001, a reed relay located on the M163 Signal board, will be energized. An audible click can be heard as the relay energizes. If the indicated action is observed, the Baseline Channel Detector, U3201, Q3206, and the two NOR gates of U3203 that follow, are all working properly.

(c) Leave the BASELINE SAMPLE DELAY control fully counterclockwise.

(5) Baseline/Signal Channel Alternator Checks

(a) Monitor the voltage at pin 9 of U3206. The level should be a steady logic 0. This logic 0 applied to pin 5 of U3202 inhibits strobing of the sampling head when the BASELINE SAMPLE DELAY control is fully counterclockwise.

(b) Monitor the voltage at pin 5 of U3210. The level should be a steady logic 0. This logic 0 applied to pin 12 of U3202 inhibits the Baseline Sampling 0.5 μs one shot, which consists of two gates of U3202 (pins 1-2-3 and 11-12-13).

(c) Monitor the level at pin 8 of U3205. There should be a logic 1 level at this point. This logic 1 acts through the Baseline Feedback Switch Driver (schematic on page VII-5) to bias shunt FET Q3025 into conduction and thereby prevent the voltage at the Baseline Integrator output from being applied to the Feedback Amplifier, U3003. The logic 1 at pin 8 of U3205 is also applied to pin 13 of U3006, enabling the Signal Gate One Shot so that it can be triggered by the output of the Trigger Amplifier, Q3229-Q3230.

(d) Monitor the signal at pin 8 of U3206. The voltage at this point should be a logic 1. This voltage, applied to pin 9 of U3005, enables the Signal Strobe drive gate (U3005, pins 8-9-10-11), allowing the Sampling Head Strobe circuit to be triggered by the output of the Trigger Amplifier (Q3029-Q3030). The Sampling Head Strobe circuit should be operating at 8 kHz.

(e) Monitor the level at pin 12 of U3205. A logic 0 should be measured. This logic 0, acting through the Signal Feedback Switch Driver circuit, biases Q3024 off, allowing the output of the Signal Channel Integrator to reach the Feedback Amplifier.

(f) Rotate the BASELINE SAMPLE DELAY control clockwise about half a turn. Then monitor the signal at pin 9 of U3206. The observed signal should be a square wave at 4 kHz (trigger frequency is 8 kHz), indicating that the alternator flip-flop (one of the two flip-flops in the U3206 package) is functioning properly.

(g) Monitor pin 4 of U3203. The observed signal should be a logic 0 pulse at 8 kHz, with each logic 0 lasting 2 μs. If these signals are as indicated, the two Delay Circuits U3208 and U3209, along with the following gate of U3203, are all working properly.

(h) Monitor the signal at pin 8 of U3205. The observed signal should be the same as that at pin 8 of U3206 but delayed by 2 μs.

(i) Monitor the signal at pin 12 of U3205. The observed signal should be the same as that at pin 0 of U3206, but delayed by 2 μs. If the signals at pins 8 and 12 of U3205 are as indicated, the two flip-flops of U3210, together with the two following gates of U3205, are working correctly to provide the delayed signals that control the shunt gates ahead of the Feedback Amplifier. By delaying 2 μs, there is no possibility of a "signal cutoff" if the sample position is located near the end of the Aperture Delay Range.

(6) One Shot Checks

(a) Monitor the signal at the Model 163 GATE OUT connector. Two gate pulses should be visible, each a half microsecond wide. The position of one should be set by the

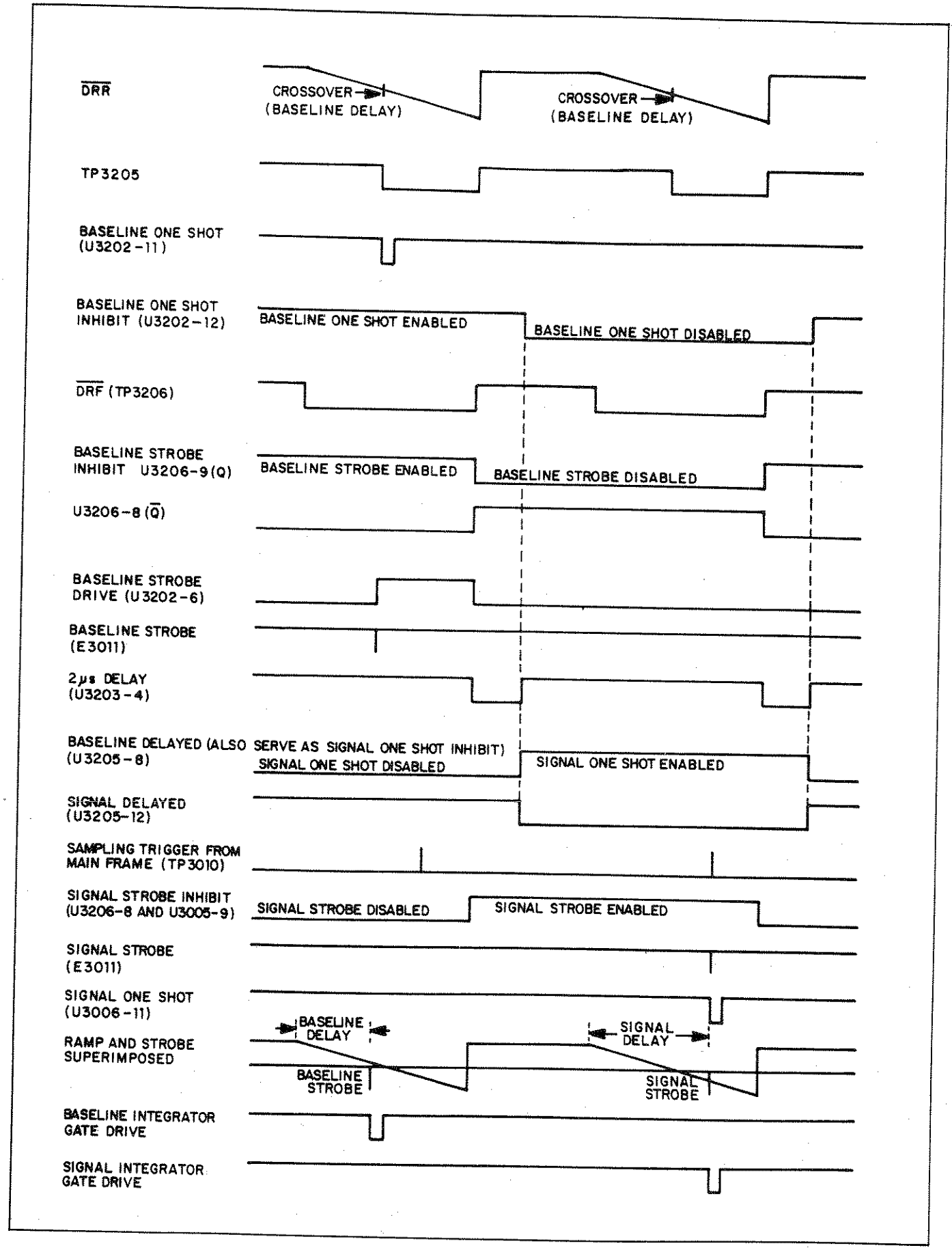


Figure VI-4. MODEL 163 LOGIC TIMING RELATIONSHIPS

BASELINE SAMPLE DELAY control (the assumption is that the oscilloscope is still being triggered from the leading edge of the Delay Range Frame). The pulse will disappear if the BASELINE SAMPLE DELAY control is rotated fully counterclockwise. The position of the other pulse is set by the Model 162 % Initial Delay A dial.

(b) If the Baseline Gate Pulse is as indicated, one can assume that the Baseline Delay Generator (schematic on page VII-3) and the following One Shot are working properly. If the Signal Gate Pulse is as indicated, one can assume that the Trigger Amplifier (schematic on page VII-6) and the following Signal Gate One Shot are working properly.

(c) Leave the BASELINE SAMPLE DELAY control half a turn from the fully counterclockwise position and leave the % Initial Delay A dial set to 75%.

(7) Integrator Gate Drivers

(a) Connect the oscilloscope to the collector of Q3019. The observed signal should be a half-microsecond wide negative going pulse with its baseline at +5 V and its peak at −7.5 V. The pulse position relative to the leading edge of the Delay Range Frame is set by the % Initial A dial. Leave the dial set to 75%. If the signal is as indicated, the Signal Integrator Gate Driver circuit (schematic on page VII-5) is working properly.

(b) Connect the oscilloscope to the collector of Q3022. The observed signal should be the same as that observed in the preceding step, except that in this case, the pulse position is set by the BASELINE SAMPLE DELAY dial. If the signal is as indicated, the Baseline Integrator Gate Driver is functioning normally. Leave the Baseline Sample Delay control set about half a turn from the fully counterclockwise position.

(8) Feedback Switch Drivers

(a) Monitor the signal at TP3006. The observed signal should be a 4 kHz square wave with its upper level at ground and its lower level at −13 V.

(b) Transfer the signal to TP3009. The signal should be the same as in the preceding step but of opposite phase. If the signal in these two steps is as indicated, the Feedback Switch Driver circuits (schematic on page VII-5) are functioning properly.

6.6D SIGNAL PROCESSING CIRCUITS

Description

Each time the Sampling Head is strobed, a sample is taken of E_{IN}. This sample passes through a series of Model 163 amplifiers and is then applied to the Signal Integrator or to the Baseline Integrator, according to whether the sequence in progress is a signal-sampling sequence or a baseline-sampling sequence, as described previously. During the half microsecond gating period, the integrator output moves asymptotically towards $-10\ E_{IN}/S$ (S is the sensitivity 1, 0.25, or 0.1), following the RC charging curve at the rate appropriate to the integrator time constant (setting of SAMPLES AVERAGED switch). The integrator output is routed through an output Buffer, U3009, and is then made available at the front-panel OUTPUT pin jack. The buffer output is also routed to the mainframe signal processing circuits. The direct integrator output is additionally applied to a Feedback Amplifier. The output of this amplifier is fed back to the Sampling Head for comparison with E_{IN}. As the integrator output asymptotically approaches $-10\ E_{IN}/S$, the feedback voltage asymptotically approaches E_{IN}. Equilibrium is reached when the feedback voltage is "exactly" E_{IN}. At that point, the Sampling Head output is zero (average value; a waveform out is always visible), no more current is available to the integrator, and the integrator output holds at the proper level.

The net Model 163 gain measured from the Sampling Head input to the OUTPUT pin jack is $1/A_{FB}$, where A_{FB} is the attenuation of the feedback half of the loop. The attenuation is set by the gain of U3003 (always $\times 0.5$) and by the attenuator that follows U3003. The attenuator is controlled by the Sensitivity switch. With a Sensitivity setting of 1 V, the attenuator reduces the U3003 output voltage to 1/5. With a sensitivity of 250 mV, the attenuation is 1/20. With a sensitivity of 100 mV, it is 1/50. Multiplying the attenuator reduction by the gain of U3003, the net feedback attenuation for the three sensitivity settings is 1/10, 1/40, and 1/100, giving net gains of $\times 10$, $\times 40$, and $\times 100$ respectively.

In Baseline Sampling operation, the output of first one integrator and then the other is fed back on alternate cycles so that the loop always works on the proper signal, allowing each integrator output to asymptotically approach the proper voltage.

There is considerable gain provided in the forward part of the loop as well. The Sampling Head output is followed by a $\times 1/2$ attenuator (R3004 and R3014) and two amplifiers (each $\times 31$) having an attenuator controlled by the Sensitivity switch interposed between them. Forward loop gain has no effect on the Processor Module sensitivity. That sensitivity is set by the feedback "gain" alone as

explained in the preceding paragraph. However, forward gain *does* influence the response time of the integrators, as does the feedback "gain" and also the actual values of the integrating RC components. Forward gain makes the RC product look smaller than it actually is. The more feedback that is applied the smaller the RC product looks. As the sensitivity is changed from 1 V to 250 mV, to 100 mV, the feedback is proportionally reduced and the apparent RC product is increased. This is compensated for by increasing the gain in the forward part of the loop to the same degree by means of the attenuator interposed between the two amplifiers. The increasing forward gain makes the RC product look smaller in the same amount as the decreasing feedback makes it look bigger, thereby keeping the gain around the entire loop constant and making the integrator response time independent of the selected sensitivity.

Troubleshooting

With regard to troubleshooting the signal processing circuits, only some very general suggestions can be made. With the Sampling Head not installed, one can make some simple dc zero checks on the amplifiers. Specifically, the voltage at the output of each of the ×31 amplifiers should be zero. The output of the feedback amplifier should be zero if TP3012 and TP3013 are grounded. The output of each of the integrators will drift up to one limit or the other. (**NOTE:** With TP3012 and TP3013 grounded, the integrator outputs are tied to hard ground.) Assuming TP3012 and TP3013 are not grounded, the integrators can be checked by pressing the front-panel CLEAR pushbutton. As long as CLEAR is held in, the integrator outputs should be at 0 V. At the same time, the front-panel OUTPUT pin-jack voltage should be 0 V, giving a check of the M163 output buffer amplifier.

If the indicated zero-check behavior is noted, chances are there are no catastrophic failures in the Model 163 Signal Processing circuits. The next step would be to install the Sampling Head and do signal tracing while performing the initial checks from Section II of the manual. If the amplifiers are working properly, and the logic circuits are working properly, the most likely components to give trouble would be the gates, Q3013 and Q3023. Leakage in these gates, or in the Clear FET's, Q3014 and Q3026, could degrade the hold time or give generally abnormal integrator performance. If Q3024 or Q3025 should fail, the feedback loop would not work properly. Either both signals would be fed back together (Q3024 or Q3025 open) or one would never be fed back (Q3024 or Q3025 shorted).

When the Model 163 troubleshooting is complete, the power should be turned off before pulling the extenders and returning the Model 163 to its normal operating position (if appropriate).

6.7 MODEL 164 TROUBLESHOOTING

The basic premise underlying the following procedure is that the mainframe is known to be in good working order and that the necessary Model 164 Extender, 6020-0093, is available.

6.7A PRELIMINARY STEPS

With the mainframe power off, plug the extender (6020-0093) into the Channel A slot. Then plug the Model 164 into the extender so that the Processor Module can be operated out on the bench. One should *not* operate with a Model 163 at the same time because of the restricted trigger rate (10 kHz) obtained with a M163.

6.7B +5 V REGULATOR CHECK

The +5 V power used in the Model 164 is established by U402, an integrated circuit regulator. This voltage is most easily checked by measuring the voltage at the positive end of C408. If the voltage is +5 V ±0.2 V, one can assume that the regulator is working properly.

6.7C TIMING AND SWITCHING CIRCUITS

(1) Mainframe Control Settings

Aperture Delay
% Initial Delay A: 50%
% Initial Delay B: 50%
Range: 20 μSEC
Trigger Mode: EXT
Scan pushbuttons: EXT and A (other pushbuttons released)
Aperture Duration: 5 μSEC and CAL
Scan Time: 1 SEC and CAL
Function: A (digital storage OFF)
Mainframe Time Constant: 0.1 mSEC and CAL

(2) Model 164 Control Settings

Time Constant: 1 μSEC
Pushbuttons: EXP. GND, and DC in (others released)

(3) Gate Generator Checks

(a) Connect a 10 kHz trigger source to the mainframe Trigger INPUT connector and adjust the TRIGGER LEVEL control for proper triggering as indicated by the mainframe TRIGGERED lamp.

(b) Monitor the signal at TP402. One should see a negative-going transient at 10 kHz. The "peak" will be at ground and the baseline at nominally +6 V. The width will only be a few nanoseconds.

(c) Monitor the signal at the collector of Q404. The observed signal should be a 5 μs wide pulse switching between nominally plus two and minus two volts. The complement of this signal should be

present at the collector of Q405. These signals drive the diode bridge gate. This bridge is active for all values of aperture duration. If the width is "wrong", see if it can be adjusted to 5 μSEC by means of the M164 front-panel GATE TRIM adjustment before concluding that the circuit is malfunctioning.

(d) Rotate the Aperture Duration switch through its entire range. For each position, the observed pulse width (collector of Q404 or collector of Q405) should be that selected. It may prove convenient to monitor at TP403 instead of Q404, and at TP404 instead of at Q405. The signals will be the same but offset negatively by one diode drop (about −0.4 V). In the SPEC position, without an appropriate "special" capacitor installed, the pulse width will be somewhere in the range of 5 ns to 50 ns.

If problems are noted with any particular range, note that the Aperture Duration switch actually controls relays K401 through K407, and that these relays switch in different timing capacitors for the different settings. Relay K403 is energized if the switch is set to any of four settings, SPEC, 500 μSEC, 50 μSEC, or 5 μSEC. Leave the Aperture Duration set to 5 μSEC.

(e) Vary the inner knob of the Aperture Duration control. The ramp should increase linearly from its calibrated value of 5 μSEC to a maximum of nominally 50 μSEC with the multiplier fully clockwise. When the trailing edge of the gate pulse extends beyond the end of the Aperture Delay Range, the OVERLAP light will glow. Because the delay is set to 50%, the gate pulse begins 10 μs after the start of the Aperture Delay Range. When the gate is 10 μs or longer, it will extend beyond the end of the Aperture Delay Frame and trigger the overlap indication. Note that the Overlap circuitry consists primarily of two gates of U401 and three gates of U403. These gates monitor both the gate pulse and the Delay Range Frame complement. The gates are arranged such that any time there is a gate pulse in progress but not a Delay Range Frame, Q411 activates the Overlap Light Drive circuit at the mainframe. At the same time, Q410 provides a Trigger Holdoff signal to the mainframe triggering circuits so that the unit cannot be triggered for the duration of the overlap. Leave the Aperture Duration set to 5 μSEC and CAL.

(f) Transfer the oscilloscope to TP406. The signal here should be a positive +5 V pulse. This pulse controls the FET gate as described later. Because the FET is switched only on the three slower ranges (four if you include SPEC), the circuitry is not as fast as that which drives the diode-bridge gate. Even though the FET gate is actually switched on the three slow ranges only, the pulse at TP406 is available on all ranges. This is the same pulse as drives the front-panel GATE OUT connector. On the three fast ranges, a dc override input to the FET gate keeps the gate in conduction independent of the applied pulse.

If the indicated behavior has been observed, one can conclude that the Model 164 APERTURE GATE GENERATOR circuitry (schematic on page VII-7) is functioning normally.

(4) Gate Circuits (schematic on page VII-9)

(a) Before proceeding, be sure that the Aperture Duration is set to 5 μSEC and CAL.

(b) Monitor the 5 μs signals at TP403 and at TP404. The signal at both points should be a 4 V pk-pk pulse, complementary with respect to the test points. The absolute level will be about +1.6 V and −2.4 V. If these signals are as indicated, one can assume a normal drive is available to the diode-bridge gate. A description of the bridge follows.

The bridge consists of diodes CR432 through CR435. The pulses that turn the bridge on and off are supplied through CR423 and CR422. In the quiescent state, CR422 and CR423 are both conducting, with the diode current supplied by current sources Q417 and Q418. The junction of CR432 and CR434 is quiescently at −2 V while the junction of CR433 and CR435 is quiescently at +2 V. The bridge diodes are back biased and nonconducting. When the pulse is applied, CR422 and CR423 cut off, the bridge diodes are biased into conduction, and the current from Q417 (identically that through Q418) flows through the bridge diodes. The voltage at the output of the preamplifier passes through the bridge and is applied to the following integrator via the FET gate Q429.

(c) Monitor the signal at TP407. The drive signal to the FET gate should be present, a negative-going pulse with its baseline at +0.6 V and its "peak" at −15 V. If the

Aperture Duration switch is set to the three longest settings or SPEC, the pulse is applied. On the three fast ranges, Q429 is locked into conduction (TP407 at − 15 V) via the dc control signal applied to the base of Q414. Leave the Aperture Duration at 5 μSEC and CAL.

6.7D SIGNAL PROCESSING CIRCUITS

(1) Preamplifier (page VII-10)

(a) Press in the CAL pushbutton and select SUMMATION averaging. Check to be sure that GND is also selected.

(b) Monitor the voltage at TP411 and adjust the M164 front-panel ZERO control for an indicated 0 V. If this can be done, chances are that feedback amplifier U407 is functioning normally.

(c) Transfer the voltmeter to TP410. The voltage at TP410 should be 0 V. If it is, chances are that the preamplifier is working properly.

(d) Release the GND pushbutton. The voltage at TP410 should increase to nominally 0.59 V, checking the preamplifier gain. An incorrect reading is indicative of a preamplifier malfunction.

(2) Overload Detect Circuit

(a) While still operating in the SUMMATION averaging mode, release CAL and connect a variable dc voltage to the M164 input. DC coupling should be selected.

(b) Start from zero and gradually increase the applied voltage until the Overload light glows. Note the required input. It should be nominally 400 mV. Try reversing the polarity. The required input to give an overload indication should still be about 400 mV. Remove the dc source.

(c) If the above indications were noted, the Overload circuit can be presumed to be functioning properly. If not, a malfunction in this circuit can be assumed. Do not overlook the possibility of a burned out light bulb. The schematic for this circuit is located on page VII-10, along with that of the preamplifier.

(3) Integrator

In the following steps, the gated integrator will be checked by observing the output behavior with a known input and a known duty factor. The trigger rate will be decreased to 1 kHz. With a five microsecond gate, this gives a duty factor of 1/200. In other words, the observed time constant will be 200 times longer than that selected with the M164 Time Constant switch.

(a) Select EXP averaging. Then push in both the CALIBRATE and GROUND pushbuttons. Set the Model 164 Time Constant to 10 mSEC and decrease the trigger rate to 1 kHz. **NOTE:** With a duty factor of 1/200 and a time constant of 10 ms, the observed time constant will be two seconds.

(b) Press in the CLEAR pushbutton. The mainframe panel meter should indicate "0". If the desired "0" cannot be obtained, the integrator may be malfunctioning, or the Q430 circuit. A failure in the Digital Storage Option could make this test fail in units equipped with that option.

(c) Release the GND pushbutton. The observed time constant should be nominally two seconds. After two seconds, the meter should indicate nominally 63% of full scale, and after ten seconds (five time constants), the meter indication should stabilize at or near full scale. If the final meter indication is not exactly full-scale, adjustment of the CAL screwdriver adjustment on the M164 front panel should result in obtaining the desired full-scale indication. Be sure to allow time for the unit to fully respond each time the adjustment setting is changed.

(d) Press CLEAR again. The meter indication should go immediately to "0" and remain there for as long as the CLEAR pushbutton is held down. When the pushbutton is released, the meter indication will again rise to full scale at the observed time constant rate.

(e) Release the CAL pushbutton. The meter indication should fall to zero, taking about ten seconds to stabilize.

If these indications were proper, the Integrator and the Gates are working properly. If not, there could be a malfunction with the integrator (U406) or with either gate circuit. (Recall that the previous gate checks only checked the gate drive waveform.) With the five microsecond aperture duration, both gates are active. One could as well check the behavior with only the bridge active by selecting an aperture duration of 50 nSEC. If the repetition rate is increased to 10 kHz at the same time, the observed time constant will remain at two seconds and the circuit response time will be the same as in the preceding checks.

Another check one can make is to evaluate the hold time. This can be done by disconnecting the trigger input when the meter indication is at about half scale. If it is done with the Aperture Duration set to 5 μSEC and CAL, the hold time with the FET gate biased off is checked. Under these conditions, and with a M164 Time Constant setting of 1 mSEC, the mainframe panel meter indication should drift no faster than 20% of full scale in 100 seconds.

If the hold time check is made with the Aperture Duration set to 5 nSEC and CAL, the hold time with the FET "on", that is, with the dominant leakage being that of the diode gate, is checked. Under these conditions, and with a M164 Time Constant setting of 10 mSEC, the mainframe panel meter indication should drift no faster than 20% of full scale in 10 seconds (leakage is a factor of hundred greater, but the time constant capacitor is a factor of ten greater as well, limiting the apparent leakage increase to a factor of ten).

If the hold-time check fails, there are several possibilities. The excessive leakage current could be inherent to the integrator IC, U406, it could be coming through Q430, or it could be coming from the gate circuits. A less likely possibility is the integrating capacitors, C461 through C464. Checking under the two sets of conditions specified allows isolation of one gate or the other, although a failure of Q429, the FET gate, could cause failure under both sets of conditions.

This completes the M164 checks. At this time, the power can be turned off so that the M164 can be returned to its normal operating position, if appropriate.

6.8 DIGITAL STORAGE OPTION

The digital storage circuitry is schematically depicted on page VII-25 (Channel A) and VII-26 (Channel B). The Channel A circuitry and the Channel B circuitry are the same. Hence the schematics are virtually identical, the only differences being that those circuits that serve both channels are shown on the Channel A schematic and not on the Channel B schematic.

Digital storage from a "black box" point of view is discussed in Subsection 6.3E. Here the discussion deals with the internal workings of the digital storage board. Even though digital storage is accomplished with a rather complicated mix of digital and analog techniques, troubleshooting with the aid of an oscilloscope should be relatively straightforward given a basic understanding of how the circuitry works.

Referring to the Channel A digital storage schematic (page VII-25), note that there are two inputs. The first is the ENCODE pulse generated in the mainframe at the end of each Delay Range Frame interval. The second is the Processor Module Output. The processor module output is applied to pin 2 of comparator U9916 (through R9938 and R9939). The digital storage output voltage is also applied to comparator U9916 (through R9940). As will be shown, the comparator operates in a loop to force the digital storage analog output voltage to be equal to the Processor Module output voltage but of opposite polarity. This loop operates and completes its activity during the 1 ms ENCODE period.

The arrival of the ENCODE pulse at the digital storage board triggers the digital storage sequence. First, ENCODE directly resets the 40 Clock, U9902. In addition, it resets the sequencer, U9908, and triggers the 50 μs pulse generator, U9910. The resultant pulse in turn inhibits the 1 MHz Oscillator, U9901, for 50 μs via Q9901. It also provides an input to the U9904 flip-flop and to the U9907 flip-flop that controls the counter input gates. The effect is to preload the counter to 50% of full scale. With the counter preloaded to 50% of full scale, a corresponding 50% of full scale current is provided at the output of the D/A Converter. This current, which is negative, is applied to the input of I/E Converter U9918. Note that positive current is also applied to the input of U9918, through R9954 and R9953. This current is also 50% of full scale but its polarity is opposite that supplied by the D/A Converter. Because the two input currents to U9918 are equal and opposite, there is no net input to this circuit and its output is at 0 V. In other words, when an ENCODE pulse is sensed, the digital storage output voltage is set to 0 V at the start of the digital storage sequence. Note that there is a third current input to U9918, this one from the output of U9917 through R9955. As a part of the starting sequence, Q9906 is switched into conduction, resetting integrator U9917. The output of U9917 then goes to zero, and no current is supplied through R9955.

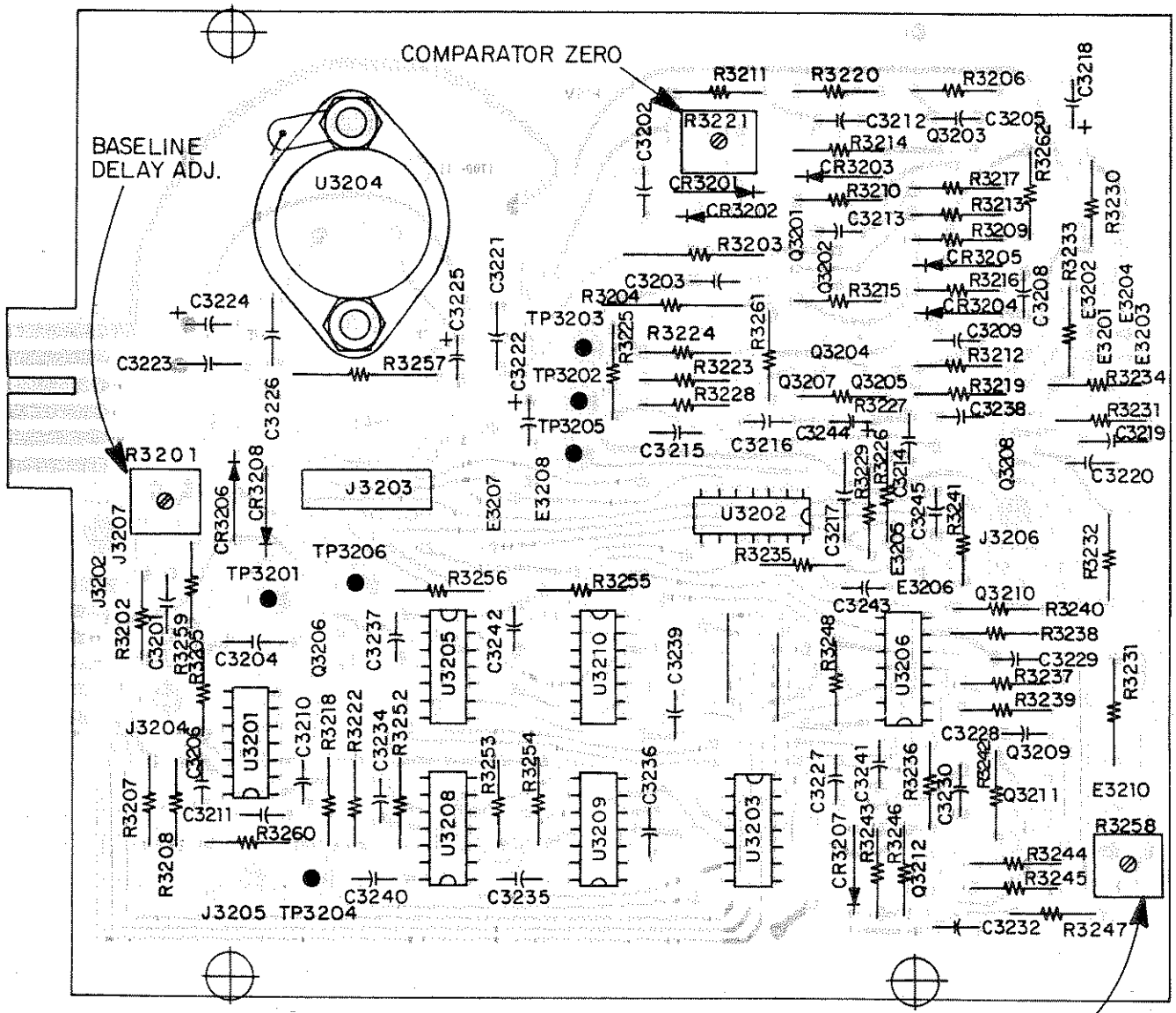
At the end of the 50 μs reset pulse triggered by ENCODE, the oscillator inhibiting ends and the oscillator starts to run at 1 MHz. U9902 provides a divide-by-four frequency division making a 250 kHz signal available to the counter. The gates controlling the counter determine whether the counter will count up or count down. Comparator U9916 does the polarity sensing. Recall that the digital storage output is at 0 V due to the reset. The Processor Module output will be either positive or negative. If the Processor Module output is positive, U9916 will act through U9911 and the following counter-control gates to cause the counter to "count down" from its 50% of full scale starting point. As the counter counts down, the negative current out of the D/A Converter diminishes, that is, becomes smaller than the positive current supplied to U9918 through R9953 and R9954. The output of U9918 goes negative in response to the

net positive input. It will continue to go negative, tracking the down count, until crossover occurs, that is, until the U9918 output voltage is greater than the Processor Module output voltage. When crossover occurs, U9916 acts through U9911 and the counter-control gates to stop the counter. With the counter stopped, the D/A output current stops changing, and the net input current to U9918 stops changing. In other words, a voltage equal and opposite to the Processor Module output voltage has been developed. Recall that the basic assumption was that the Processor Module output voltage was positive. Had it been negative, the counter-control gates would have reversed, forcing the counter to count up instead of down. In that case, the negative current out of the D/A converter would have increased, making the net input to U9918 negative, and causing a positive digital storage output to be developed. By preloading the counter to 50% of full scale, and subtracting the 50% at the input to U9918, operation with either polarity input is accomplished.

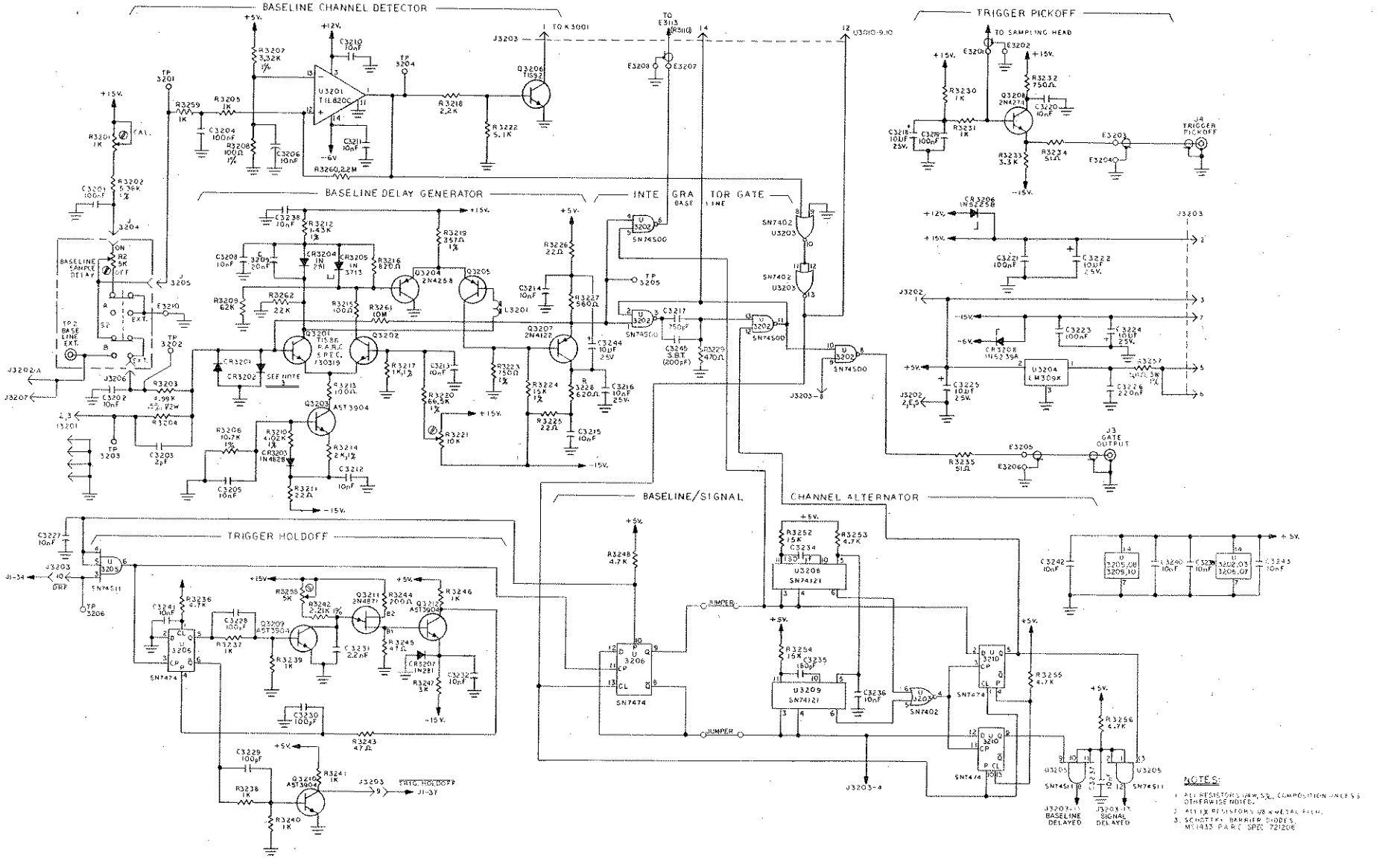
It should be noted that the final voltage developed during the sequence just described can be in error by as much as one counter bit, which corresponds to ± 100 mV at the output of U9918. Consequently, as soon as the counter is switched off, another loop takes over to correct this remaining small error. This second loop, which consists of U9918, U9916, U9915, and U9917, is activated by switching Q9906 off and Q9907 on at the end of the counter-active part of the sequence. Unless the U9918 output voltage and the Processor Module output voltage have identically the same magnitude, there will be a non-zero voltage developed at the output of U9916. This voltage is amplified by U9915 and applied to integrator U9917. As soon as Q9907 is switched into conduction (this happens when the counter stops counting), the integrator begins to ramp positively or negatively according to the polarity of the residual error. The loop is closed by applying the output of U9917 to the "trim" input of U9918 through R9955. Thus the output of U9917 asymptotically approaches that voltage which, when applied to U9918 causes the output of U9918 to be identically the Processor Module output (but of opposite polarity). When the two magnitudes are the same, there will be no further net error voltage at the output of U9916 and U9915, and therefore no more input current to U9917. Thus the U9917 output voltage holds at the level reached, keeping the net input current to U9918 at precisely the correct value.

The entire sequence described is completed during each 1 ms ENCODE pulse. By the end of the ENCODE interval, the required equal but opposite voltage is developed. This voltage and the Processor Module output voltage are compared and the difference fed back to the Processor Module integrator as described in Subsection 6.3E. Because integrator U9917 is not perfect, but drifts, the analog "correction" voltage drifts as well, and with time, the digital storage output voltage can change as much as 400 mV. It can change no more than that, however, because 400 mV represents the limit of influence of the U9917 integrator on the U9918 output voltage.

SECTION VII
SCHEMATICS

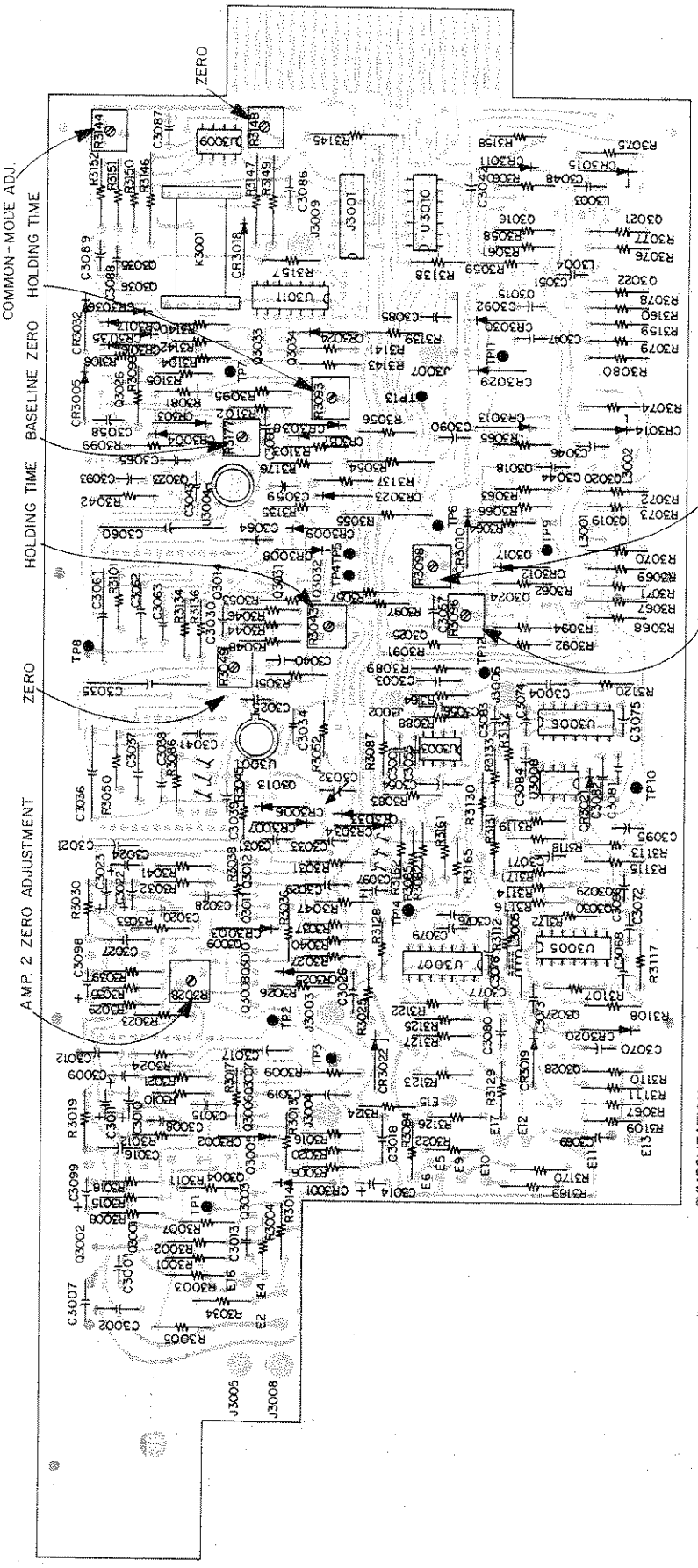


SYMBOLIZATION
MODEL 163
LOGIC BOARD

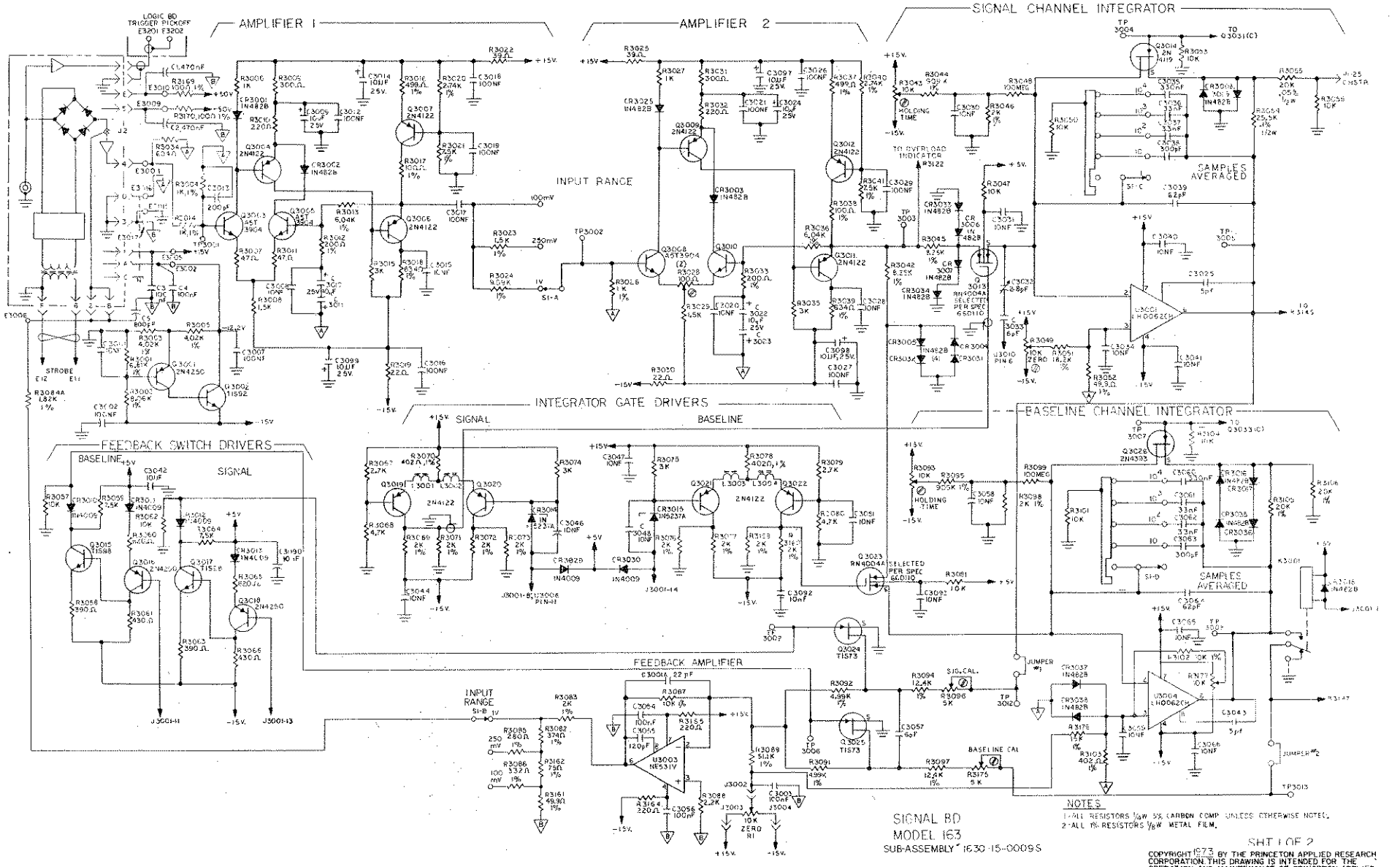


LOGIC BOARD SUB-ASSEMBLY 1630-24-0008S MODEL 163

8251 D SD K



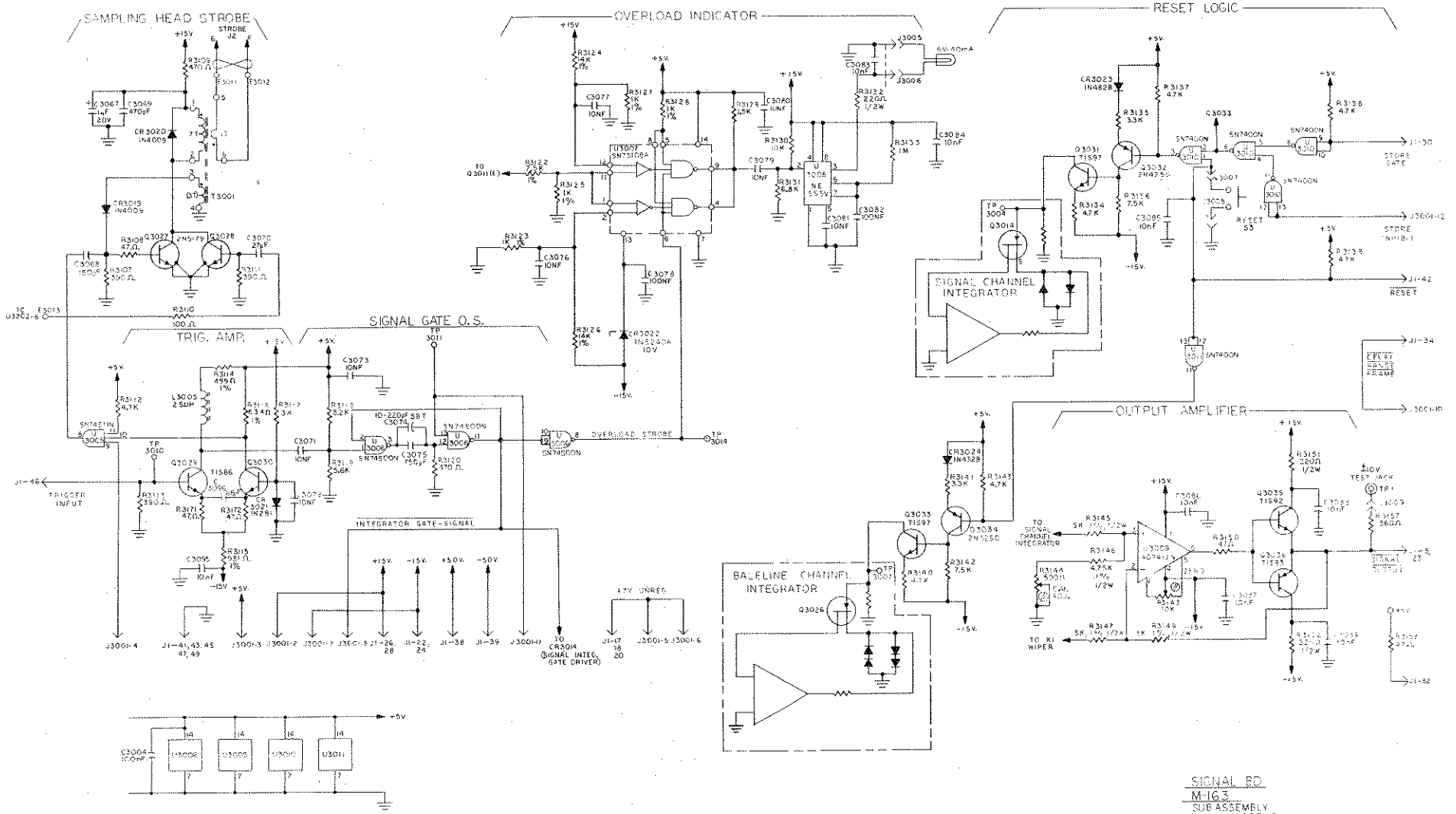
SYMBOLIZATION
MODEL 163
SIGNAL BOARD



NOTES
1-ALL RESISTORS ¼W 5% CARBON COMP UNLESS OTHERWISE NOTED.
2-ALL 1% RESISTORS ⅛W METAL FILM.

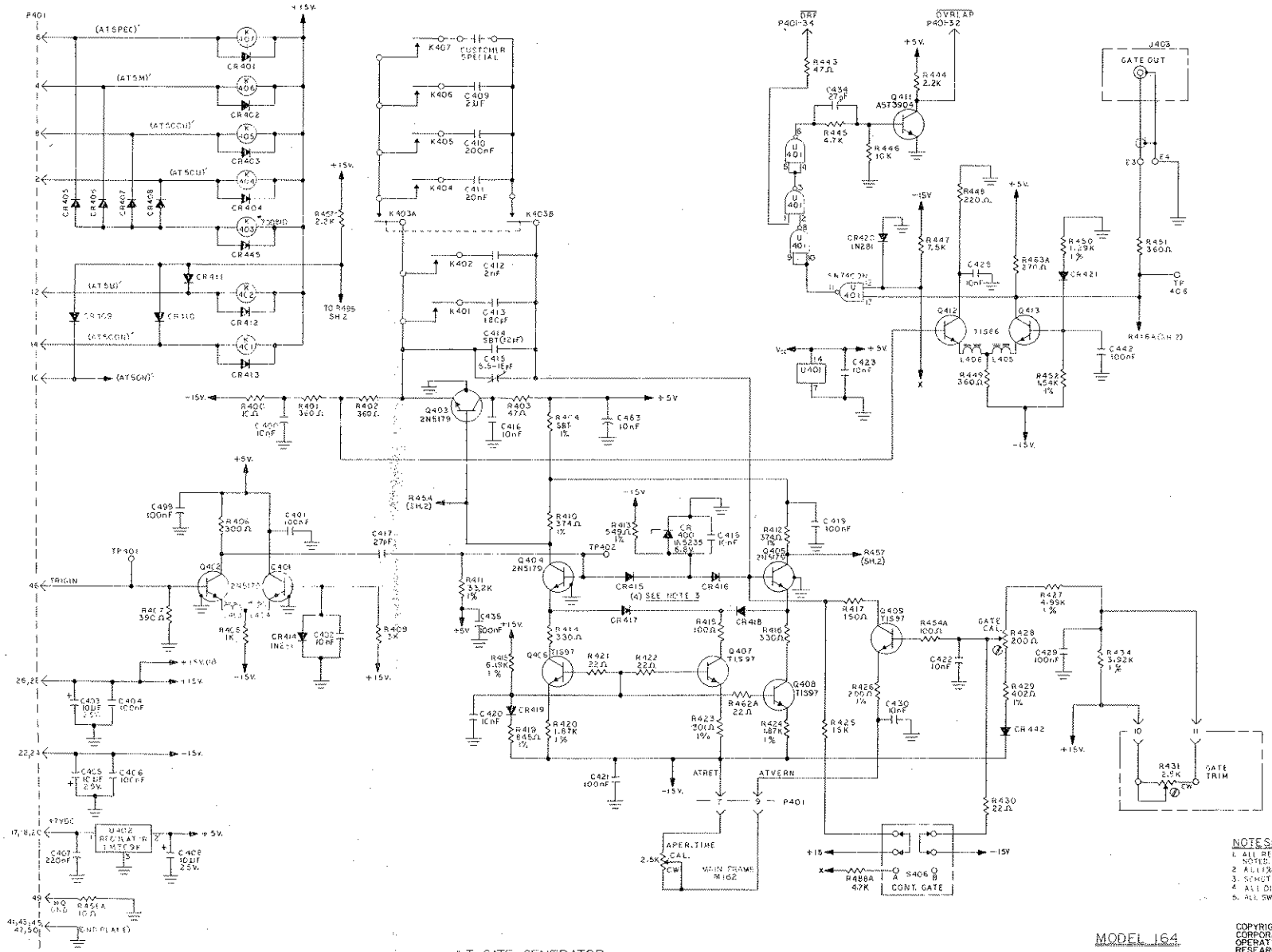
SHT 1 OF 2

8244 D 5D F



SHT 2OF2

8244 D 50

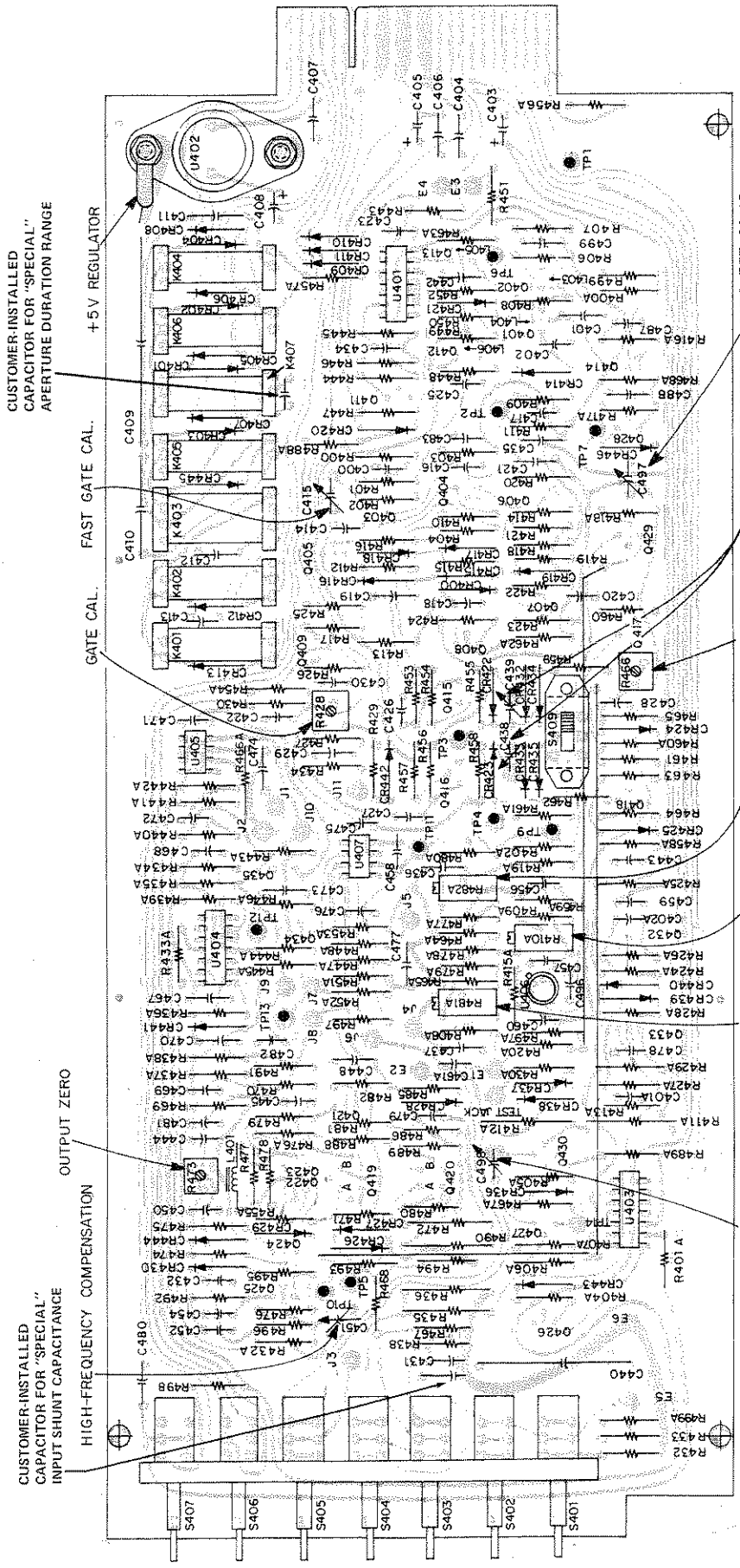


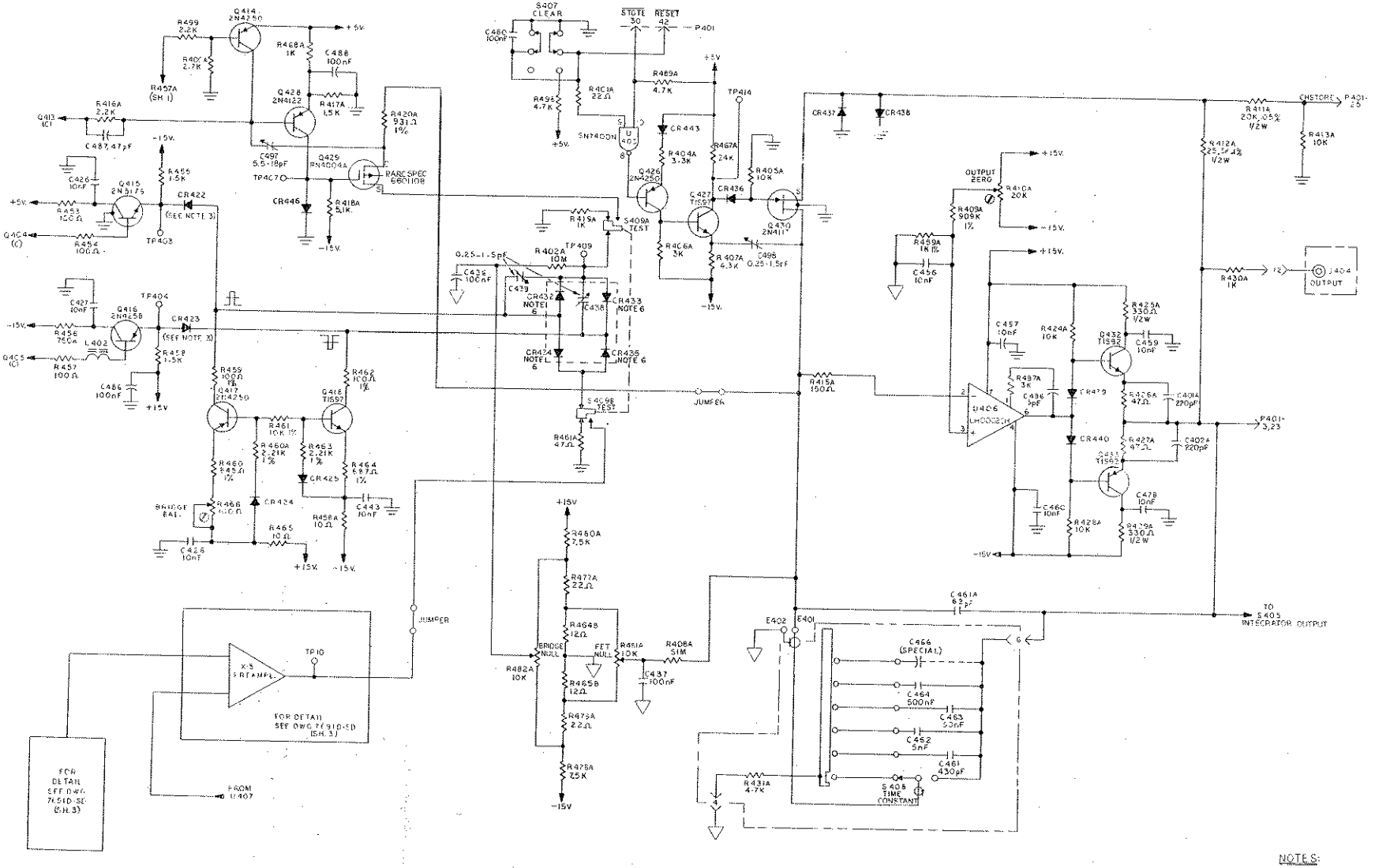
A.T. GATE GENERATOR

SUB ASSY 1640-13-0009s
(PARTIAL)

MODEL 164

NOTES:
1. ALL RESISTORS ¼W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. ALL 1% RESISTORS ARE ¼W METAL FILM.
3. SCHOTTKY DIODES.
4. ALL DIODES ARE IN4828 UNLESS OTHERWISE NOTED.
5. ALL SWITCHES SHOWN IN ACTUATED POSITION.


CUSTOMER-INSTALLED
CAPACITOR FOR "SPECIAL"
APERTURE DURATION RANGE
+5 V REGULATOR
FAST GATE CAL.
GATE CAL.
GATE FET COMP.
BRIDGE COMPENSATION
BRIDGE NULL
BRIDGE BAL.
OUTPUT ZERO
FET NULL
FET COMPENSATION
OUTPUT ZERO
HIGH-FREQUENCY COMPENSATION
CUSTOMER-INSTALLED
CAPACITOR FOR "SPECIAL"
INPUT SHUNT CAPACITANCE
SYMBOLIZATION
MODEL 164
MAIN BOARD



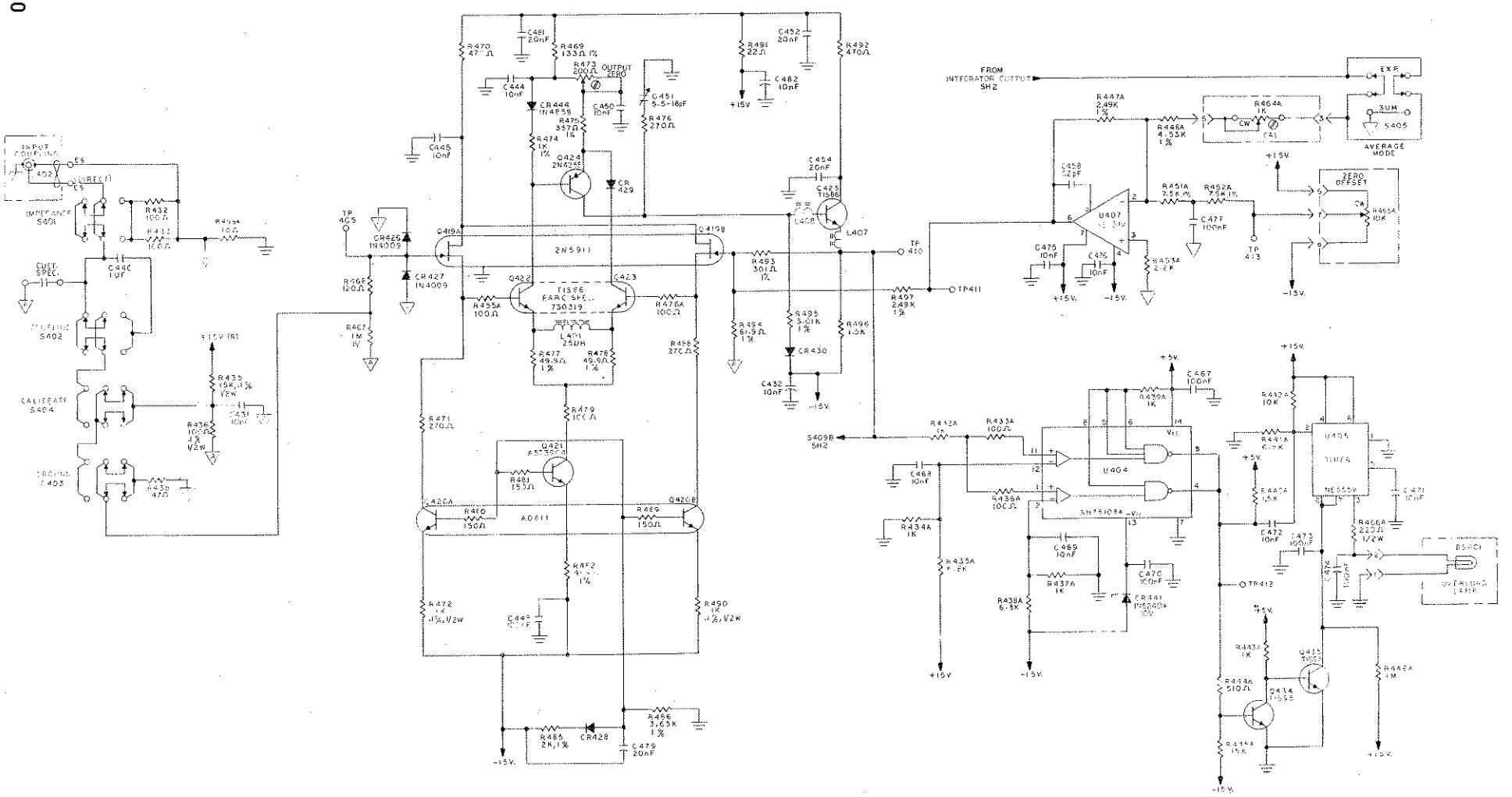
GATED INTEGRATOR
SUB ASSY 1640-13-0009s
(PARTIAL)

MODEL 164

NOTES:

SEE SHEET 1

6 MATCHED SET OF SCHOTTKY DIODES PAIR SPEC* 720407



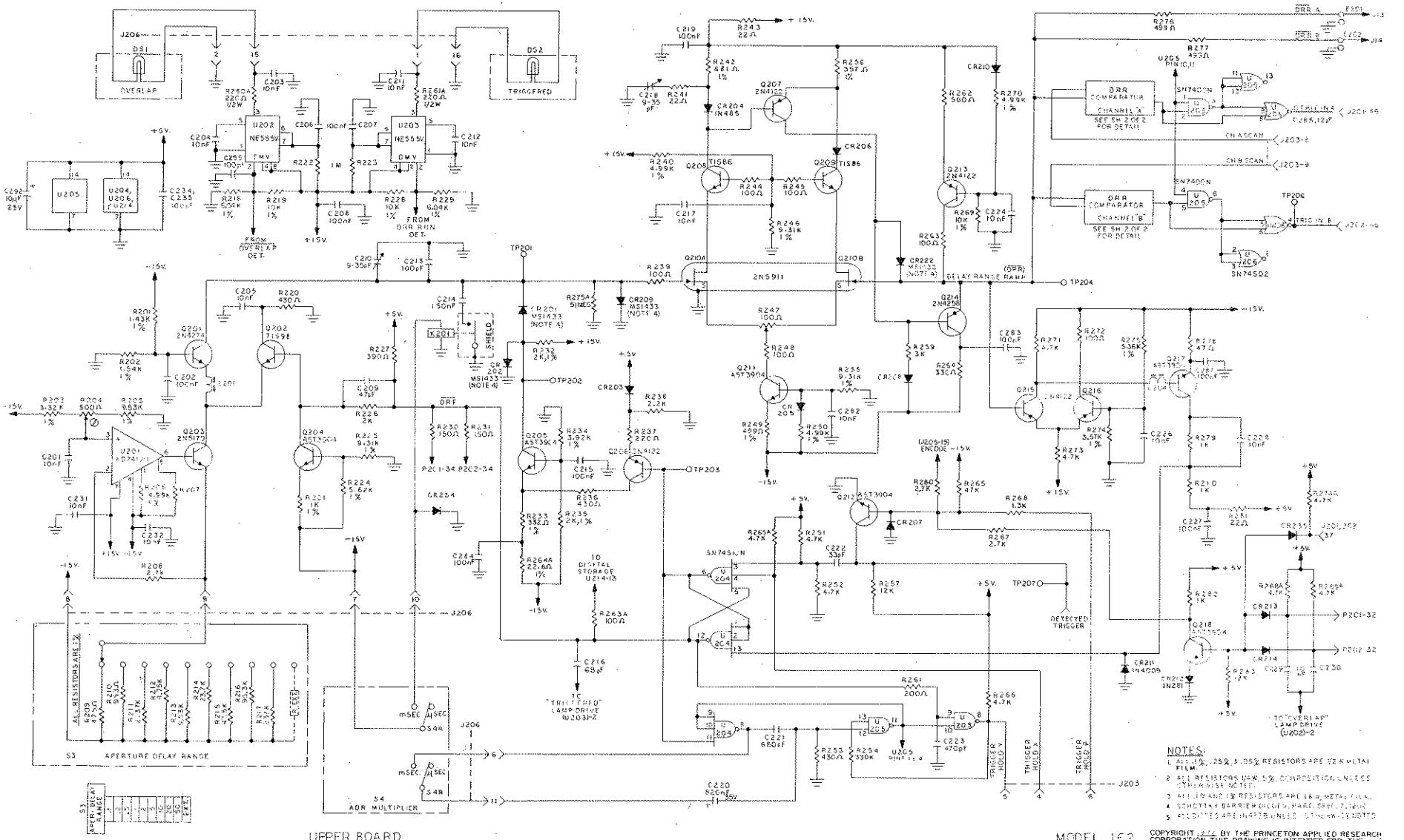
NOTES:
SEE SHEET 1 & 2

INPUT-AMP/OVERLOAD DETECTOR
SUB ASSY 1640-13-0009s (PARTIAL)

MODEL 154

SHEET 3 OF 3 | 7691 | D | SD

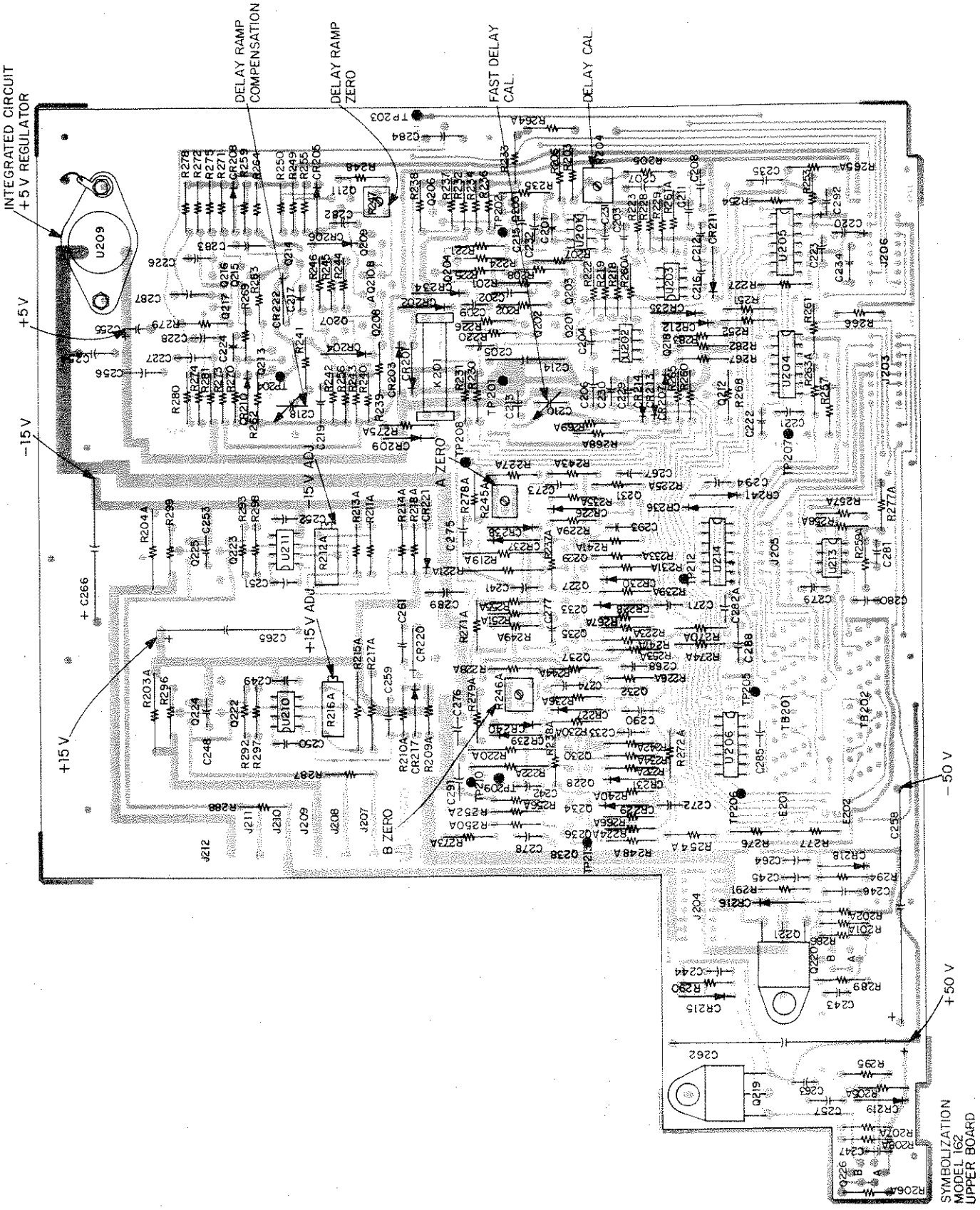
7691-D-SD SH 3 OF 3

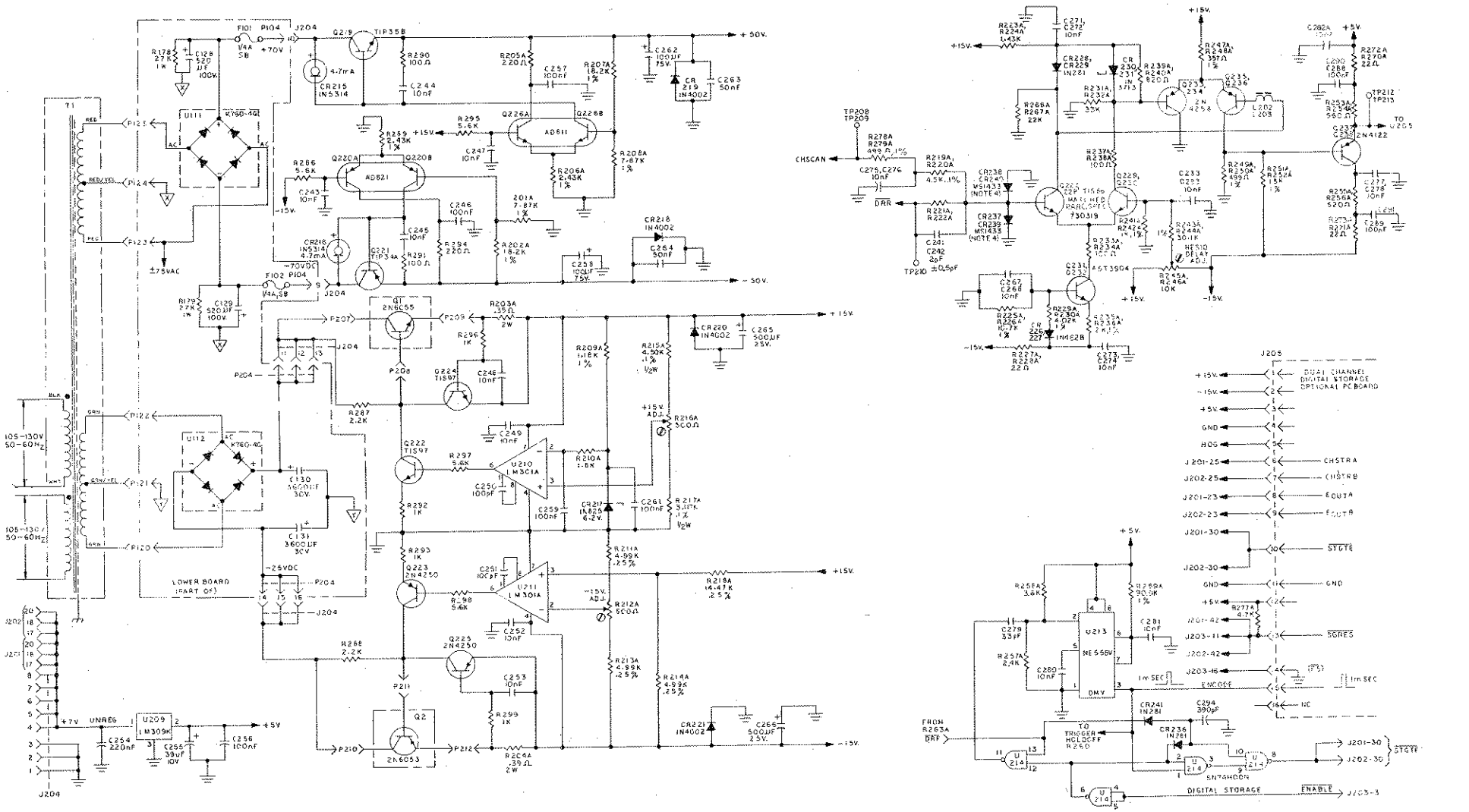


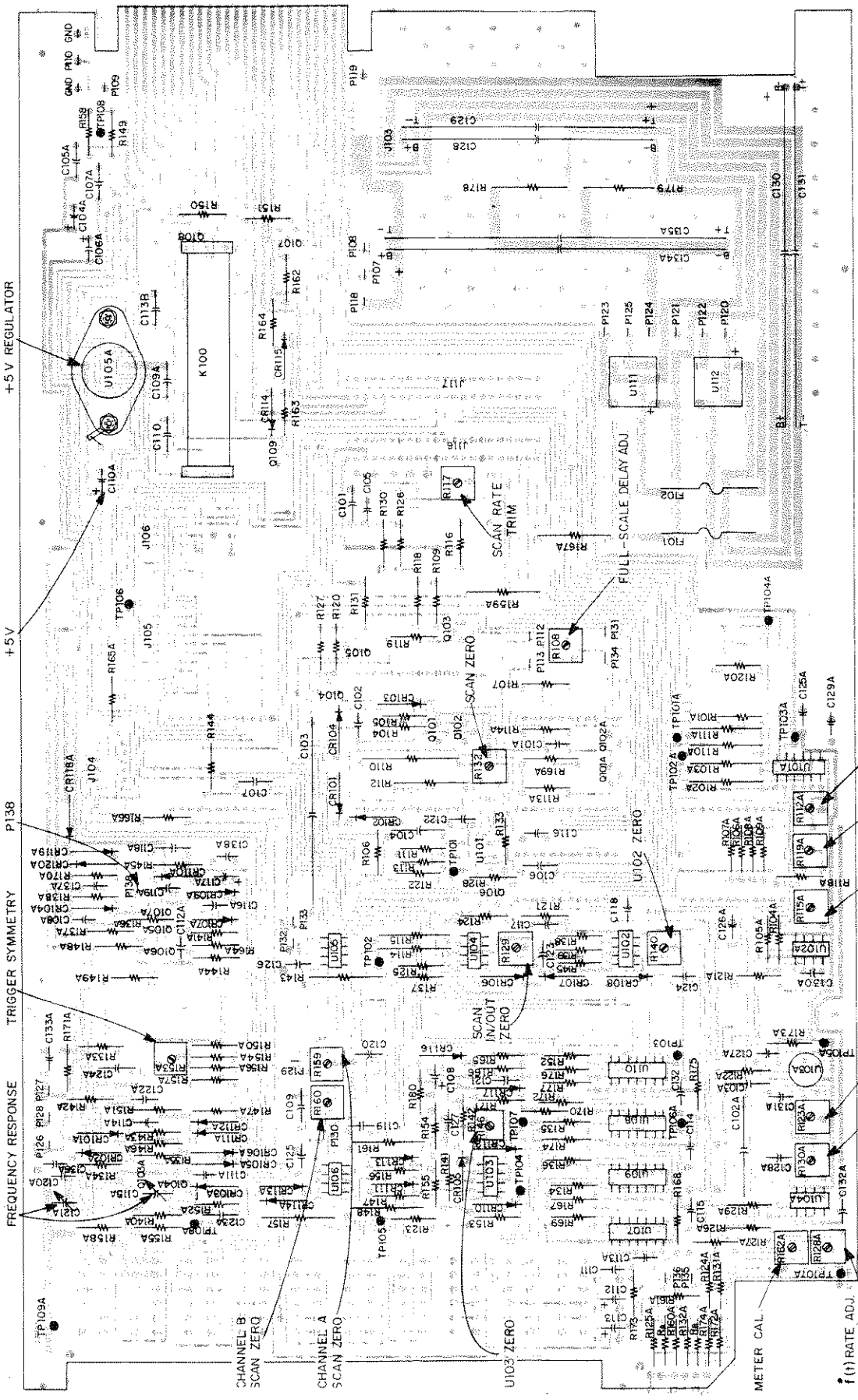
UPPER BOARD
APERTURE DELAY RANGE LOGIC SUB ASSEMBLY 1620-24-0000S

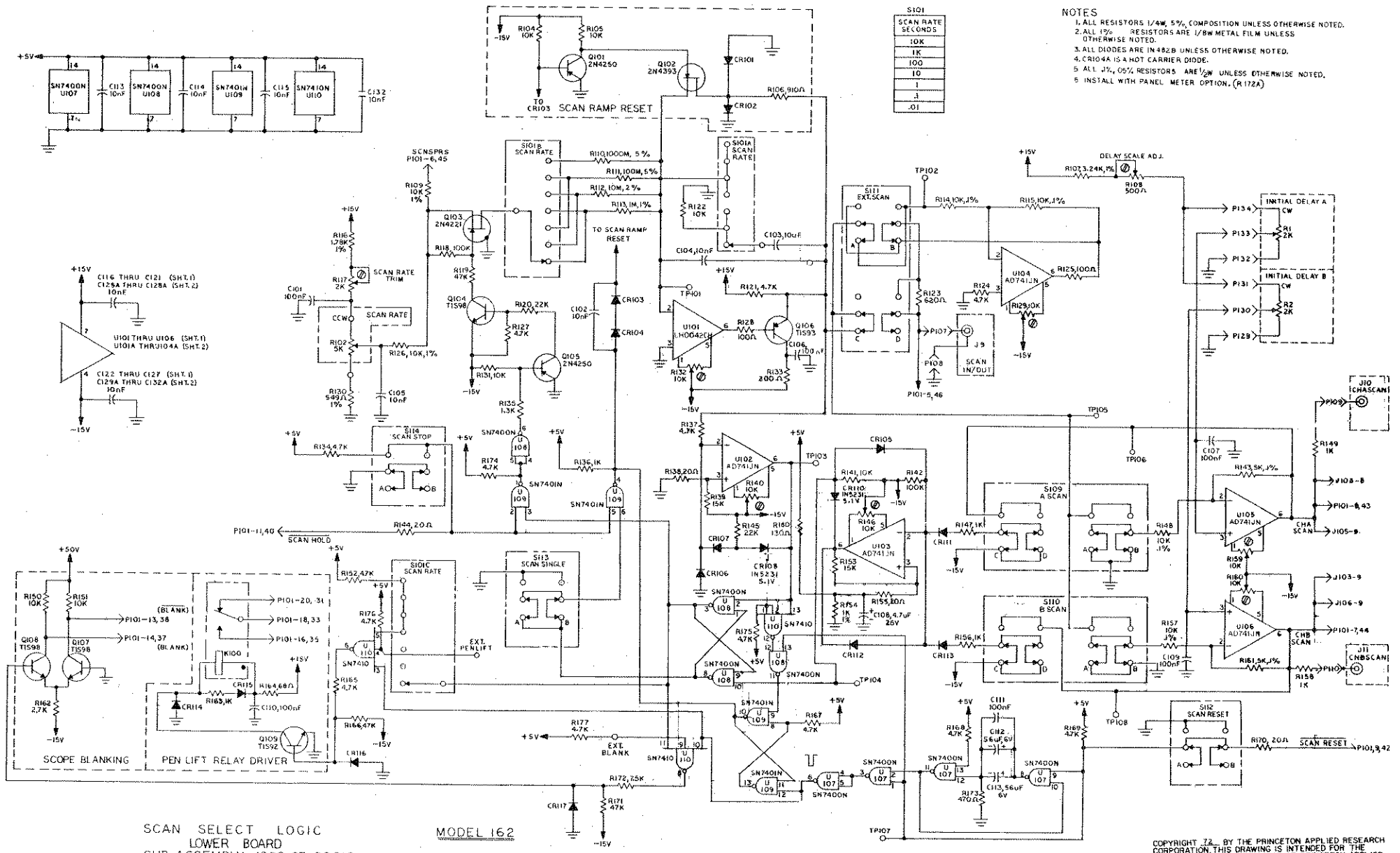
MODEL 162

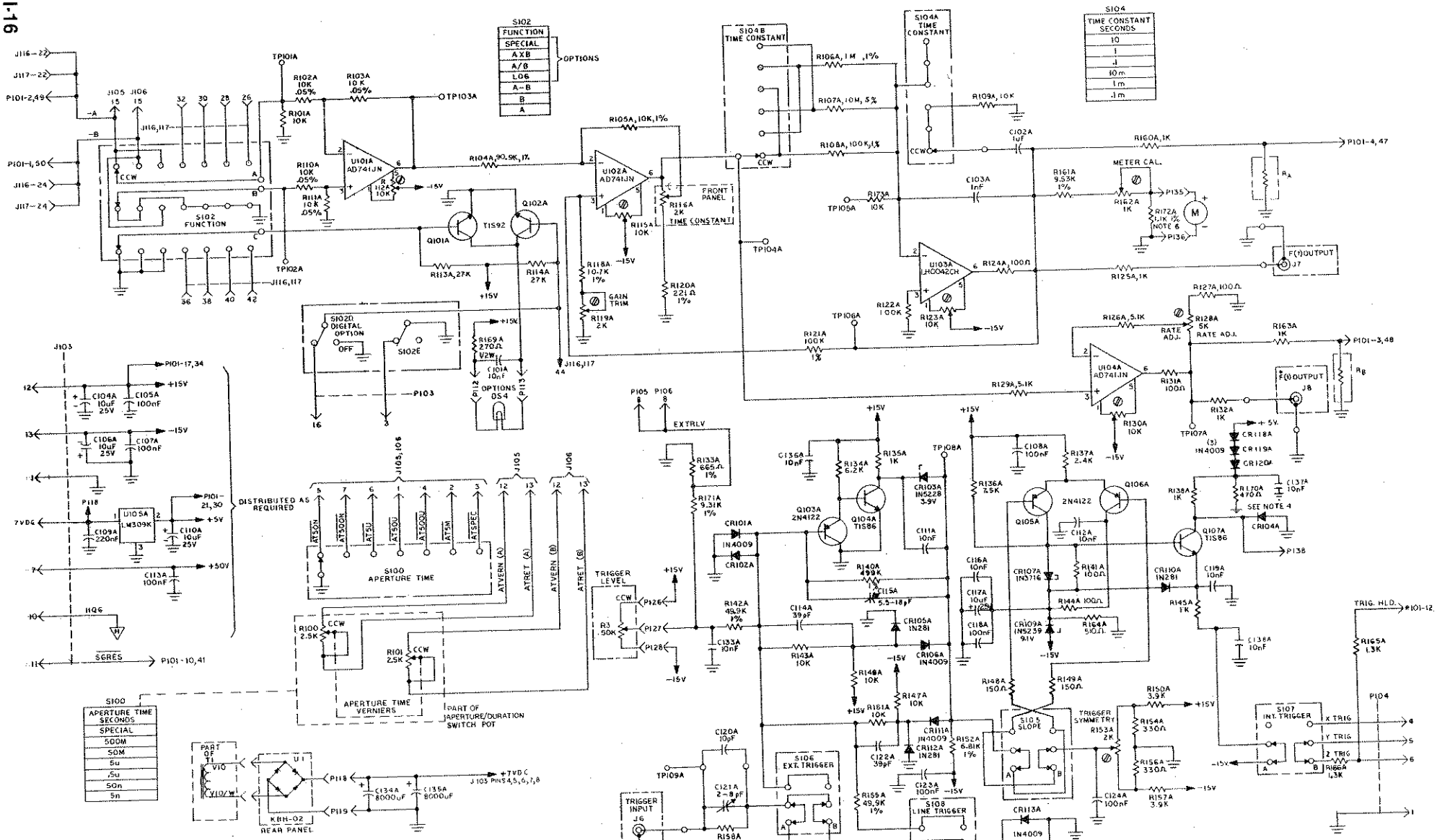
NOTES:
1. ALL 1%, .25%, .05% RESISTORS ARE 1/2 W METAL FILM.
2. ALL RESISTORS 1/4 W, 5%, COMPOSITION, UNLESS OTHERWISE NOTED.
3. ALL 1/2 AND 1W RESISTORS ARE 1W, METAL FILM.
4. SCHOTTKY BARRIER DIODE, MARC SERIES.
5. ALL CAPACITORS ARE IN MFD UNLESS OTHERWISE NOTED.


INTEGRATED CIRCUIT
+5 V REGULATOR
DELAY RAMP COMPENSATION
DELAY RAMP ZERO
FAST DELAY CAL.
DELAY CAL
+5V
−15 V
+15 V
+15 V ADJ
A ZERO
B ZERO
−50 V
+50 V
SYMBOLIZATION
MODEL 162
UPPER BOARD




+5 V REGULATOR
+5 V
P138
TRIGGER SYMMETRY
FREQUENCY RESPONSE
SCAN RATE TRIM
FULL-SCALE DELAY ADJ
SCAN ZERO
SCAN IN/OUT ZERO
U102 ZERO
U101A ZERO
U102A GAIN
U102A ZERO
U103A ZERO
U104A ZERO
SYMBOLIZATION MODEL 162 LOWER BOARD
CHANNEL B SCAN ZERO
CHANNEL A SCAN ZERO
U103 ZERO
METER CAL
f(t) RATE ADJ





TRIGGER / SIGNAL PROCESSING MODEL 162

LOWER BOARD SUB ASSEMBLY 1620-23-0001S

PIN ASSIGNMENTS (J1-J2) (TB201,202)

FUNCTION	ABBR.	PIN	PIN	ABBR.	FUNCTION
+7VDC UNREG.	+7VDC	18	17	+7VDC	+7VDC UNREG.
+7VDC UNREG.	+7VDC	20	19	—	J1 TO J2 INTERCONN.
-15VDC REGULATED	-15VDC	22	21	—	SPARE
-15VDC REGULATED	-15VDC	24	23	-E(OUT)(A,B)	ANALOG OUT(A,B)
+15VDC REGULATED	+15VDC	26	25	CHSTR(A,B)	STORED ANAL. SIG.(A,B)
+15VDC REGULATED	+15VDC	28	27	DLGTE(A,B)	DELAY GATE (A,B)
STORAGE GATE	STGTE	30	29	—	SPARE
OVERLAP BUS	OVRLP	32	31		
DELAY RANGE FRAME	DRF	34	33		SPARE
SPARE	—	36	35	—	SPARE
+50VDC REGULATED	+50VDC	38	37	TRIGHLD	TRIGGER HOLDOFF BUS
J1 TO J2 INTERCONN.	—	40	39	-50V.	-50V REGULATED
COMMON SIG. RESET	SGRES	42	41	GND	GROUND RETURN
SPARE	—	44	43	GND	GROUND RETURN
ATTRIG. INPUT(A,B)	TRIGIN (A,B)	46	45	GND	GROUND RETURN
SPARE	—	48	47	GND	GROUND RETURN
GROUND RETURN	GND	50	49	HQ GND	HIGH QUALITY GND

PIN ASSIGNMENTS P105 & J1 CHANNEL A
PIN ASSIGNMENTS P106 & J2 CHANNEL B

PIN	ABBR.	FUNCTION
1	—	SPARE
2	(AT50J)'	AT ENABLE (.5-50µS)
3	-E$_{OUT}$(A,B)	ANALOG OUT(A,B)
4	(AT5m)'	AT ENABLE (.5-5mS)
5	—	SPARE
6	(AT SPEC)'	AT ENABLE (SPECIAL)
7	AT RET(A,B)	AT RETURN(A,B)
8	(AT500J)'	AT ENABLE (50-500µS)
9	AT VERN(A,B)	AT VERNIER (A,B)
10	(AT50n)'	AT ENABLE (5-50nS)
11	—	SPARE
12	(AT 5µ)'	AT ENABLE (.5-5µS)
13	—	SPARE
14	(AT500n)'	AT ENABLE (50-500nS)
15	CHSCAN(A,B)	SCAN DELAY(A,B)
16	EXTRLV	EXT. TRIG. LEVEL

P101 INTERFACE CONNECTIONS

PINS	FUNCTION		REMARKS
1,50	-E(OUT)B		±10V FS, 1KΩ
2,49	-E(OUT)A		±10V FS, 1KΩ
3,48	F'(EOUT)		RATE OUTPUT
4,47	F(EOUT)		PROCESSED OUTPUT
5,46	SCAN IN/OUT	*	0 TO +10VDC, Z_o=600Ω, Z_{in}=10K
6,45	SCNSPRS	*	PUT SCAN SUPPRESS ACCES.
7,44	CHBSCAN		CHANNEL B SCAN VOLTAGE
8,43	CHASCAN		CHANNEL A SCAN VOLTAGE
9,42	SCANRES	*	LOGIC ZERO RESETS SCAN
10,41	SGRES	*	LOGIC ZERO RESETS SIGNALS
11,40	SCANHLD	*	LOGIC ZERO HOLDS SCAN
12,39	TRIGHLD	*	LOGIC ONE INHIBITS TRIGGERS
13,38	SCOPE BLANK (-)		-35V. PULSE FOR RETRACE BLNK
14,37	SCOPE BLANK (+)		+35V. PULSE FOR RETRACE BLNK
15,36	—		SPARE
16,35	PENLIFT (NO)		1 AMP RELAY CONTACT (NO)
17,34	+15VDC		+15V ± 1%, 100mA
18,33	PENLIFT (W)		1 AMP RELAY CONTACT (WIPER)
19,32	-15VDC		-15V ± 1%, 100mA
20,31	PENLIFT (NC)		1 AMP RELAY CONTACT (NC)
21,30	+5VDC		+5V ± 1%, 300mA
22,29	—		SPARE
23,28	GROUND		GROUND RETURN
24,27	GROUND		GROUND RETURN
25,26	HQ GROUND		HIGH QUALITY (SIGNAL) GROUND

* CONTROL INPUTS (SEE NOTE 2)

NOTES:

1. APERTURE DELAY RANGE — SEE UPPER BOARD SCHEMATIC 7661-D-SD SH1, FOR DETAILS.
2. LOGIC LEVELS FOR EXTERNAL CONTROL INPUTS ARE TTL/DTL COMPATIBLE.
3. FOR 230V. OPERATION USE 1/2 AMP, SB FUSE.

UPPER BOARD (SCHEMATICS 7661-D-SD) (2 SHEETS)

J205 OPTIONAL TWO CHANNEL DIGITAL STORAGE

PIN	FUNCTION
1	+15V.
2	-15V.
3	+5V.
4	GND
5	HQ GROUND
6	CHSTRA-STORED VAL A
7	CHSTRB-STORED VAL B
8	E(OUT)A FROM CH A
9	(E OUT B)- FROM CH B
10	STGTE - FROM D/A TO CH'S
11	GND
12	+5V.
13	SGRES - SIGNAL RESET
14	FS - DIGI. OPT. SW. S103A
15	ENCODE - 1m SEC. PULSE
16	—

PIN	FUNCTION
1	GND
2	—
3	ENABLE DIGITAL STORAGE
4	TRIGHLD X
5	TRIGHLD Y
6	TRIGHLD Z
7	+50VDC
8	CHASCAN
9	CHBSCAN
10	HQ GND
11	SGRES - SIGNAL RESET BUS
12	+15V. REG.
13	-15V. REG.
14	GND
15	LINE SYNC
16	FS DIGITAL OPT. SW. S103A

PINS	UNREG. VOLTAGE
1,2,3	GROUND
4,5,6,7,8	+7VDC
9	-70VDC
10	470 VDC
11,12,13	+6.5VDC
14,15,16	-25VDC

PIN	FUNCTION
2	+15V.
4	—
6	-15V.
8	—
10	+5V.
12	—
14	GND
16	—
18	HQ GND
20	—
22	(-A) INPUT
24	(-B) INPUT
26	(SPEC) OUT
28	(A X B) OUT
30	(A/B) OUT
32	LOG(A/B) OUT
34	—
36	F1 LOG A/B
38	F2 A/B
40	F3 AXB
42	F4 SPEC
44	F5 D/E

OPTION INSTALL.

LOWER BOARD (SCHEMATICS 7599-E-SD) (2 SHEETS)

S105 S106 S107 S108 S109 S110 S111 S112 S113 S114
SLOPE | EXT. | INT | LINE | SCAN A | SCAN B | SCAN EXT. | RESET | SINGLE | HOLD

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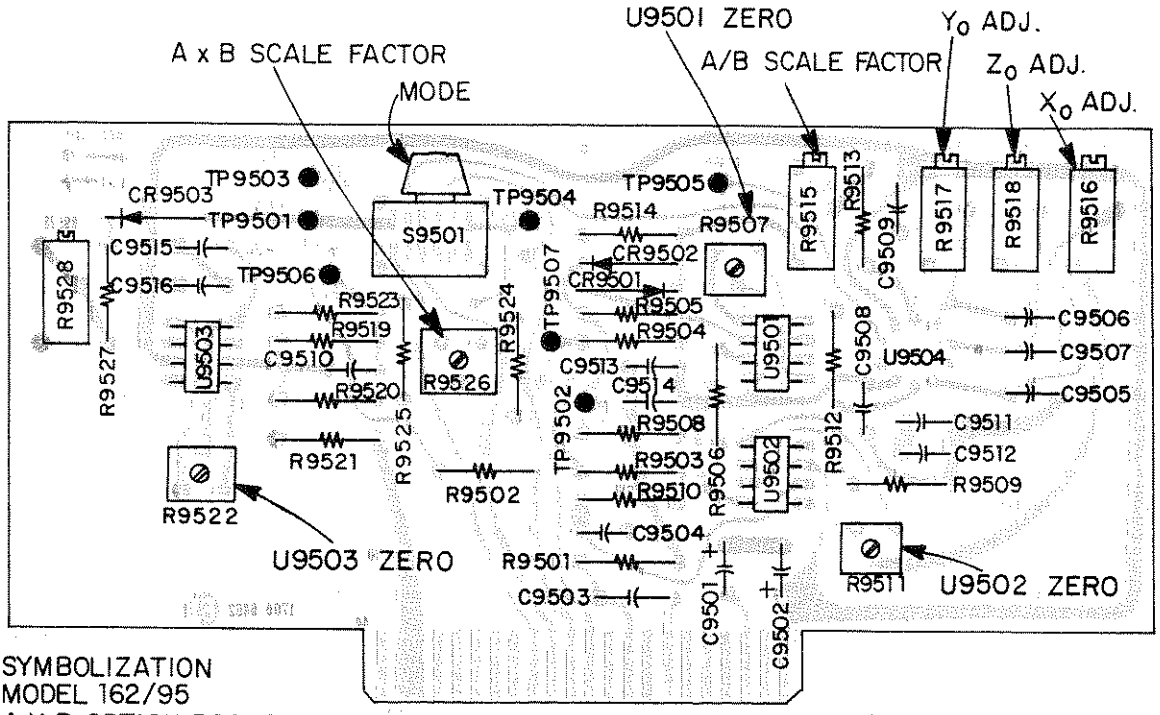
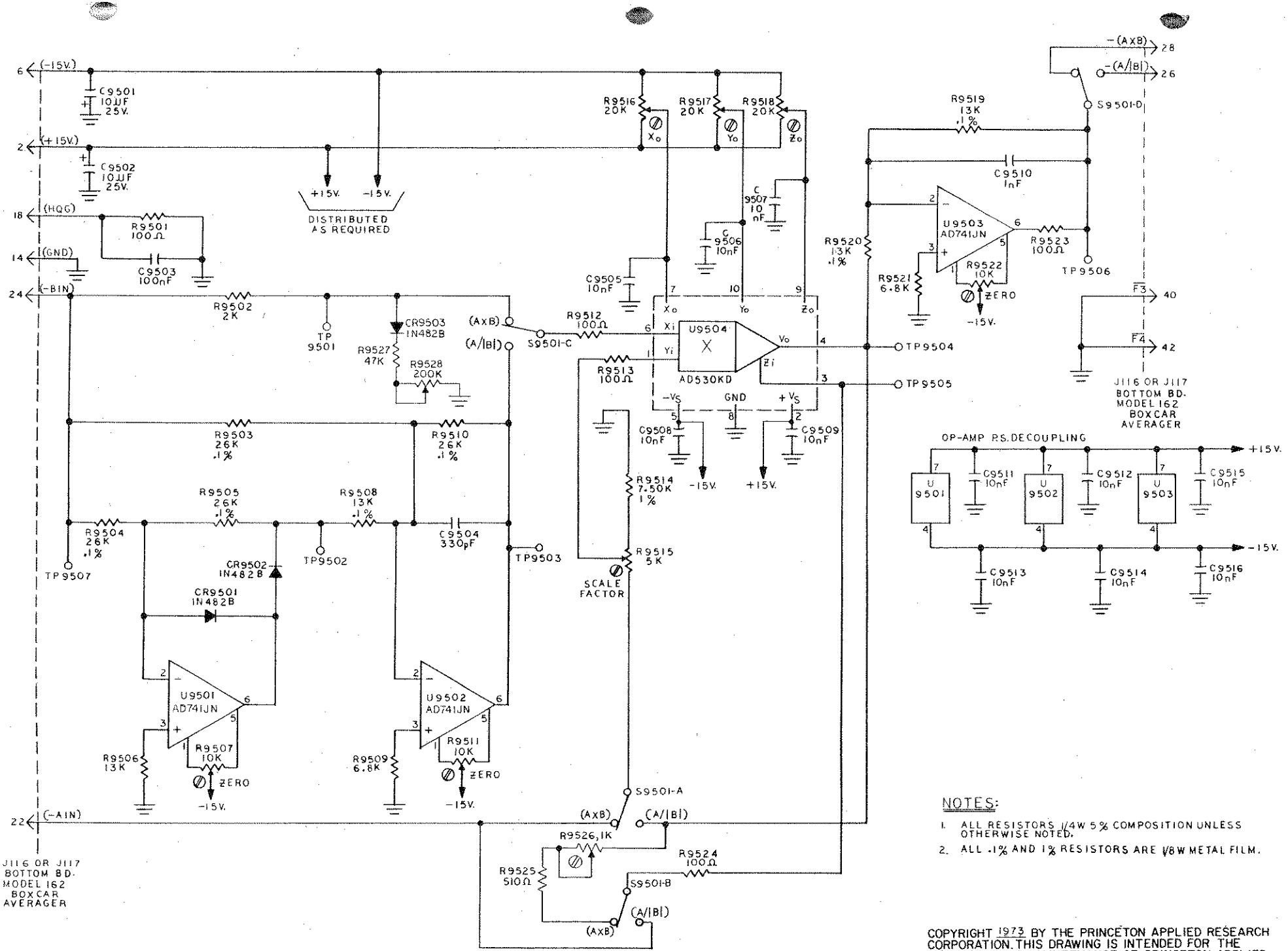
CHASSIS WIRING DIAGRAM

MODEL 162

7864 D SD



SYMBOLIZATION
MODEL 162/95
A X B OPTION BOARD

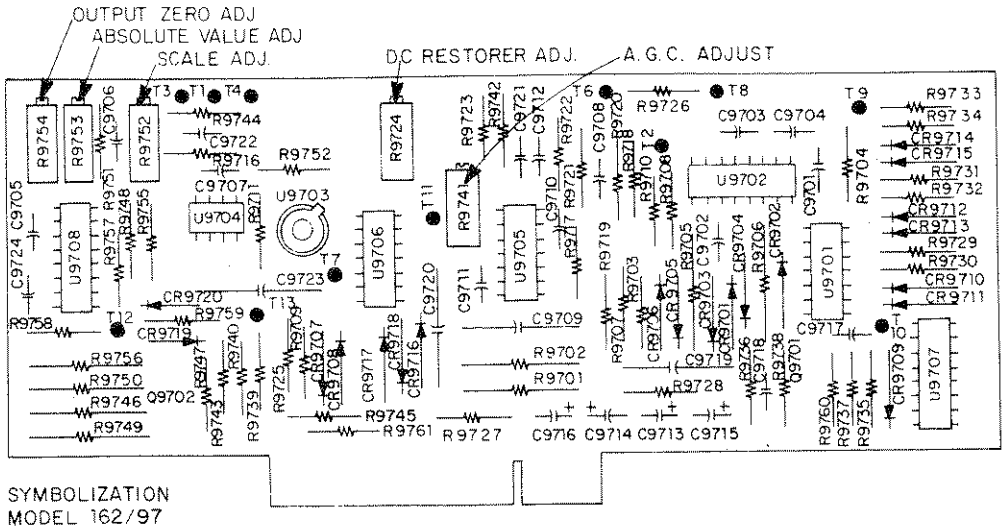


NOTES:

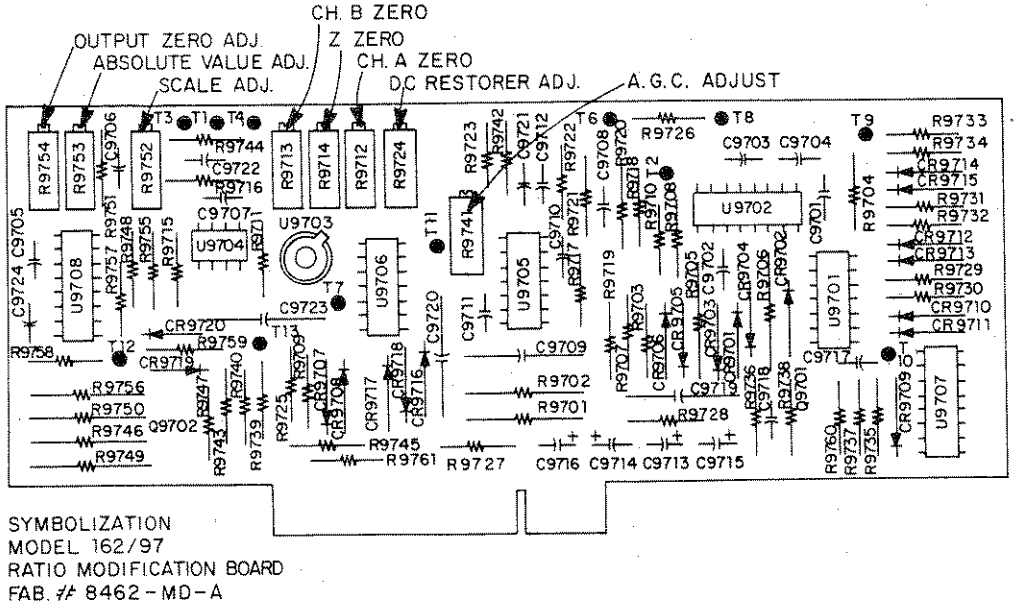
1. ALL RESISTORS 1/4W 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. ALL .1% AND 1% RESISTORS ARE 1/8W METAL FILM.

(AXB) OPTION BOARD

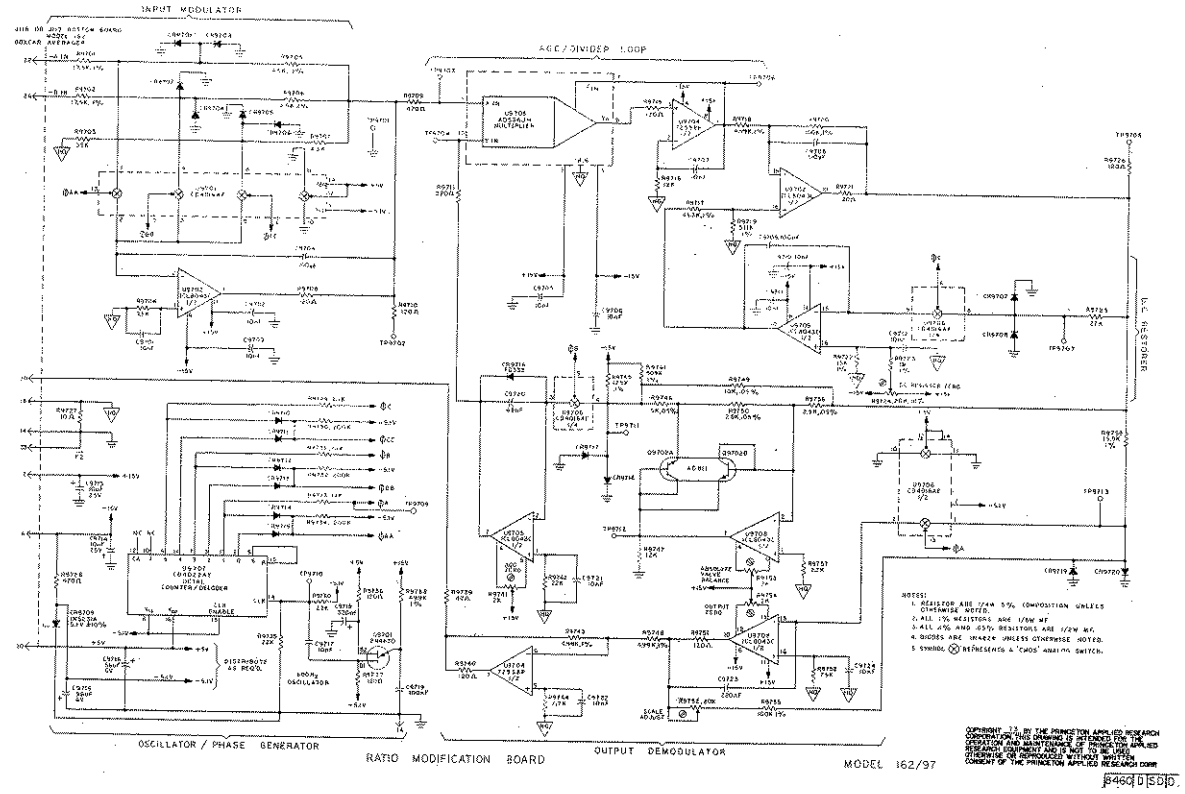
MODEL 162/95



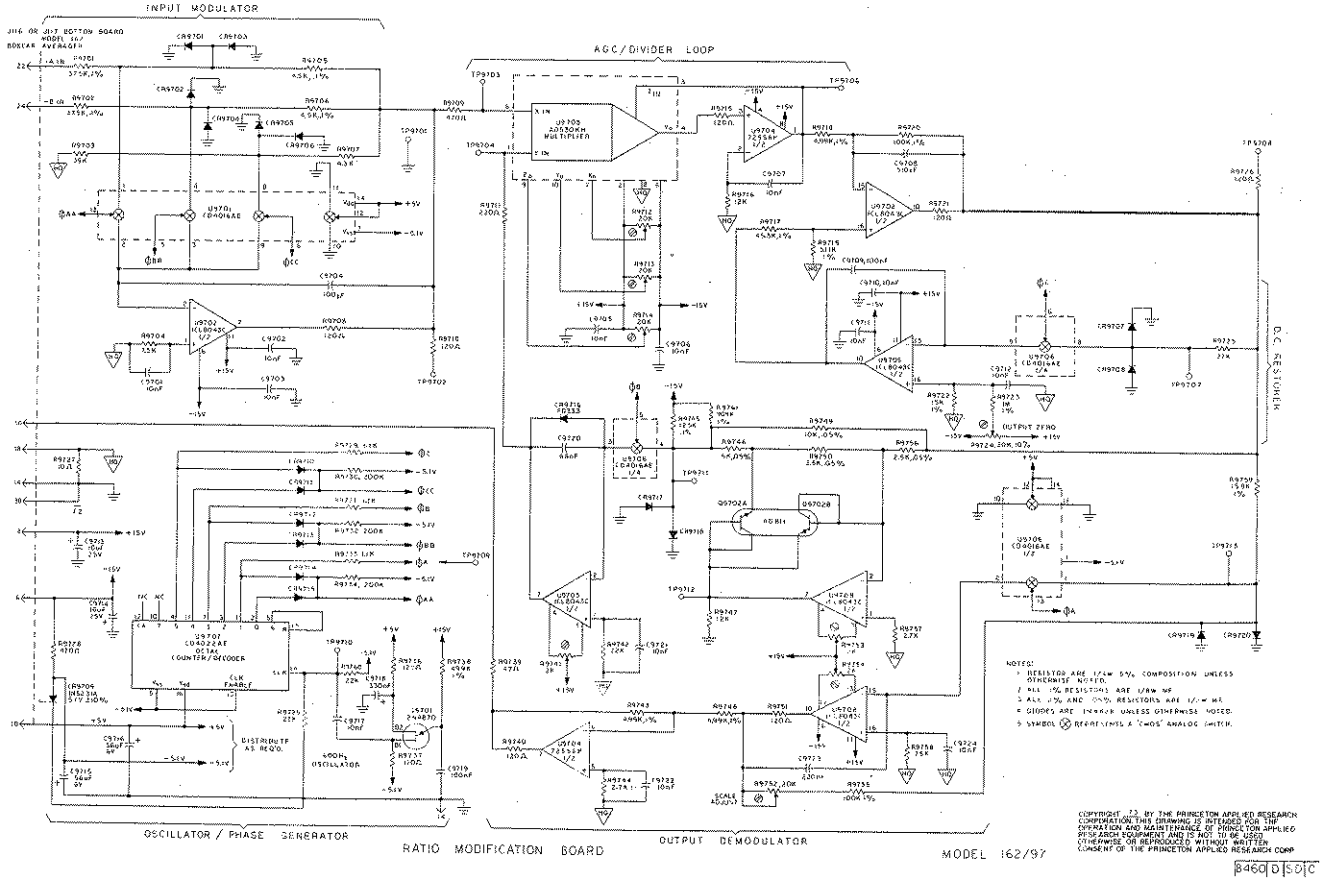
VERSION 2



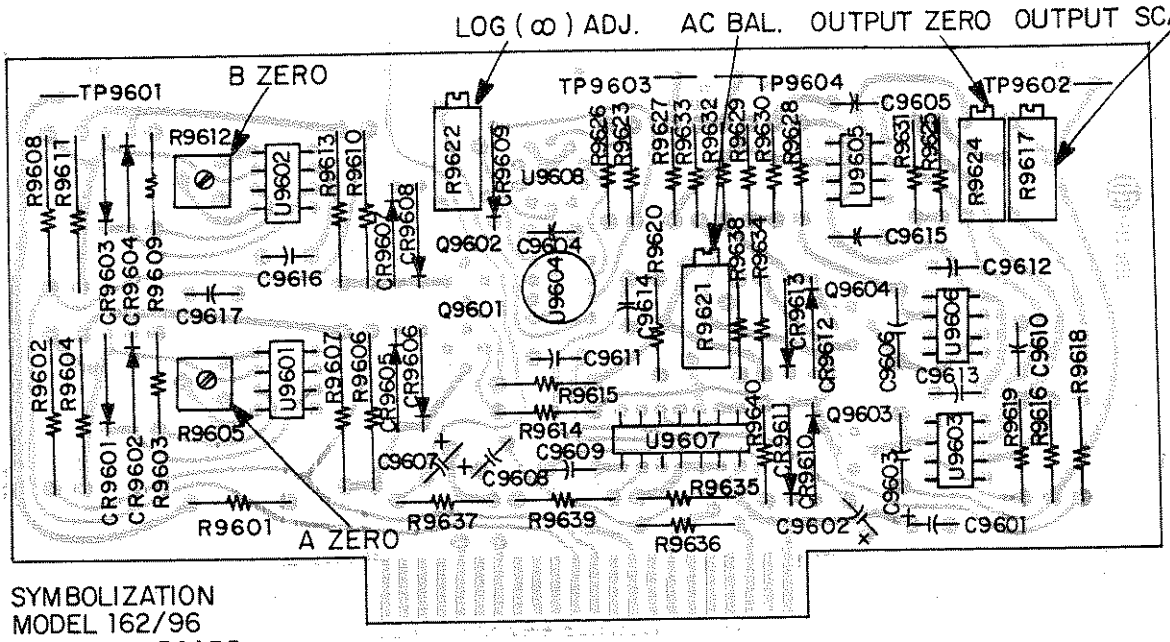
VERSION 1



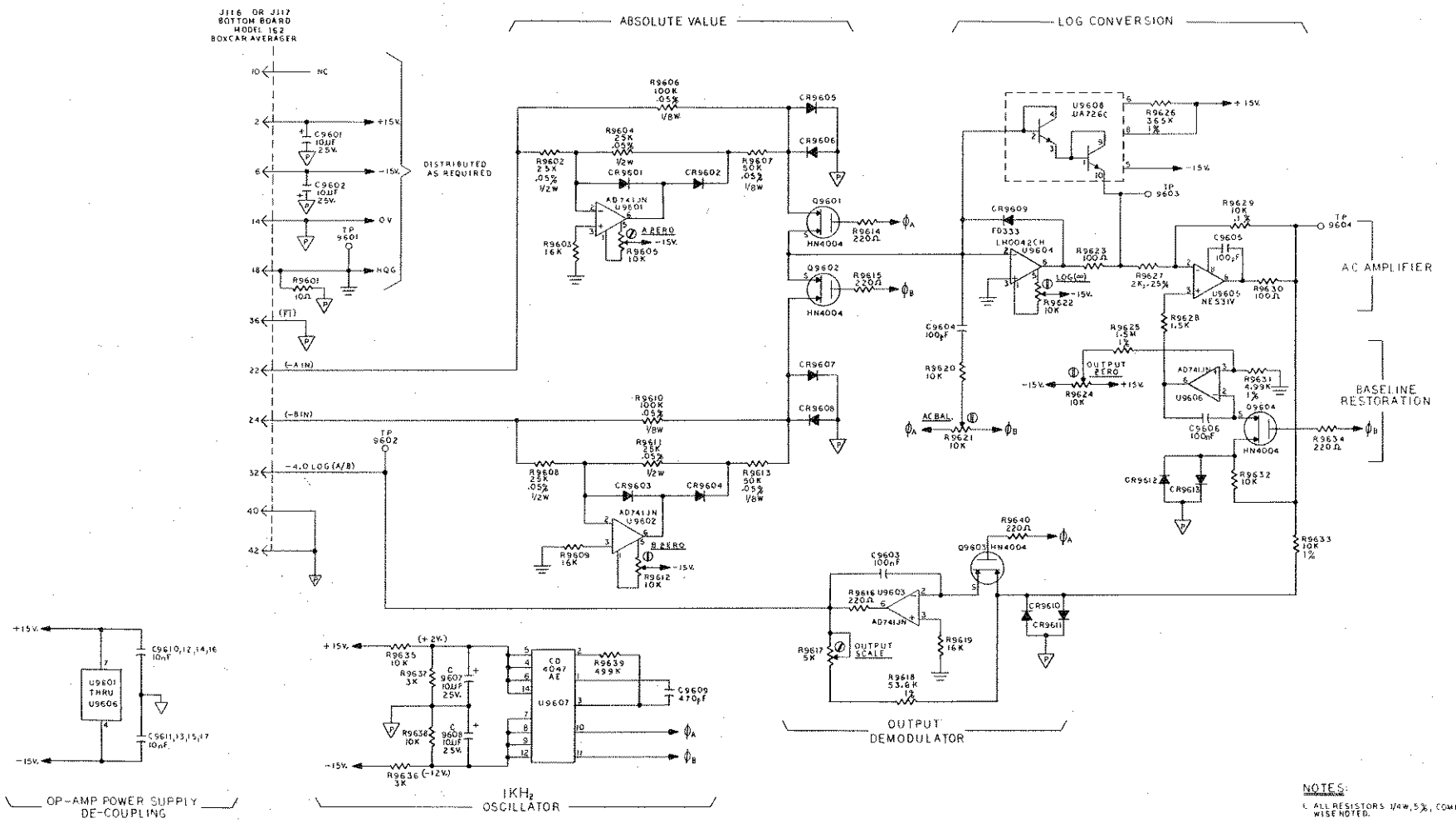
VERSION 2



VERSION 1



SYMBOLIZATION
MODEL 162/96
LOG RATIO BOARD



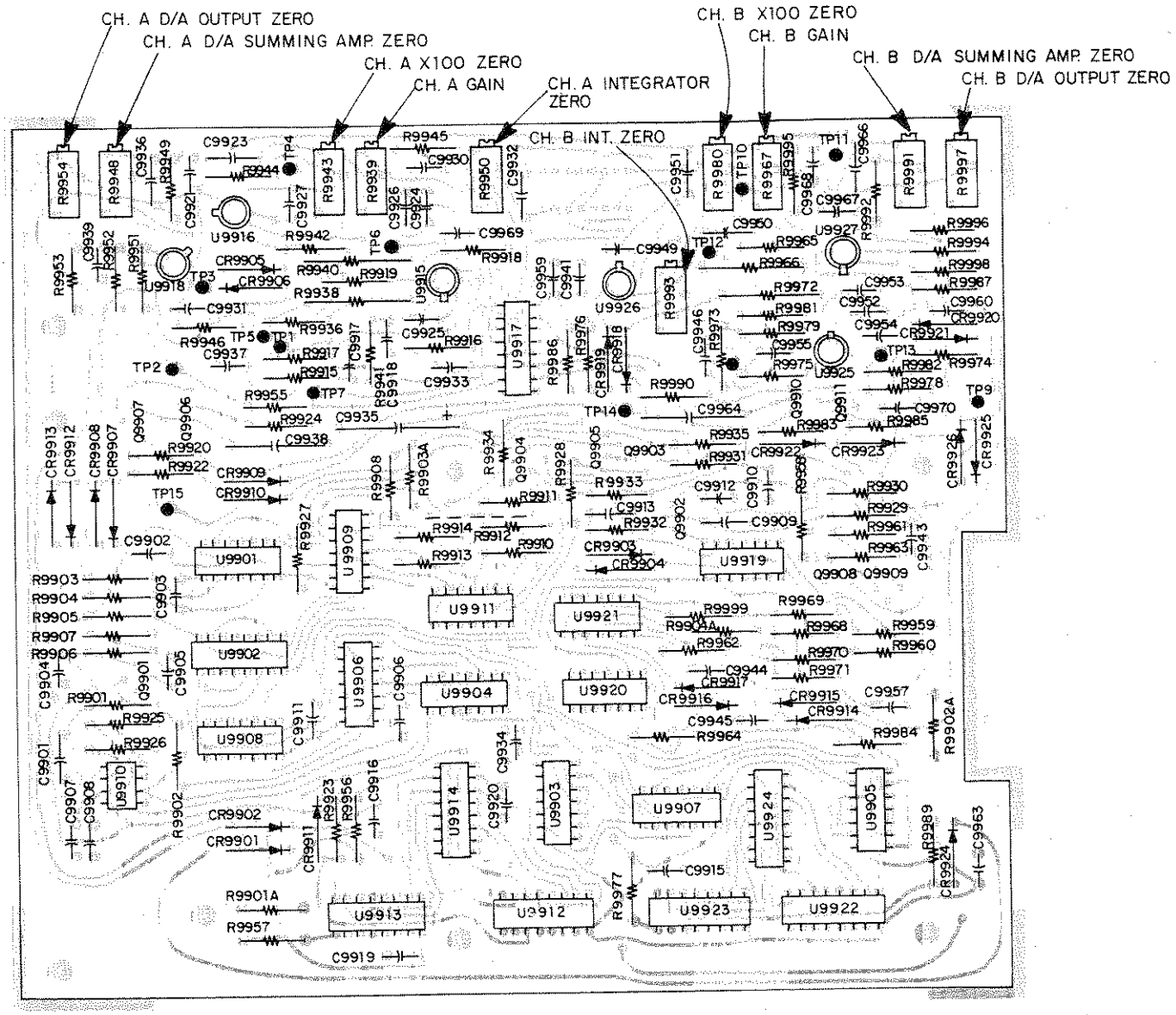
NOTES:

1. ALL RESISTORS 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. ALL 1%, .25%, AND .1% RESISTORS ARE 1/8W METAL FILM.
3. ALL .05% RESISTORS ARE 1/2W METAL FILM.
4. ALL DIODES ARE 1N482B EXCEPT CR9609 WHICH IS FD333.

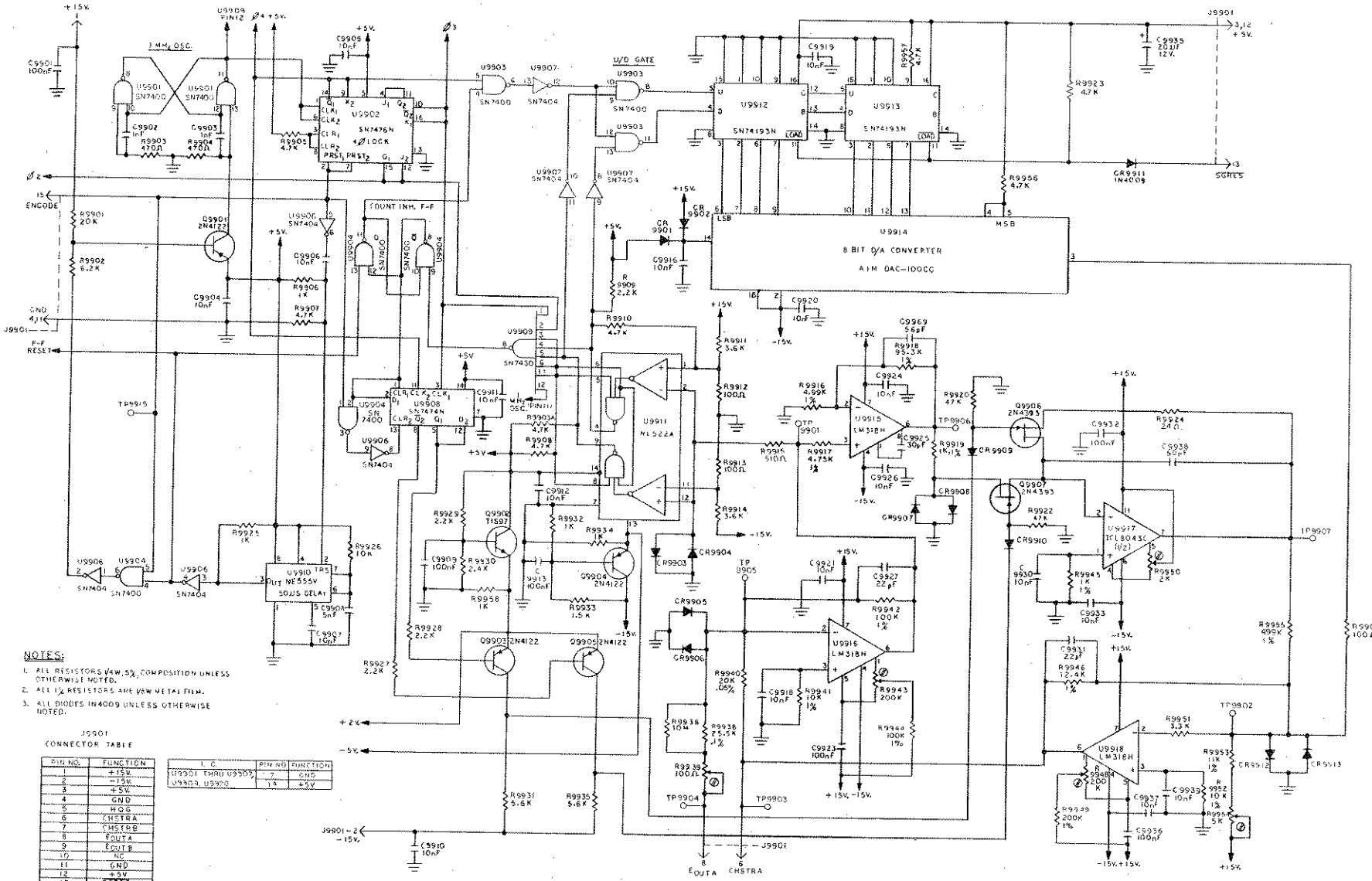
LOG RATIO BOARD

MODEL 162/96

8123 D SD A



SYMBOLIZATION
MODEL 162/99
DIGITAL STORAGE BOARD



NOTES:

1. ALL RESISTORS ¼W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. ALL 1% RESISTORS ARE ¼W METAL FILM.
3. ALL DIODES IN4009 UNLESS OTHERWISE NOTED.

J9901 CONNECTOR TABLE

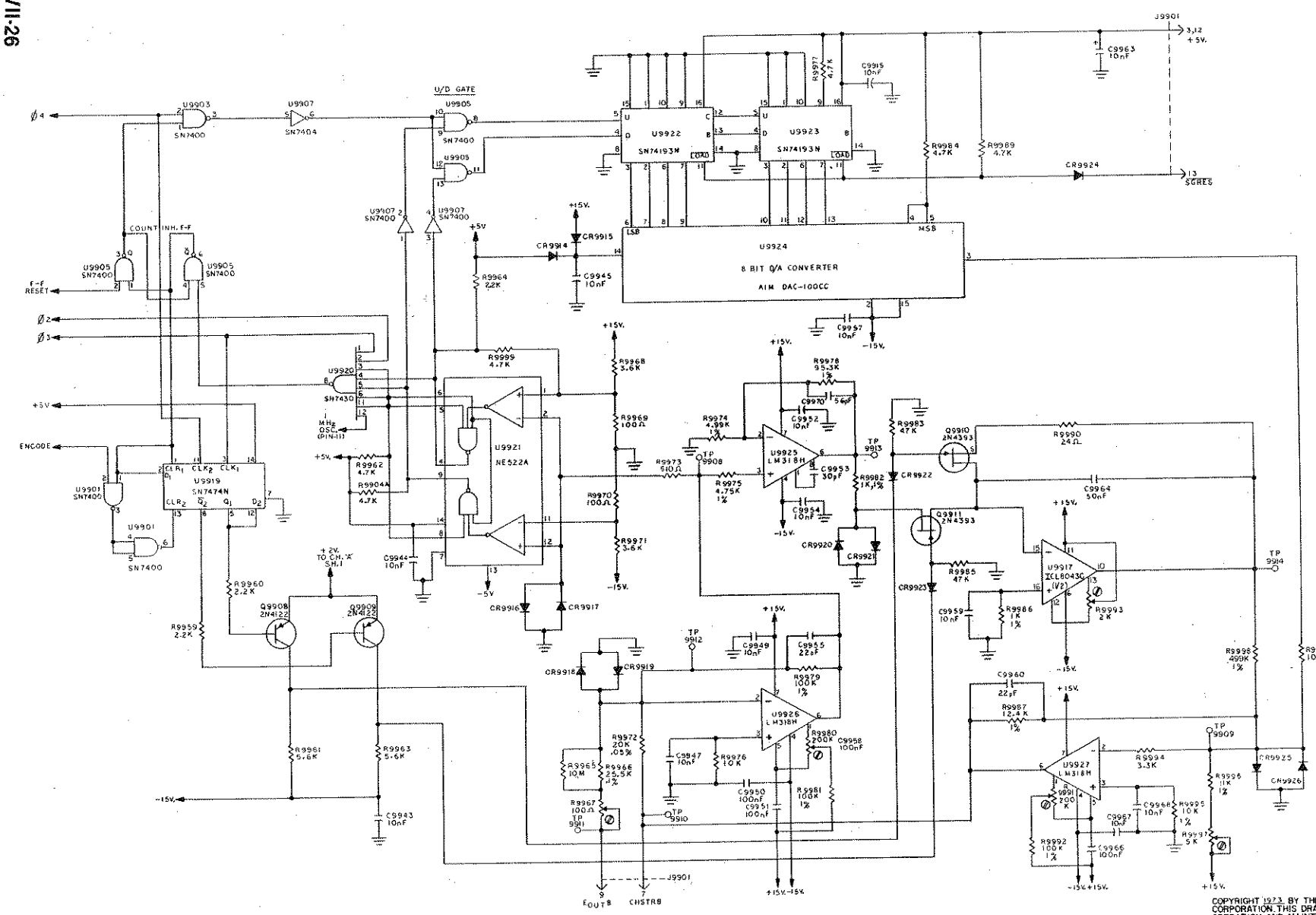
PIN NO.	FUNCTION
1	+15V.
2	-15V.
3	+5V.
4	GND
5	HOG
6	CHSTRA
7	CHSTRB
8	EOUTA
9	EOUTB
10	NC
11	GND
12	+5V
13	SGRES
14	F-F (GND)
15	ENCODE
16	NC

I. C.	PIN NO.	FUNCTION
U9901 THRU U9907,	7	GND
U9909, U9910	14	+5V

DIGITAL STORAGE BOARD
CHANNEL 'A'

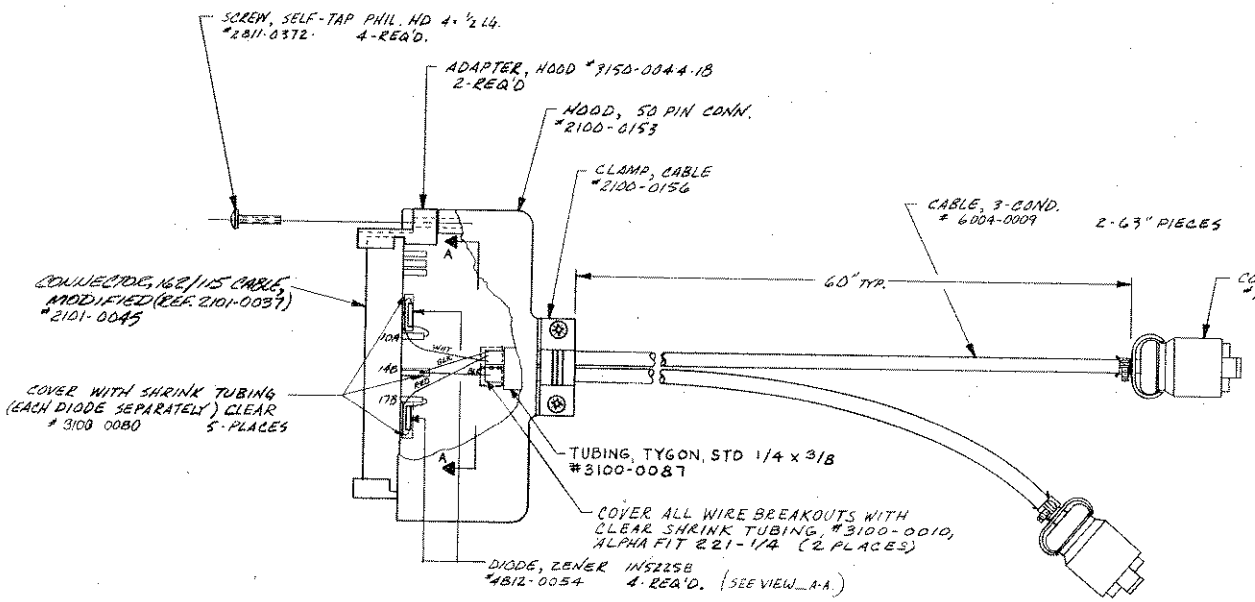
MODEL 162/99

SHEET 1 OF 2 | 6385 | D | SD | C



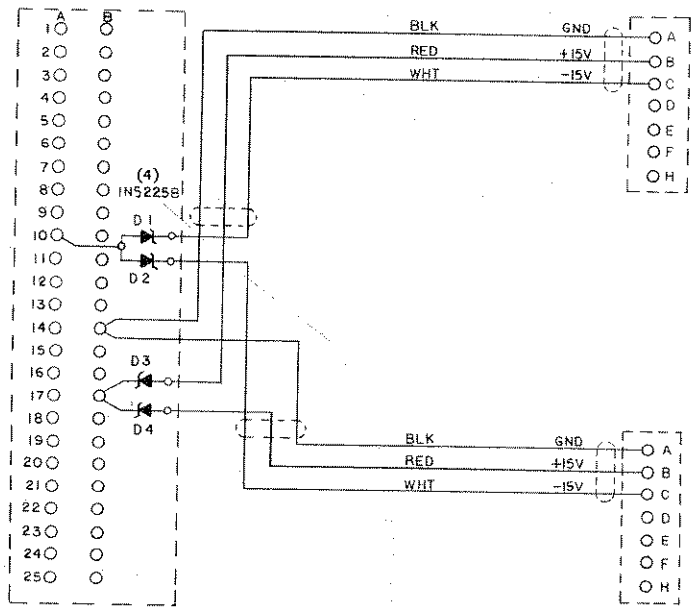
DIGITAL STORAGE BOARD
CHANNEL 'B'

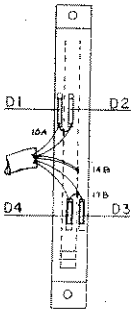
MODEL 162/99



NOTE

FOR BILL OF MATERIALS SEE MPL #6020-0132





VIEW A-A

APPROVED FOR PROCUREMENT

REV	ZONE	DESCRIPTION	DATE	BY	APPD
C2		CLEAR SHRINK TUBING #3100-0010 WAS BLK SHRINK TUBING #3100-0014. CORRECTED TYGON TUBING MFR 3100-0086 TO 3100-0087 ECN 4361	7/14/82	[illegible]	[illegible]
C1		UPDATE REV, HOOD & CLAMP WERE BRIDGE ECN 5909	9/15/81	DM	DM
C		ZENER DIODE INSTALLED #4812-0054 WAS INSTALLED #28-0049	7-1-80	JB	JAC
B		SHRINK TUBING #3100-0014 WAS GRAY #3100-0003. UPDATED EDP# CHECK PLOT 77-20. ECN 4360	6-4-79	FS	JAC
A		[illegible] ECN 4361	5-8-79	[illegible]	

UNLESS OTHERWISE NOTED

DEC. .00 ± .01 METRIC

DEC. .000 ± .005 FRAC. ± 1/64

SCALE NONE ANG. ± 1/2°

DRWN. DJS DATE 10.8.76

CHKD DATE 10/18/76

APPD DATE 10/28/76

TITLE

CABLE ASSEMBLY
M162/2, M-115 INTERFACE

PRINCETON APPLIED RESEARCH

MODEL NO. 162, 115

PART APPROVED FOR PROD QUOTE

PART NO. 6020-0132

PRINCETON APPLIED RESEARCH CORPORATION
P.O. BOX 2565
PRINCETON, N. J. 08540

DWG. NO. 11198-C-ESA

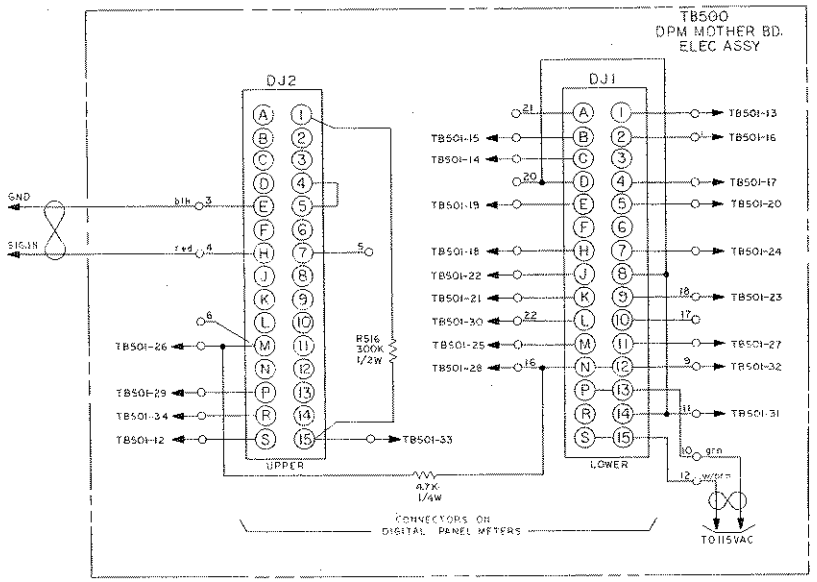
SHT 1 OF 1

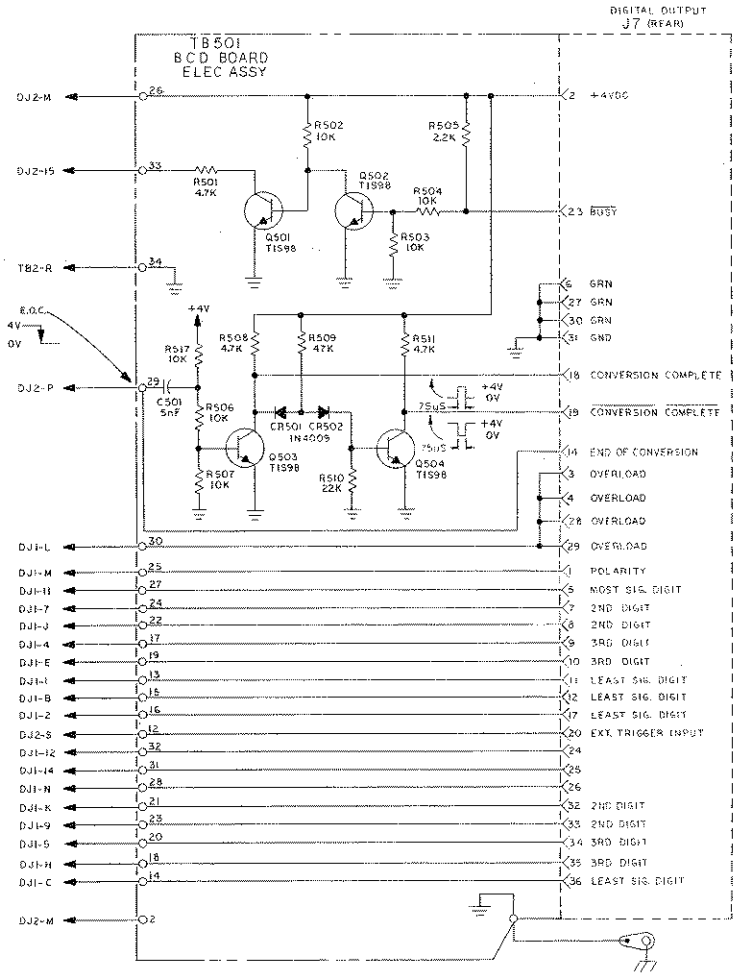
REV C2

C2 11198-C-ESA

REV SHT OF SHTS DWG NO.

VII-27





CHASSIS WIRING DIAGRAM
DIGITAL PANEL METER W/
BCD OUTPUT

MODEL 162/98

NOTES:
1 ALL RESISTORS 1/4W 5% COMP UNLESS OTHERWISE NOTED
2 ALL 1% RESISTORS 1/2W, METAL FILM.

3/26/79

EG&G PRINCETON APPLIED RESEARCH

SHT. 1 OF 1 12760 D SD

APPENDIX A
M164 P MAX AS A FUNCTION OF APERTURE DURATION AND TIME CONSTANT