T800-30-0000/0002 DFSK Modulators

8th September 2000

Applicability

This Technical Note (TN) applies to the fitting of T800-30-0000 and T800-30-0002 DFSK modulators in T800 Series II Exciters and Transmitters.

Introduction

The T800-30-0000/0002 is a Direct Frequency Shift Key (DFSK) Modulator designed as an auxiliary module to provide T800 Series II transmitters with DFSK capability, and is suitable for POCSAG or similar paging data formats. Analogue transmissions (e.g. tone or speech) are still possible by disabling the data path with control line S6. 512 or 1200 baud data rates are link selectable and reference frequency stability is ±2.5ppm from -30°C to +70°C.

The T800-30-0002 has additional circuitry for phase locking to an external reference oscillator for simulcast transmission. External frequency standards of 100kHz multiples up to 12.8MHz are link programmable and reference frequency stability is determined by the external standard. Otherwise the operation of the T800-30-0002 is identical to that of the T300-30-0000.

The T800-30-0000/0002 PCB is not designed for use with 66 to 88MHz equipment.

Note: The T800-30-0000 and T800-30-0002 were previously numbered T800-30 and T800-35 respectively. Some illustrations and diagrams in this technical note are used for both products and will therefore have labels referring to the T800-30/35.

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Parts Required

The T800-30-0000 kit should contain the following items:

1 x T800-30-0000 DFSK modulator board
1 x T800-03-0000 auxiliary D-range kit
1 x coaxial socket
1 x 47 ohm resistor SMD 0805
1 x terminated coaxial cable
4 x M3 x 8 Taptite Pan Torx screws
4 x cable ties
3 x cable clips

The T800-30-0002 kit should contain the following items:

1 x T800-30-0002 DFSK modulator board
1 x auxiliary D-range with coaxial socket
1 x coaxial socket
1 x 47 ohm resistor SMD 0805
2 x terminated coaxial cable
4 x M3 x 8 Taptite screws
4 x cable ties
3 cable clips

Installation

Caution: **The radio must be powered off for this modification. After modification, do not remove the coaxial lead from the socket unless the radio is powered off.**

1. Remove the TCXO (=IC700) from the synthesiser compartment of the T800 Series II transmitter.

   Fit the miniature coaxial socket (=SK710) and 47 Ohm SMD resistor (=R705) to the PCB pads provided beneath the TCXO, as shown in Figure 1.

Note: Keep the angle of the coaxial socket steep to ensure that there is space for the Micromatch cable as well as for the coaxial cable.

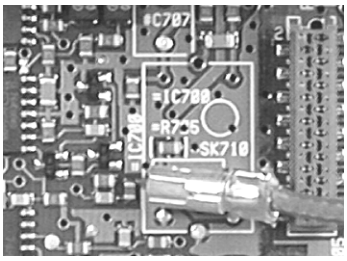

Figure 1 Location Of Socket And SMD Resistor

2. Remove the two screws and cover plate from the second D-range mounting hole at the rear of the T800 Series II chassis.

3. Remove C263 and R296 from the audio processor (shown in Figure 2), and clear the holes of solder.

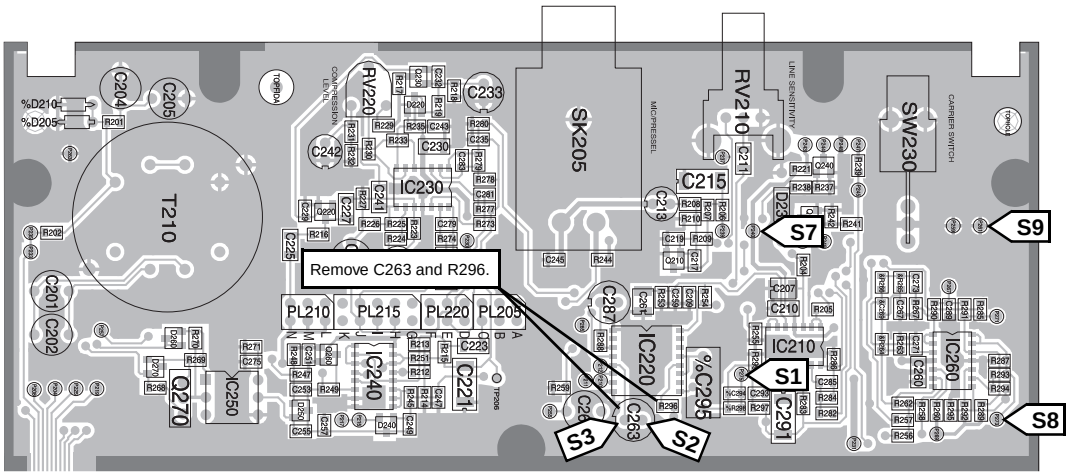

Figure 2 T800 Series II Transmitter Audio Processor - Top Side

4. Remove R841 and R842 (SMD) from the microcontroller compartment (shown in Figure 3) to disconnect the appropriate lines from the microcontroller.

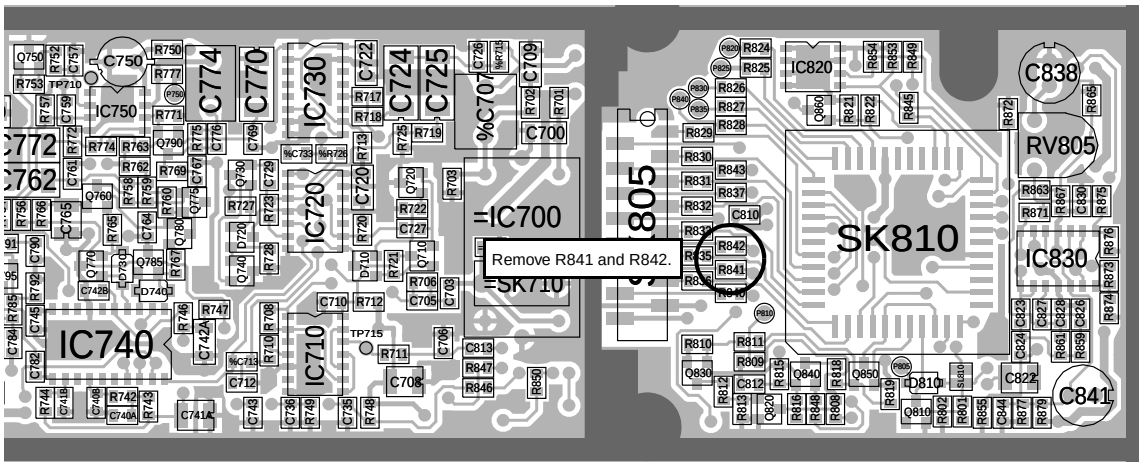

Figure 3 T800 Series II Microcontroller Compartment - Top Side

5. Lay the T800-30-0000/0002 PCB above the exciter compartment with the component side up and positioned so that the wires are facing the front panel of the radio.

   Twist the orange (T800-30-0002 only), yellow, green and blue wires together and secure with the cable ties provided.

   Route the wires and coaxial cable via the loom channel cast into the chassis to the synthesiser and D-range compartments as shown in Figure 4. Depending on the chassis type, there will be either holes in the chassis through which to pass the wires, or slots in the top of the chassis walls. If the wires are passed through slots, use cable clips to hold them in place.

Pass the wires through the D-range hole and connect to the auxiliary D-range plug (D-range 2) (later D-ranges have pads provided for the wires, as shown in brackets) as follows:

Wire	Length (mm)	Connection	Signal
yellow	370	S4 pin 13 (Y)	DATA
green	370	S5 pin 8 (G)	GROUND
blue	370	S6 pin 14 (B)	$\overline{\text{DATA}}$/SPEECH
orange[a]	370	S10 pin 10 (O)	LOCK DETECT

a. T800-30-0002 only

Table 1 D-range Wire Connections

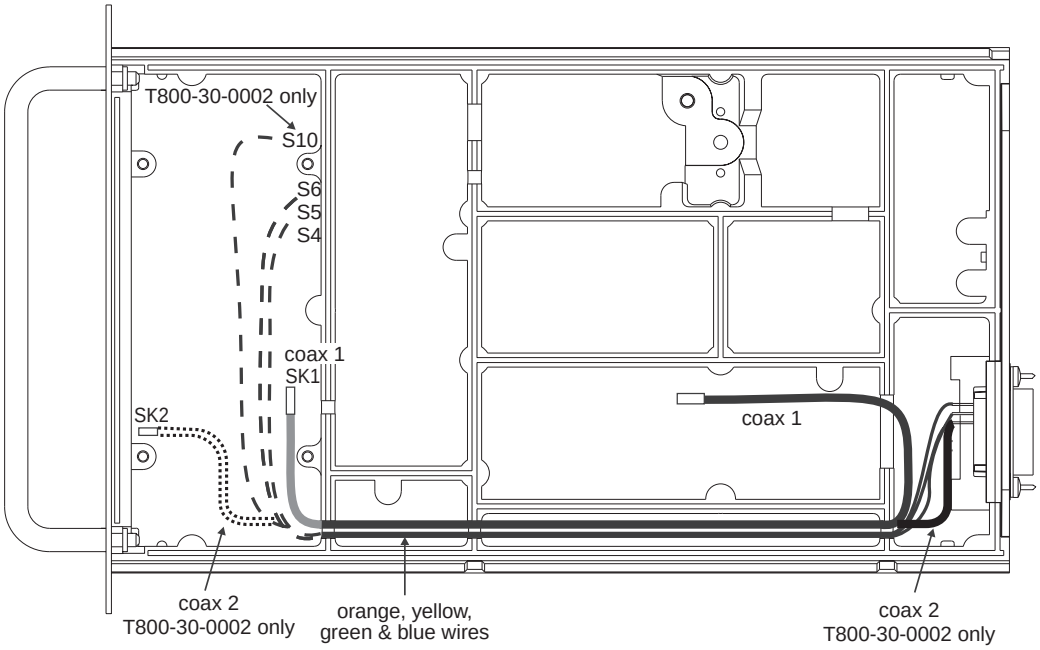

Figure 4 Cable Routing

6. Screw D-range 2 in place.

7. Connect the wires from the T800-30-0000/0002 PCB to the audio processor as follows (refer to Figure 2 and the Test Points & Options Connections drawing in the relevant service manual):

Wire	Length (mm)	Connection	
brown	150	S1	I/O Pad, P275 (POCR) between C295 and IC210
red	140	S2	positive side of C263
orange	190	S3	negative side of C263
purple	100	S7	I/O Pad, P240 (+9V) just below D230
grey	150	S8	I/O Pad, P273 (POCI)
white	205	S9	I/O Pad, P261 (GND)

Table 2 Audio Processor Wire Connections

8. The T800-30-0000/0002 PCB links are set for UHF operation and 512 baud data rate. For the location of the PCB links refer to Figure 5.

   For 1200 baud rate, solder short LINK2.

   For VHF operation, solder short LINK3, LINK4 and LINK5.

   T800-30-0002 only: To set the links for the external oscillator frequency, solder short the links as follows:

1MHz reference	LINK10, LINK11, LINK12, LINK7, LINK9.
5MHz reference	LINK10, LINK6, LINK7, LINK9.
10MHz reference	LINK12, LINK6, LINK8, LINK9.

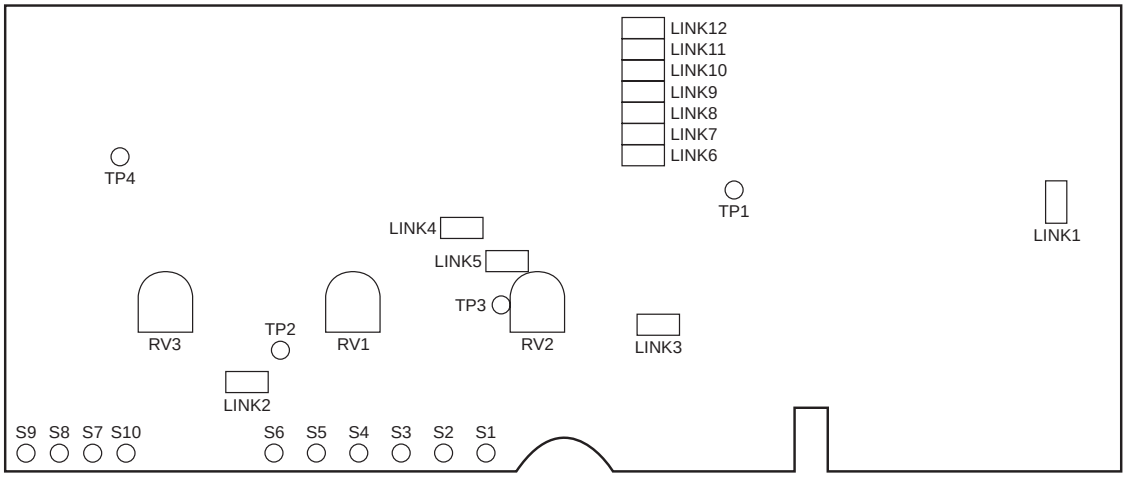

Figure 5 T800-30-0000/0002 Link Location - Top Side

To set the links for 12.8MHz reference, use the following method:

- Cut pin 18 (shown in Figure 6) approximately half way down the pin and bend it away so that its logic level floats high.

Caution: **Do not cut the pin too close to IC15 if you are likely to reverse the procedure in the future to enable different reference frequencies to be applied.**

- Solder short the links as follows: LINK6, LINK7, LINK8, LINK9, LINK10, LINK11, LINK12.

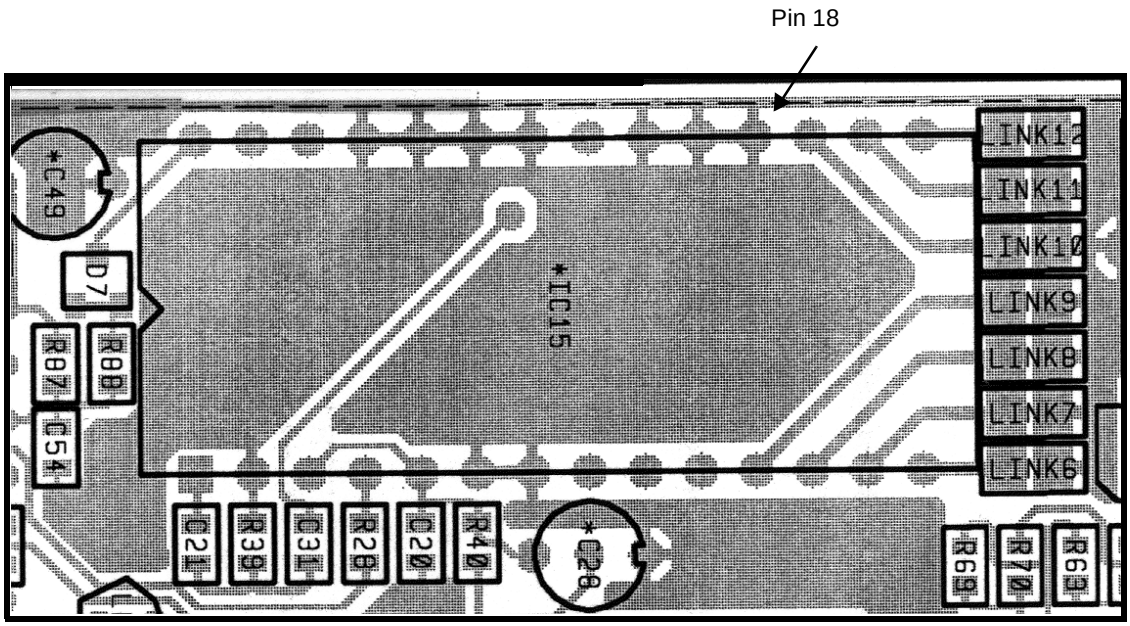

Figure 6 T800-30-0002 Location of Pin 18 - Top Side

If other external oscillator frequencies are required, the link code can be calculated using the following method:

- Divide the external oscillator frequency by 100kHz.
- Convert the result into binary.
- Program the T800-30-0002 PCB links 6 to 12 as shown, using the calculated binary number.

MSB						LSB
N6	N5	N4	N3	N2	N1	N0
LINK10	LINK11	LINK12	LINK6	LINK7	LINK8	LINK9

Table 3 Link Selection

Note: A shorted link represents ‘logic 0’ and an open link represents ‘logic 1’.

9. Connect the coaxial cable provided between SK1 on the T800-30-0000/0002 PCB and =SK710 on the T800 Series II transmitter PCB, as shown in Figure 4.

10. **T800-30-0002 only:** Connect the other coaxial cable between SK2 on the T800-30-0002 PCB and the auxiliary D-range.

11. Position the T800-30-0000/0002 PCB above the audio processor compartment, with the wires and components facing down.

    Screw in place using the 4 M3 x 8 screws provided.

Adjustment

It is preferable to set up the T800-30-0002 with an applied external standard, otherwise the slave VTCXO on the T800-30-0002 will not be locked. However, the adjustment procedure for setting the modulator levels will still be valid.

External Standard Lock Confirmation

1. Check that the T800-30-0002 PCB links 6 to 12 are set to equal the external frequency standard.

2. Apply an external frequency standard at an output level of about 1Vp-p (+4.0dBm, 50 ohm). Levels from 0 to +10dBm are acceptable.

3. Confirm that phase lock has been achieved by checking with an oscilloscope that the 'LOCK DETECT' line on pin 3 of the second D-range plug switches to below 0.2V.

Modulator Adjustment

For speech modulator and data modulation adjustment with a T800-30-0000/0002 DFSK modulator PCB, carry out the following instructions instead of the audio processor modulator adjustments in Section 3 of the service manuals. Carry out the limiter adjustments as described in the service manuals.

During adjustment ***do not*** provide an input on the $\overline{\text{DATA}}$/SPEECH terminal (S6).

The audio test frequencies used are as follows:

Transmitter	Frequency 1	Frequency 2
T836/7	120Hz	600Hz
T856/7	100Hz	300Hz

Table 4 Audio Test Frequencies

Note: Deviation settings are given first for wide band radios, followed by settings for narrow band radios in brackets [ ].

Speech Modulator Adjustment

1. Inject an audio signal of frequency 2 at approximately +5dBm (1.4Vrms, 600 ohm) into the CTCSS input (D-range 1 pin 8) and earth the key line.

2. Adjust the audio generator output to obtain ±3kHz [±1.5kHz] peak deviation at frequency 2.

3. Change the audio generator frequency to frequency 1 and adjust RV3 (reference deviation speech) on the T800-30-0000/0002 PCB to obtain ±3kHz [±1.5kHz] peak deviation.

4. Change the audio generator input frequency back to frequency 2 and repeat steps 2 and 3 until the deviations achieved at the two input frequencies are within 0.2dB of each other.

   You will need to do this at least four times.

Data Modulation Adjustment

1. Inject a 100Hz 1:1 square wave into S4 of the T800-30-0000/0002 PCB (D-range 2 pin 13) of at least 5Vp-p, to simulate a data input.

2. Monitor the carrier FM with a modulation meter via a suitable attenuator (if necessary), and observe the modulation level.

3. Monitor the control line of the VCO (pin 1 on the VCO PCB) with an AC coupled oscilloscope set to a sensitivity of at least 20mV/div with the time base set to 2ms/div.

4. Adjust both RV1 (VCO modulation) and RV2 (reference modulation) on the T800-30-0000/0002 PCB to achieve a flat topped square wave on the oscilloscope, corresponding to ±4.5kHz peak on the modulation meter.

   You may need to repeat this procedure several times.

   Figure 7 shows a typical 100HZ VCO control line waveform with RV1 and RV2 set correctly.

Note: Be aware that if the lower cut off frequency of an AC coupled oscilloscope is too high, excessive distortion may be introduced which will result in 'sag' on the square wave displayed. Determine if this is a problem by directly monitoring the original square wave source and observe any sag.

If there is sag, switch the oscilloscope to DC and use a 10µF capacitor in series with the scope probe (observing the correct polarity) to directly monitor the VCO control line. Note that the trace settling time will be approximately one minute.

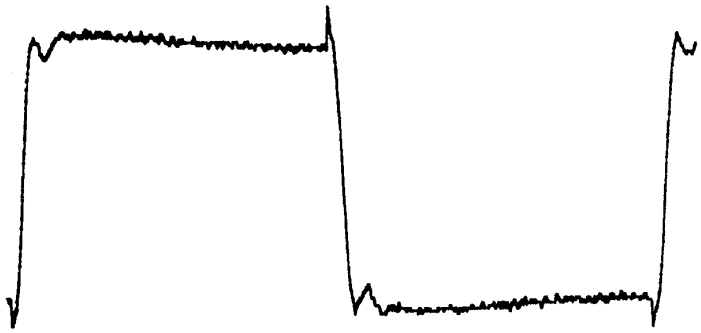

Figure 7 100Hz VCO Control Line Waveform

$\overline{\text{DATA}}$/SPEECH Input

With S6 low, data mode is enabled. If no data is present, the DFSK modulator defaults to speech mode. However if S6 is high, only speech mode is enabled, regardless of the presence of data.

Circuit Operation

Circuit Overview

The potential problem with achieving direct FSK modulation of a frequency synthesiser is that the modulation must go down to DC. This is in order to cope with the long rows of either zeros or ones which occur in an invariant data stream. The lowest cut off frequency can be extended downwards by employing dual point modulation which is the simultaneous modulation of both the VCO and the frequency standard. The T800 employs a phase modulator to modulate the frequency standard and a phase modulator inherently cannot extend down to DC.

A frequency standard with the required temperature stability which can be directly modulated is not available. The T800-30-0000/0002 therefore utilises a VCXO which is able to be modulated and which is referenced to the on-board TCXO. However a direct control loop would again prevent DC modulation. To overcome this, the control loop is disabled when the data is invariant. A simple retriggerable monostable with a period equal to the data bit period is used to detect data transitions. The monostable output enables the control loop, so that a 0-1-0-1 data sequence would continuously enable the loop. When the data is invariant, the control line of the VCXO is effectively frozen. This process ensures that no net DC component is introduced by the data onto the control loop when it is enabled.

In the T800-30-0000/0002, the VCXO is phase locked to the TCXO only in the speech mode. For data mode, the control loop is used in the AFC mode. This is because the noise which would be generated by switching the phase lock loop on and off using the monostable is unacceptably high. However, in the AFC mode, this additional loop noise is minimal. The AFC loop holds the VCXO on frequency to within a small fraction of a part per million. The following circuit description explains the difference between the two modes of basic control loop operation: AFC mode and phase lock mode. Phase lock is the default mode when no data is present. AFC mode operation is automatically enabled as soon as data is present.

AFC/PLL Operation

In the T800-30-0000/0002, the TCXO is the default frequency standard. In the absence of data, the slave 12.8MHz VCXO (Q1 etc) is phase locked to the TCXO. Both the TCXO and the VCXO outputs are clipped in IC1 and IC2 and frequency divided by 4 in the twisted ring counters, IC3 (TCXO) and IC4 (VCXO). The slave VCXO is also fed to the main T800 synthesiser via a low pass filter (C8 and L2) to replace its standard TCXO.

Each twisted ring counter provides four divide-by-four outputs, the Q and not-Q of each JK having relative phases 0, 90, 180 and 270. These signals are combined in the two exclusive OR gate phase discriminators in IC5, so as to provide two beat frequencies which are in phase quadrature, before phase lock is achieved. Both these outputs are passed through a low pass RC filter to remove the sum frequency of 6.4MHz and to pass the low beat frequency 5V p-p triangular wave. The output from pin 8 of IC5 is then passed through a differentiator (R48, C37 and IC11 pin 6 through to pin 7) to provide a further 90 phase shifted square wave output. The amplitude of the output is proportional to the frequency difference. This output is then inverted (R66 and IC11 pin 2 through to pin 1) to provide two complementary outputs.

The triangular output from IC5 pin 11 passes through an RC filter and is amplified (R41 and IC12 pin 5 through to pin 7) to just less than 9V p-p and clipped (R58 and IC12 pin 9 through to pin 8) to 9V p-p square wave. This square wave is either in phase or inverted with respect to the square wave output from the differentiator, depending upon whether the VCXO frequency is higher or lower than the TCXO frequency. The clipped output is inverted via two NOR gates (IC6 pins 5, 4 and 9, 10) which gate the CMOS switches at IC7 pins 5 and 13.

The output from these switches (IC7 pins 2 and 3) is therefore a full wave rectified direct voltage from the two complementary outputs of the differentiator, measured with respect to the half wave voltage available at pin 14 of IC12. It has a relative amplitude and sense proportional to the beat frequency and as such provides an AFC voltage which is fed via R75 to an integrator (IC11 pin 9 through to pin 8). This output feeds to a summing operational amplifier (IC11 pin 13 through to pin 14), which is the control line of the VCXO. This negative feedback loop therefore ensures that the fullwave rectified direct voltage, fed via the integrator, is reduced to close to zero. This corresponds to a very low frequency error between the VCXO and the TCXO.

This is the AFC mode operation of the control loop and must not be confused with the phase lock mode, which is the default mode in the absence of data. In the phase lock mode of operation, the CMOS switch between pins 10 and 11 of IC7 is closed and the switch between pins 9 and 8 is open. The integrator is therefore exposed to the combined output of the AFC loop and the amplified exclusive OR output, via R60 and R61, ensuring that phase lock of the VCXO to the TCXO is achieved.

Data Processing

1. Data Path

The incoming data enters via terminal S4 through the RS232 interface buffer Q2 and optional data inverting exclusive OR gate, IC5 pin 3. The data is level translated via buffer IC10 pins 6 and 7. Pin 6 feeds the data via a low pass data filter (IC12 pin 1 and RV2) and a CMOS switch (IC8 pins 10 and 11) via R77 to a summing operational amplifier (IC11 pin 13 through to 14). The data signal is therefore added into the AFC mode control loop to achieve data modulation of the VCXO. The data output from IC10 pin 7 provides direct modulation of the main T800 synthesiser VCO via RV1, R16, a CMOS switch (IC8 pins 1 and 2), terminal S2 and the subsequent T800 processing.

2. Data Monostables

The data output from IC5 pin 3 is also processed through three monostables. The first is formed by the exclusive OR gate IC5 output pin 6. An RC time constant (R47, C34) delays the data to IC5 pin 5 so that narrow positive pulses are generated at pin 6, coincident with both positive and negative edges of the data. These pulses are level translated via IC10 pin 3 to trigger two parallel monostables operated in the retriggerable mode. The data present monostable in IC9 output pins 9 and 10, has a nominal 100ms period. When data is present it remains in the active triggered state. In this state it:

Enables only the AFC mode by switching the two CMOS switches (IC7 pins 6 and 12) on and off, respectively.

- Enables the data transition monostable (IC9 output pin 6) by removing the reset at pin 3.
- Enables data modulation of the main synthesiser VCO via the CMOS switch (IC8 pin 13) and disables the audio path via the CMOS switch controlled by pin 5.
- Enables the data modulation of the summing operational amplifier by switching on the CMOS switch in IC8 control pin 12.
- Disables the audio modulation of the VCXO by turning off the CMOS switch in IC8 pin 6.

The data transition monostable has a monostable period approximately equal to the data period for both 512bds and 1200bds, set up by link 2. Each time a data edge transition occurs, the monostable enables the AFC CMOS switches for a bit period, via the NOR gates in IC6 (pins 1, 3 and 6, 8). If the data has a long row of zeros or ones, the monostable is not triggered, the AFC is temporarily disabled and the integrator remains in a 'frozen' state. This ensures that the VCXO is not pulled off frequency during these periods. If the data toggles at its maximum rate, the AFC loop is permanently enabled.

If edge transitions are absent for longer than 100ms, the POCSAG data stream is terminated and the data present monostable is not triggered. AFC, via IC6 pin 2, and the phase lock mode are then permanently enabled until the next data stream commences.

The required data dual point modulation is set up via RV2 for the VCXO and RV1 for the VCO.

The $\overline{\text{DATA}}$/SPEECH terminal, S6, forces the data mode to be disabled if speech is selected.

Speech Operation

The unit defaults to the speech mode when no data is present or when speech is selected by a high level on terminal S6. The audio path to the synthesiser is enabled to the synthesiser via the CMOS switch in IC8 pin 5.

The phase modulator in the main T800 is disabled and the dual point modulation is achieved by modulating the VCXO via the CMOS switch in IC8 control pin 6. The dual point modulation of the audio is set up by RV3.

T800-30-0002 PCB

In the T800-30-0002 the standard TCXO is replaced by a VCTCXO as detailed in the circuit diagram variant table. This is so that the VCTCXO can be phase locked to an external frequency set up by the links 6 to 12. The external signal is fed to the synthesiser IC15 pin 1 and divided down to a reference frequency of 100kHz. This is compared with the VCTCXO fed into pin 27 of the synthesiser IC where it is divided by 128 to also provide 100kHz.

The synthesiser three state phase discriminator output, pin 4, is fed via R28 to an integrator (IC14). Its output, via a low pass filter (R29 and C24), is the control line for the VCTCXO.

The second operational amplifier in IC14 is a lock detect comparator and is fed by pin 28 (LD) of the synthesiser to provide a 9V logic level from IC10 pin 13 when out of lock and 0V when locked.

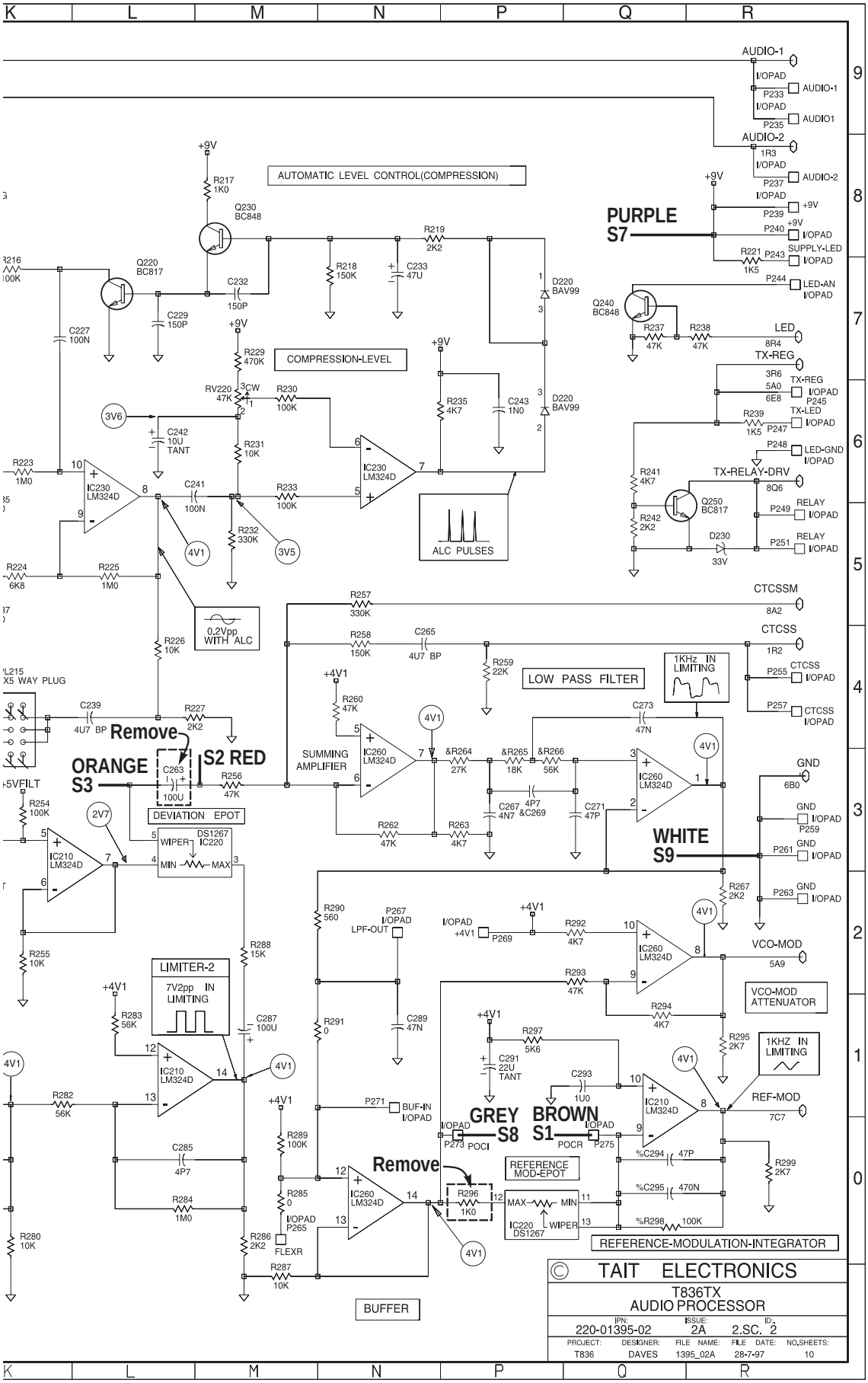

Figure 8 T800 Series II Transmitter Audio Processor Circuit Modifications

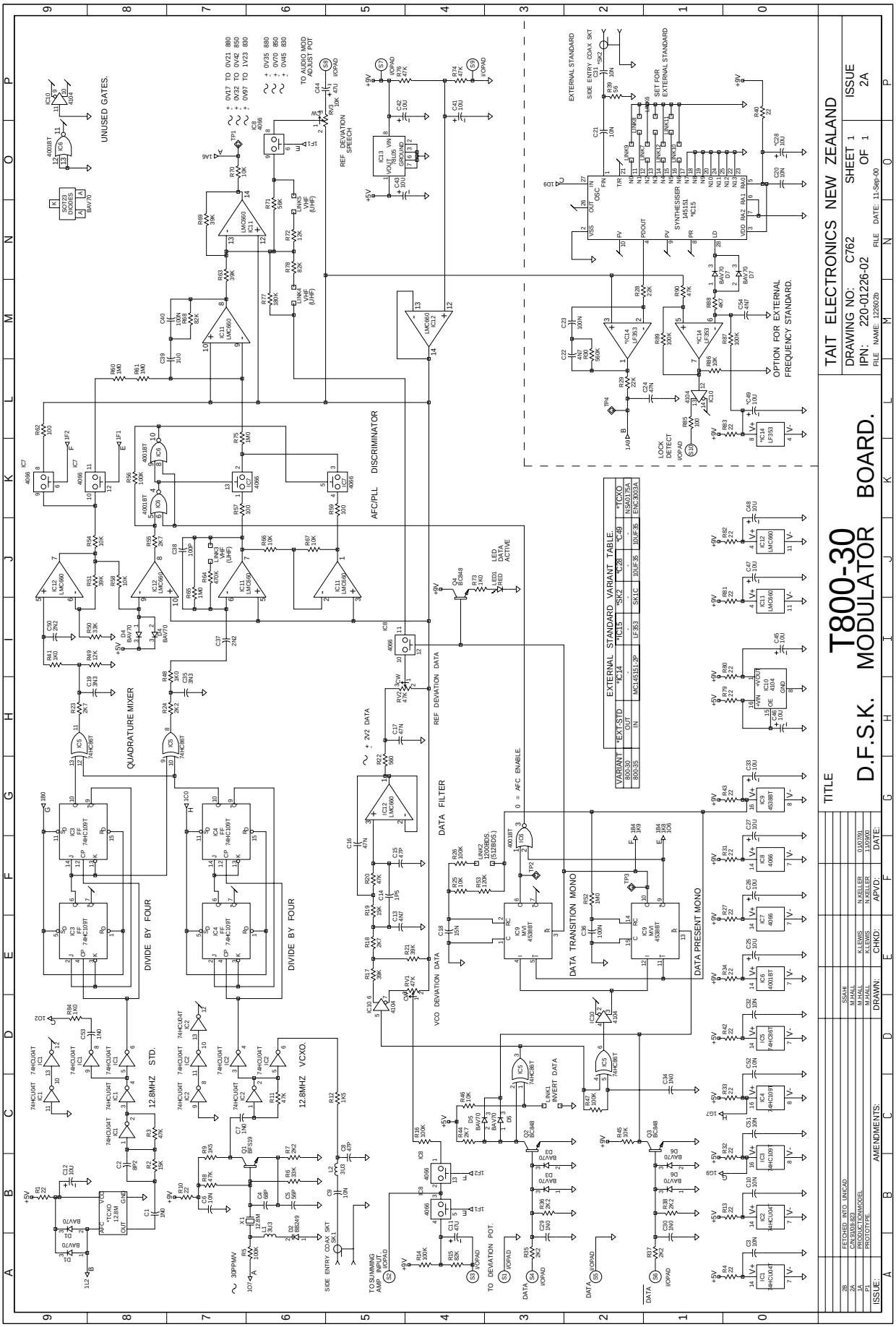

Figure 9 T800-30-0000/0002 Circuit Diagram (IPN 220-01226-02)

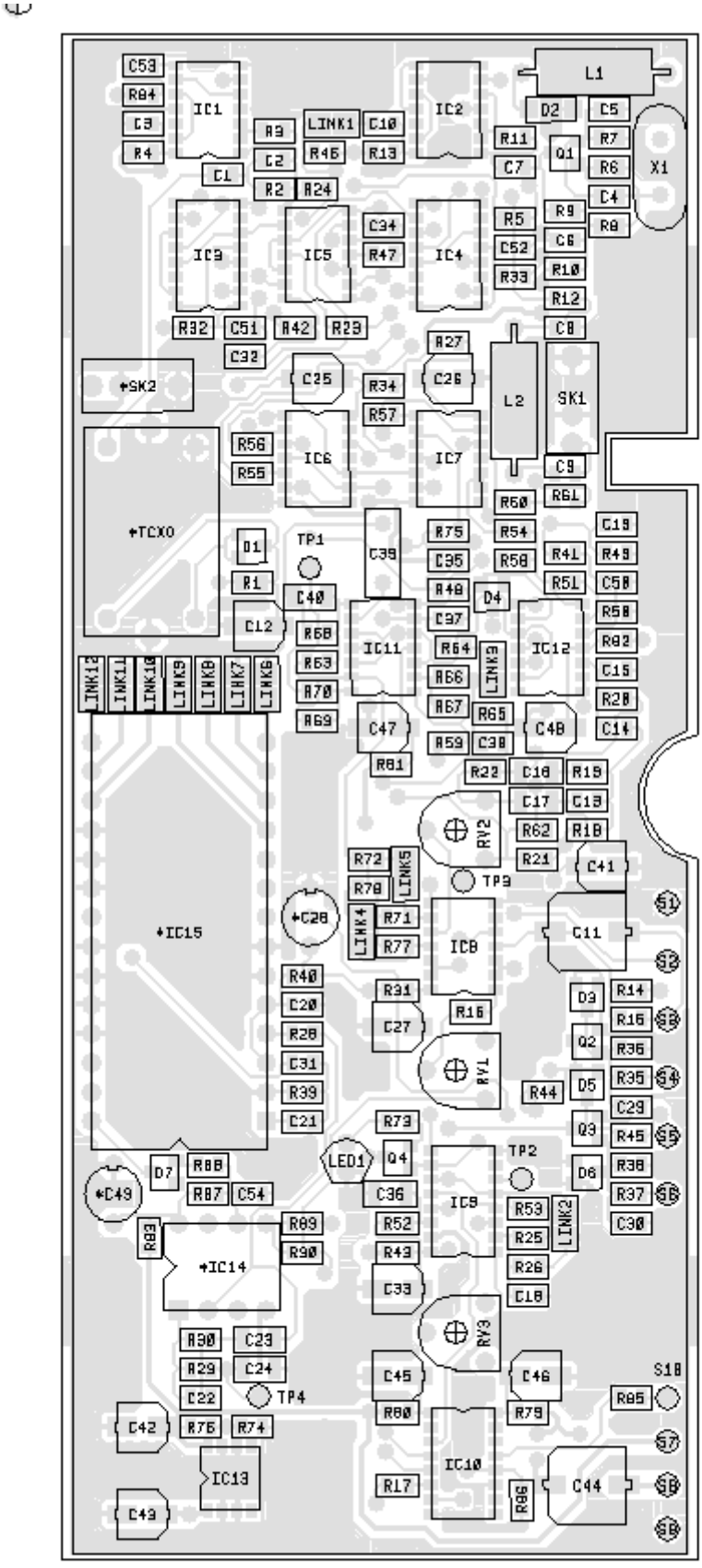

Figure 10 T800-30-0000/0002 PCB Layout - Top Side (IPN 220-01226-02)

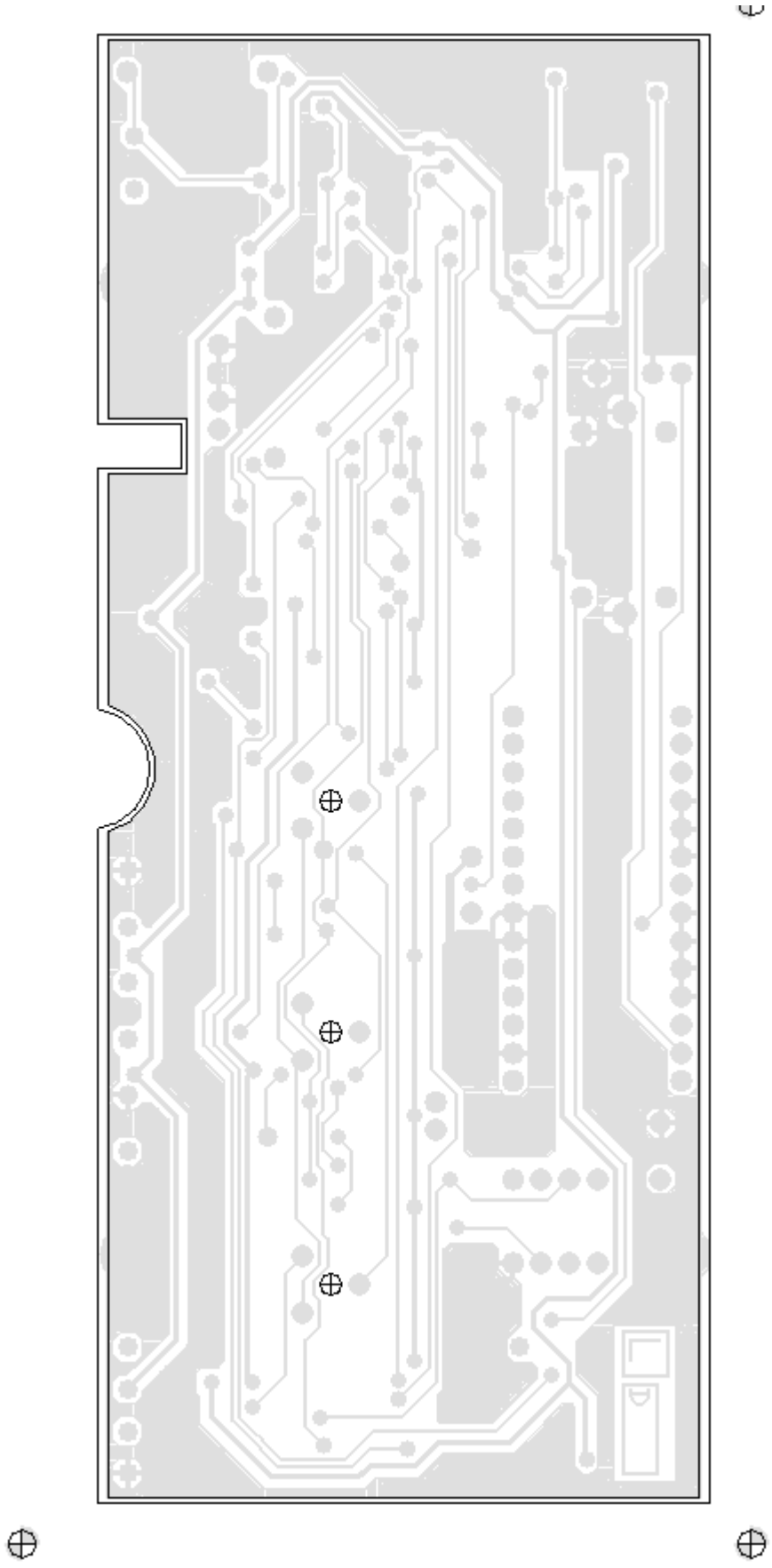

Figure 11 T800-30-0000/0002 PCB Layout - Bottom Side (IPN 220-01226-02)

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