2

ANT-20, ANT-20E
Advanced Network Tester

STM-1 Mappings

BN 3035/90.01 to 90.06

Drop & Insert

BN 3035/90.20
in combination with
STM-1 Mappings

Software Version 7.20

Operating Manual

BN 3035/98.25

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Please direct all enquiries to your local Wavetek Wandel Goltermann sales company. The addresses are given at the end of this handbook.

Wavetek Wandel Goltermann
Eningen GmbH & Co.
Mühleweg 5, 72800 Eningen u. A.

Author: MDD/TD
Translator: John Nutley

Order no.: BN 3035/98.25
Edition: 13/00.07 (V 7.20)

Previous edition:
12/00.04 (V 7.1)

Printed in Germany

Contents

Specifications

1 STM-1 Mapping S-1

1.1 General information S-1
1.2 Tributary channel numbering S-2
1.3 Scrambling/Descrambling S-2
1.4 Overhead generation S-3
1.4.1 Section Overhead (SOH) S-3
1.4.2 STM-1 error insertion (anomalies) S-4
1.4.3 STM-1 alarm generation (defects) S-5
1.4.4 Pointer action generation S-6
1.4.5 STM-1 error measurements (anomalies) S-9
1.4.6 STM-1 alarm detection (defects) S-10
1.4.7 Measurement of AU and TU pointer actions S-11
1.4.8 VC-4 Path Overhead (POH), High Order S-12
1.4.9 VC-3 Path Overhead (POH), High Order S-13
1.4.10 Evaluation of Section Overhead (SOH) and VC-4/VC-3 Path Overhead (POH) S-14
1.5 C-12 mapping (2 Mbit/s in STM-1, AU-3/AU-4) S-15
1.5.1 VC-12 Path Overhead contents S-16
1.5.2 VC-12 error insertion (anomalies) S-16
1.5.3 VC-12 alarm generation (defects) S-17
1.5.4 VC-12 error measurements (anomalies) S-17
1.5.5 VC-12 alarm detection (defects) S-18
1.5.6 VC-12 Path Overhead evaluation S-18
1.6 C-3 mapping (34/45 Mbit/s in STM-1, AU-3/AU-4) S-19
1.6.1 VC-3 Path Overhead contents (Low Order) S-20
1.6.2 VC-3 error insertion (anomalies) S-20
1.6.3 VC-3 alarm generation (defects) S-21
1.6.4 VC-3 error measurement (anomalies) S-21
1.6.5 VC-3 alarm detection (defects) S-22
1.6.6 VC-3 Path Overhead evaluation S-22
1.7 C-4 mapping (140 Mbit/s in STM-1/STS-3c) S-23

1.8 C-11 mapping (1.5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12) S-24
1.8.1 VC-11 Path Overhead contents S-26
1.8.2 VC-11 error insertion (anomalies) S-26
1.8.3 VC-11 alarm generation (defects) S-27
1.8.4 VC-11 error measurements (anomalies) S-27
1.8.5 VC-11 alarm detection (defects) S-28
1.8.6 VC-11 Path Overhead evaluation S-28
1.9 C-2 mapping (6.3 Mbit/s in STM-1, AU-3/AU-4, TU-2) S-29
1.9.1 VC-2 Path Overhead contents S-30
1.9.2 VC-2 error insertion (anomalies) S-30
1.9.3 VC-2 alarm generation (defects) S-31
1.9.4 VC-2 error measurements (anomalies) S-31
1.9.5 VC-2 alarm detection (defects) S-32
1.9.6 VC-2 Path Overhead evaluation S-32
1.10 Filler channel contents S-32

2 Drop & Insert / Through Mode S-33

2.1 Functions S-33
2.1.1 Clock generator S-34
2.1.2 Overhead generator S-35
2.1.3 Anomaly insertion S-35
2.1.4 Defect generation S-35
2.1.5 Pointer generation S-35
2.1.6 Measurements S-35
2.2 Signal outputs S-36
2.2.1 AUXILIARY signal output [11], electrical S-36
2.2.2 LINE/AUXILIARY signal output [13], electrical S-36
2.3 Signal inputs S-37
2.3.1 AUXILIARY signal input [10], electrical S-37
2.3.2 LINE/AUXILIARY signal input [12], electrical S-38

Specifications

These specifications apply to the options:

STM-1 Mapping

for ETSI tributaries

C-12 (2 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.01
C-3 (34 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.02
C-4 (140 Mbit/s in STM-1) . . . . . .BN 3035/90.03
C-2 (6 Mbit/s, unframed, in STM-1, AU-3/AU-4). . . . . .BN 3035/90.06

for ANSI tributaries

C-11 (1,5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12) . . . . . .BN 3035/90.04
C-3 (45 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.05

Drop & Insert . . . . . .BN 3035/90.20

1 STM-1 Mapping

1.1 General information

Mapping/Demapping

The PDH tributaries are mapped into a STM-1 signal via the AU-4 or the AU-3 layer.

Container contents for all mapping options:

- Framed or unframed PDH test signal in one selected container
  (6 Mbit/s, unframed only)
- PDH multiplex signal in one selected container
  (together with Mux/Demux Chain 64k/140M or M13 option)
- Filling one selected container with a test pattern without justification bits
  (Bulk Signal to O.181)

Drop & Insert

An additional Drop & Insert Option (BN 3035/90.20) for dropping or inserting tributary signals (via sockets) is available in conjunction with the mapping options.

1.2 Tributary channel numbering

TU-3	TU-2	TU-12	TU-11	TS #
100	110	111	111	1
		112	112	22
		113	113	43
			114	64
	120	121	121	4
		122	122	25
		123	123	46
			124	67
	130	131	131	7
		132	132	28
		133	133	49
			134	70
	140	141	141	10
		142	142	31
		143	143	52
			144	73
	150	151	151	13
		152	152	34
		153	153	55
			154	76
	160	161	161	16
		162	162	37
		163	163	58
			164	79
	170	171	171	19
		172	172	40
		173	173	61
			174	82

TU-3	TU-2	TU-12	TU-11	TS #
200	210	211	211	2
		212	212	23
		213	213	44
			214	65
	220	221	221	5
		222	222	26
		223	223	47
			224	68
	230	231	231	8
		232	232	29
		233	233	50
			234	71
	240	241	241	11
		242	242	32
		243	243	53
			244	74
	250	251	251	14
		252	252	35
		253	253	56
			254	77
	260	261	261	17
		262	262	38
		263	263	59
			264	80
	270	271	271	20
		272	272	41
		273	273	62
			274	83

TU-3	TU-2	TU-12	TU-11	TS #
300	310	311	311	3
		312	312	24
		313	313	45
			314	66
	320	321	321	6
		322	322	27
		323	323	48
			324	69
	330	331	331	9
		332	332	30
		333	333	51
			334	72
	340	341	341	12
		342	342	33
		343	343	54
			344	75
	350	351	351	15
		352	352	36
		353	353	57
			354	78
	360	361	361	18
		362	362	39
		363	363	60
			364	81
	370	371	371	21
		372	372	42
		373	373	63
			374	84

Table S-1 Channel numbers to G.707 (relationship between TU and time slot TS #)

1.3 Scrambling/Descrambling

The STS-N signal is scrambled/descrambled as described in ITU-T G.707.

1.4 Overhead generation

1.4.1 Section Overhead (SOH)

Standard Overhead, STM-1 (hex)

SOH										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	
1	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	J0 01	— AA	— AA	
2	B1 XX	— 00	— 00	E1 00	— 00	— 00	F1 00	— 00	— 00	
3	D1 00	— 00	— 00	D2 00	— 00	— 00	D3 00	— 00	— 00	
4a	H1 68	Y 9B	Y 9B	H2 00	— FF	— FF	H3 00	H3 00	H3 00	for AU-4
4b	H1 68	H1 68	H1 68	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	for AU-3
5	B2 XX	B2 XX	B2 XX	K1 00	— 00	— 00	K2 00	— 00	— 00	
6	D4 00	— 00	— 00	D5 00	— 00	— 00	D6 00	— 00	— 00	
7	D7 00	— 00	— 00	D8 00	— 00	— 00	D9 00	— 00	— 00	
8	D10 00	— 00	— 00	D11 00	— 00	— 00	D12 00	— 00	— 00	
9	S1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	E2 00	— 00	— 00	

Table S-2 SOH contents

XX: Inserted by parity formation (B1, B2)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown), H3 depends on whether or not a pointer action takes place.

SOH byte contents

- Static bytes: all except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: all except B1, B2, H1, H2, H3
- Trace Identifier (Length = 16 frames with CRC7 formation): J0
- Dynamic bytes filled using PRBS 11: E1, F1, E2
- Dynamic byte groups filled using PRBS 11: D1 to D3, D4 to D12
- Dynamic bytes filled via DCC/ECC interface (V.11): E1, F1, E2
- Dynamic byte groups filled via DCC/ECC interface (V.11): D1 to D3, D4 to D12, K1 to K2

1.4.2 STM-1 error insertion (anomalies)

Error insertion (anomalies) . . . . . B1, B2, B3 parity errors, FAS word errors, MS-REI, HP-REI, bit errors in test pattern (TSE), code errors (single errors only)

Trigger types . . . . . Single or Rate

When Rate triggering is selected a bit error rate is inserted.

Anomaly	**Single**	**Rate[1]**	**Burst m, n (frames)**
FAS	yes	2E-3 to 1E-10	m = 1 to 196000
B1	yes	2E-4 to 1E-10	m = 1 to 196000
B2	yes	2E-3 to 1E-10	m = 1 to 196000
MS-REI	yes	2E-3 to 1E-10	m = 1 to 196000
B3[2]	yes	2E-4 to 1E-10	m = 1 to 196000
HP-REI	yes	2E-4 to 1E-10	m = 1 to 196000
TSE	yes	1E-2 to 1E-8	-
CODE	yes	-	-

1 Mantissa: 1 to 9 (only 1 for TSE), exponent: -1 to -10 (whole numbers)
2 Static error insertion, can be edited using an 8-bit mask (x = don't care, 1 = insert error)

Table S-3 Available anomalies (STM-1) and trigger modes

The insertion of **errors** (anomalies) **and alarms** (defects) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.3 STM-1 alarm generation (defects)

Defect	**Test sensor function**	**Test sensor thresholds**	
	On/Off	M in N	|----t1----| |------t2------|
LOS[1]	yes	M = 800 bis 7200 N = 1600 bis 8000	t1 = 0.1 bis 60.0 s t2 = 0.2 bis 600 s
LOF	yes	M = 1 to N - 1 N = 1 to 8000[2]	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RS-TIM	yes	-	-
MS-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
MS-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-UNEQ	yes	M = 1N to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-PLM	yes	M = 1N to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-TIM	yes	-	-

1 Only in conjunction with an optical interface
2 Included in mainframe (no option required)

Table S-4 Available defects (STM-1)

The insertion of **alarms** (defects) **and errors** (anomalies) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.4 Pointer action generation

Stimulation

Pointer sequences

On all pointer levels to ITU-T G.783

T1, T4: 0.25 ms to 600 s . . . . . (2 to 4800000 frames)

T2, T3: 0.25 ms to 10 s . . . . . (2 to 80000 frames)

T5: 0 ms to 600 s. . . . . (0 to 4800000 frames)

n: 1 to 2000

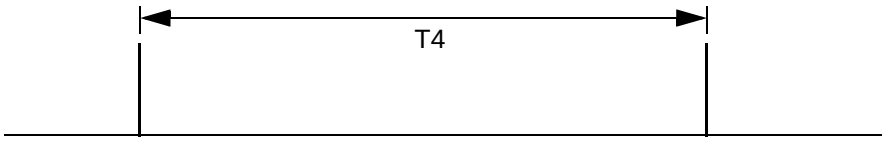

Fig. S-1 Perodic (single/multiple) pointers with identical polarity

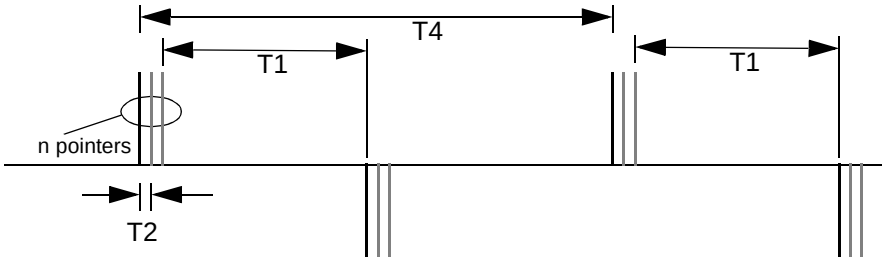

Fig. S-2 Periodic (single/multiple) pointers with different polarity

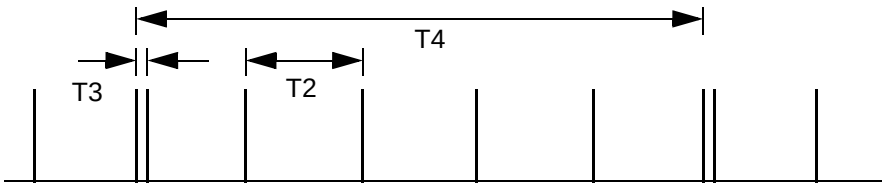

Fig. S-3 Periodic pointers with one double pointer

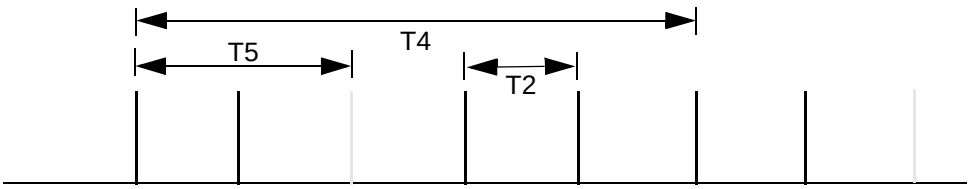

Fig. S-4 Periodic pointers with one missing pointer

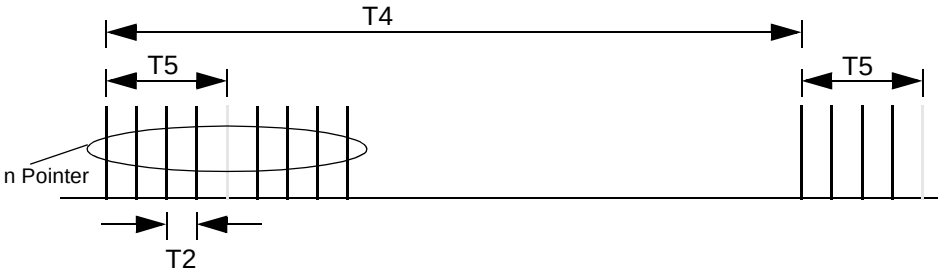

Fig. S-5 Pointer burst with missing pointers

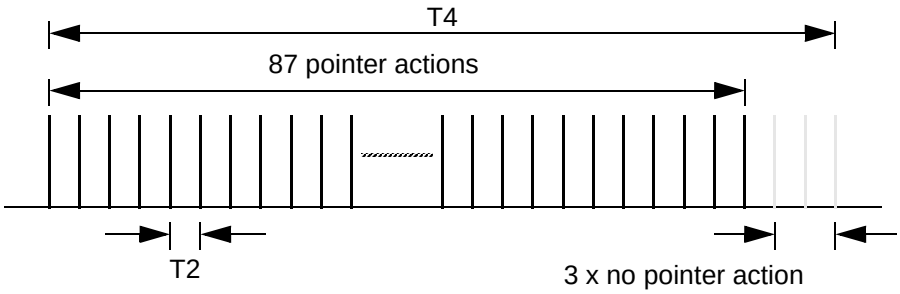

Fig. S-6 ”87-3” sequence

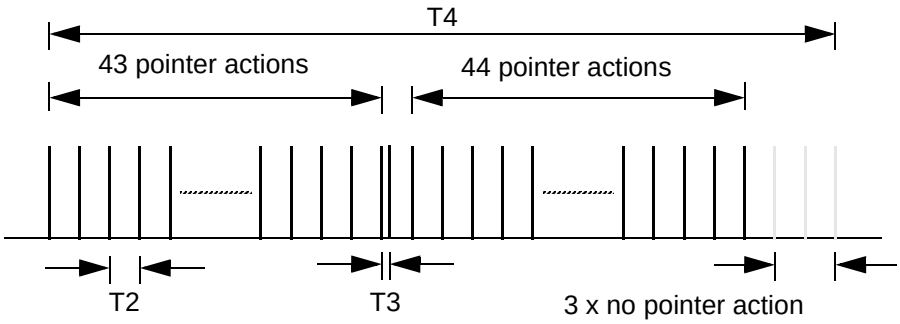

Fig. S-7 ”43-44” sequence with double pointer

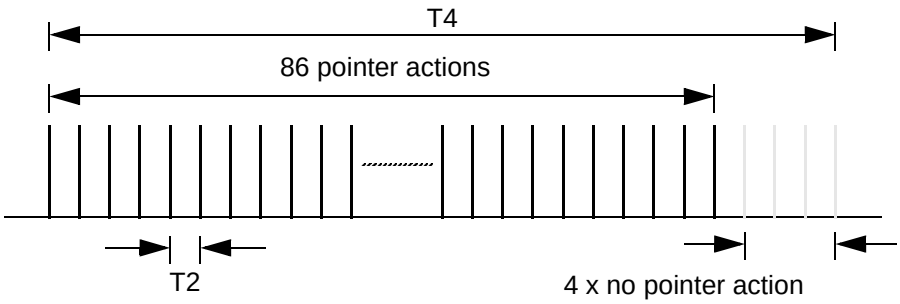

Fig. S-8 ”86-4” sequence with missing pointer

Pointer jumps

Pointer jump from pointer value A to pointer value B (also setting a new pointer).

Pointer jumps are executed with NDF.
Pointer range A + B:

AU-4/AU-3 pointer	0 to 782
TU-3 pointer	0 to 764
TU-2 pointer	0 to 427
TU-12 pointer	0 to 139
TU-11 pointer	0 to 103

1.4.5 STM-1 error measurements (anomalies)

Evaluation

All errors (anomalies) are counted simultaneously and stored.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

of anomalies via LEDs:

CURRENT LED (red) is on when the anomaly is present

HISTORY LED (yellow) is on if the anomaly has occurred at least once during the current measurement interval.

Display of errors as count or ratio values (equivalent bit error ratio): When calculating the ratio value, correction formulae are used for the anomalies B1, B2, B3 and BIP-2 as well as MS-REI, HP-REI and LP-REI. These take into account that a multiple error in the same bit can lead to clearance of the error.

Anomaly	**LED**
OOF -155	LOF/OOF
FAS-155	-
B1	B1/B2
B2	B1/B2
MS-REI	-
B3	B3
HP-REI	-
CRC-4	FAS/CRC
E-Bit	-
TSE	TSE
CODE	-

Table S-5 LED display of possible anomalies (STM-1)

1.4.6 STM-1 alarm detection (defects)

Evaluation

All alarms (defects) which occur are evaluated simultaneously where possible and stored. Storage takes place only within a started measurement interval.

Time resolution of defects . . . . . 100 ms

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present

HISTORY LED (yellow) is on if the defect has occurred at least once during the current measurement interval.

Defect	**LED**
LOS	LOS
LOF-155	LOF/OOF
RS-TIM	-
MS-AIS	MS-AIS
MS-RDI	MS-RDI
AU-LOP	AU-LOP
AU-AIS	AU-AIS
HP-UNEQ	HP-UNEQ
HP-PLM	HP-PLM
HP-RDI	HP-RDI
HP-TIM	-
LSS	LSS

Table S-6 LED display of possible defects (STM-1)

1.4.7 Measurement of AU and TU pointer actions

Evaluation

All pointers in the selected path are shown as absolute values and the direction and number of pointer movements is detected and counted.

NDF (New Data Flag) is recorded and counted.

Display

of:

- Number of pointer operationsseparated for AU and TU pointer:
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address
- Number of NDF events
- Corresponding clock deviation
- AU-NDF and TU-NDF can be indicated by the LED display (front panel)
  (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP”
  – the “TU-LOP/LOP-V” LED indicates “TU-NDF” in addition to “TU-LOP”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are displayed as a histogram with selectable time resolution in seconds, minutes, hours or days.

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are printed out as a table with 1 second time resolution.

1.4.8 VC-4 Path Overhead (POH), High Order

Standard overhead

POH byte	Option 3035/90.01, Option 3035/90.04, Option 3035/90.06	Option 3035/90.02 and Option 3035/90.05	Option 3035/90.03
J1 (ASCII)	“WG HP-TRACE”		“VC-4 MAPPING” “VC-4 BULK”
B3 (hex)	Inserted by parity formation		
C2 (hex)	“02”	“04”	“12” for MAPPING “FE” for BULK
G1 (hex)	“00”		
F2 (hex)	“00”		
H4 (hex)	“FC”, ”FD”, ”FE”, ”FF” sequence across 4 frames	“FF”	
	48-byte-sequence as G.709		
F3 (hex)	“00”		
K3 (hex)	“00”		
N1 (hex)	“00”		

Table S-7 POH contents

VC-4 POH byte contents

- Static bytes: all except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using PRBS 11: F2
- Dynamic bytes filled via DCC/ECC interface (V.11): F2, K3, N1
- H4 sequence, switchable, 4/48 byte

1.4.9 VC-3 Path Overhead (POH), High Order

Standard overhead

POH byte	Option 3035/90.01, Option 3035/90.04 and Option 3035/90.06		Option 3035/90.02 and Option 3035/90.05	
	Measured channels	**Fill channels**	**Measured channels**	**Fill channels**
J1 (ASCII)	“WG HP-TRACE”	“WG IDLE”	“VC-3 Mapping” “VC-3 Bulk”	“WG IDLE”
B3 (hex)	Inserted by parity formation			
C2 (hex)	“02”	“02”	“04” for mapping “FE” for bulk	“04”
G1 (hex)	“00”			
F2 (hex)	“00”			
H4 (hex)	“FC”, “FD”, “FE”, “FF” sequence across 4 frames		“FF”	
	48-byte-sequence asG.709			
F3 (hex)	“00”			
K3 (hex)	“00”			
N1 (hex)	“00”			

Table S-8 POH contents

VC-3 POH byte contents

- Static bytes: all except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using a pseudo-random sequence: F2
- Dynamic bytes filled by DCC/ECC interface (V.11): F2, K3, N1
- H4 sequence, switchable, 4/48 byte

1.4.10 Evaluation of Section Overhead (SOH) and VC-4/VC-3 Path Overhead (POH)

Display

of complete SOH and POH . . . . . hexadecimal
of Trace Identifier J0, J1 . . . . . ASCII, plain text

Evaluation

Bit error measurement

using PRBS 11 (bytes). E1, F1, E2, F2
using PRBS 11 (byte groups) . . . . . D1 to D3, D4 to D12

Output

as bytes via DCC/ECC interface (V.11) E1, F1, E2, F2, K3, N1
as byte groups via DCC/ECC interface (V.11). . . . . D1 to D3, D4 to D12, K1 to K2

1.5 C-12 mapping (2 Mbit/s in STM-1, AU-3/AU-4)

Option: BN 3035/90.01

Mapping structure: AU-4

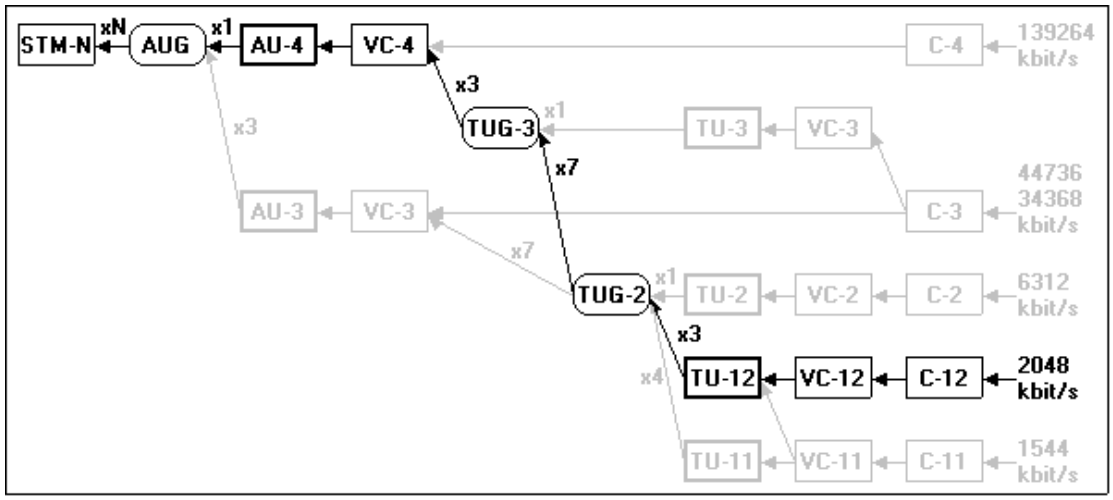

Fig. S-9 Mapping structure: 2 Mbit/s → C-12 → AU-4 → STM-1

Mapping structure: AU-3

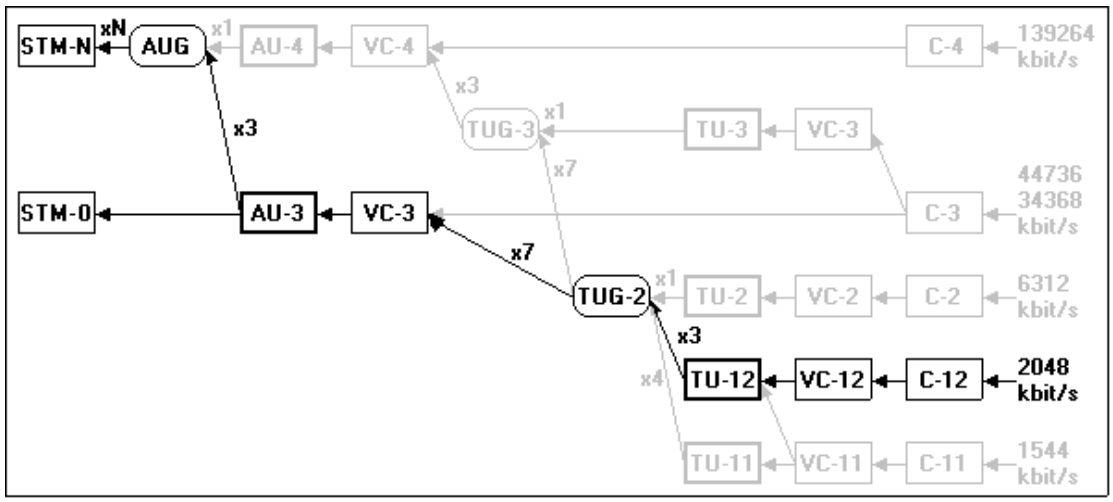

Fig. S-10 Mapping structure: 2 Mbit/s → C-12 → AU-3 → STM-1
Mapping structure: 2 Mbit/s → C-12 → AU-3 → STM-0; option 3035/98.13 required

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating)

1.5.1 VC-12 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “110” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-9 VC-12 POH (Standard Overhead) contents

Measurement channel byte contents (VC-12)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier (Length = 16 frames with CRC7 formation): J2
- Dynamic bytes filled by DCC/ECC interface (V.11): N2

Filler channel byte contents (VC-12)

Fixed, non-editable as in (see Tab. S-9).

1.5.2 VC-12 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-4:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-10 Additional available anomalies (VC-12)

Error insertion refers to the selected measurement channel.

1.5.3 VC-12 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-5:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-11 Addition available defects (VC-12)

Alarm generation refers to the selected measurement channel.

1.5.4 VC-12 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-9:

Anomaly	**LED**
LP-BIP	LP-BIP
LP-REI	-

Table S-12 LED display of additional anomalies (VC-12)

Evaluation and display refer to the selected measurement channel.

1.5.5 VC-12 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-10:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-13 LED display of additional alarms (VC-12)

Evaluation and display refer to the selected measurement channel.

1.5.6 VC-12 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.6 C-3 mapping (34/45 Mbit/s in STM-1, AU-3/AU-4)

Option: BN 3035/90.02 for 34 Mbit/s
Option: BN 3035/90.05 for 45 Mbit/s

Mapping structure: AU-4

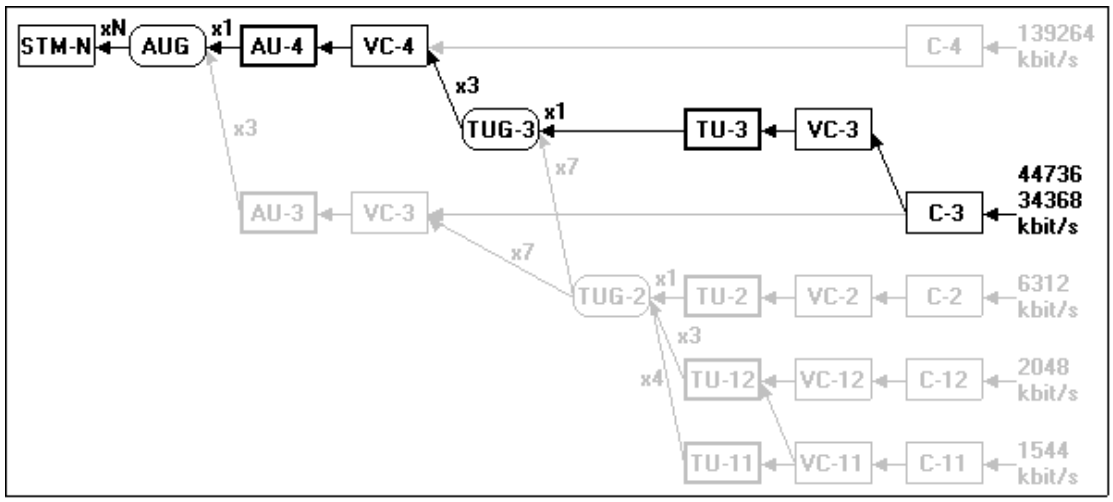

Fig. S-11 Mapping structure: 34/45 Mbit/s → C-3 → AU-4 → STM-1

Mapping structure: AU-3

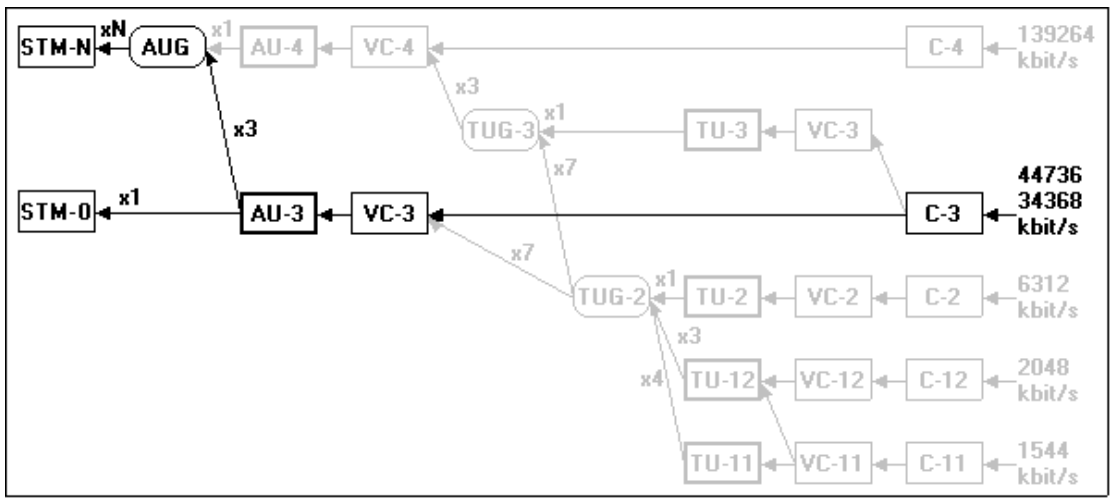

Fig. S-12 Mapping structure: 34/45 Mbit/s → C-3 → AU-3 → STM-1
Mapping structure: 34/45 Mbit/s → C-3 → AU-3 → STM-0;
option 3035/90.12 required

1.6.1 VC-3 Path Overhead contents (Low Order)

POH byte	Measurement channel	Filler channels
J1 (ASCII)	“WG TRACE”	“WG IDLE”
B3 (hex)	Inserted by parity formation	
C2 (hex)	“04” for mapping signal “FE” for bulk signal	“04”
G1 (hex)	“00”	
F2 (hex)	“00”	
H4 (hex)	”FF”	
Z3 (hex)	“00”	
K3 (hex)	“00”	
N1 (hex)	“00”	

Table S-14 VC-3 POH (Standard Overhead) contents

Test channel byte contents (VC-3)

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using pseudo-random bit sequence: F2
- Dynamic bytes via V.11 interface (V.11): F2, K3, N1

Filler channel byte contents

Fixed, non-editable (see Tab. S-14).

1.6.2 VC-3 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-4:

Anomaly	Single	Rate
LP-B3[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 8-bit mask (x = don’t care, 1 = insert error)

Table S-15 Additional available anomalies (VC-3)

Error insertion refers to the selected measurement channel.

1.6.3 VC-3 alarm generation (defects)

The following defects can be inserted in addition to the defects specified in Sec. 1.4.3, Page S-5:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-

Table S-16 Additional available defects (VC-3)

Alarm generation refers to the selected measurement channel.

1.6.4 VC-3 error measurement (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-9:

Anomaly	**LED**
LP-B3	LP-BIP
LP-REI	-

Table S-17 LED display of additional anomalies (VC-3)

Evaluation and display refer to the selected measurement channel.

1.6.5 VC-3 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-10:

Defect	LED
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-

Table S-18 LED display of additional defects (VC-3)

Evaluation and display refer to the selected measurement channel.

1.6.6 VC-3 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J1

Output

- Bit error measurement using PRBS 11: F2 (byte)
- Byte output via DCC/ECC interface (V.11): F2, K3, N1

1.7 C-4 mapping (140 Mbit/s in STM-1/STS-3c)

Option BN 3035/90.03

STS-3c see also
Operating Manual “STS-1 mappings”, section “STS-3c SPE mappings”.

Mapping structure

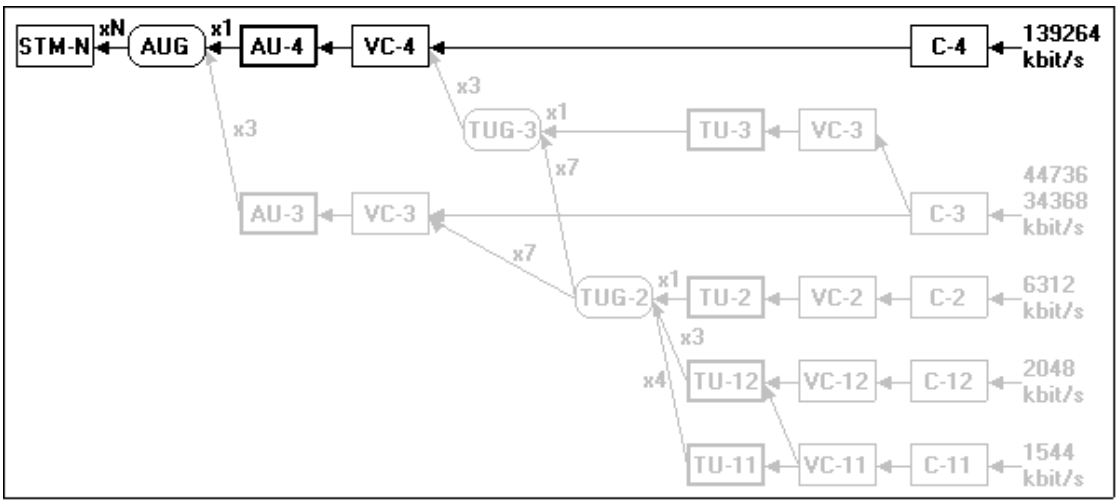

Fig. S-13 Mapping structure: 140 Mbit/s → AU-4 → STM-1

The mapping characteristics are described in Sec. 1.4, Page S-3.

1.8 C-11 mapping (1.5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12)

Option BN 3035/90.04

Mapping structure: AU-3, TU-11

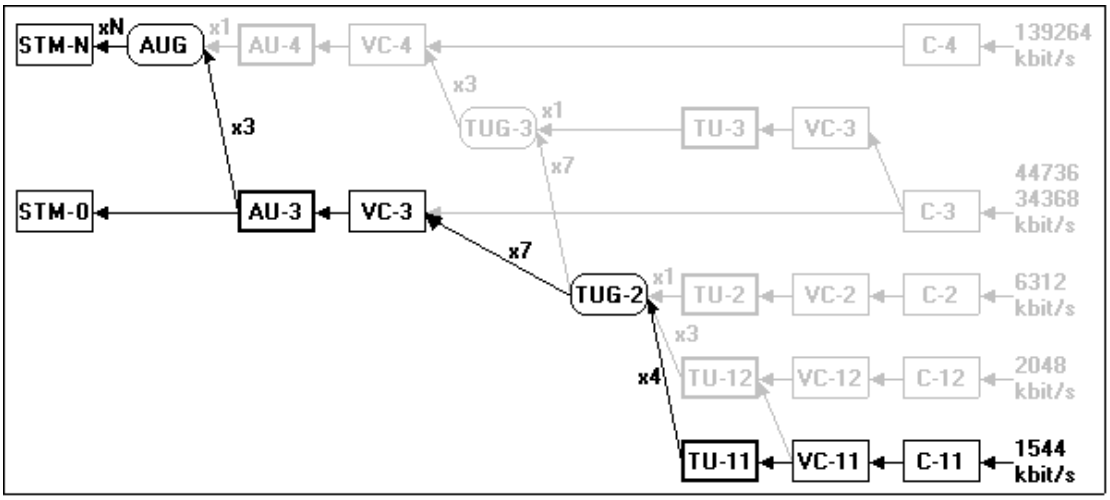

Fig. S-14 Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-3 → STM-1
Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-3 → STM-0;
option 3035/90.10 required

Mapping structure: AU-3, TU-12

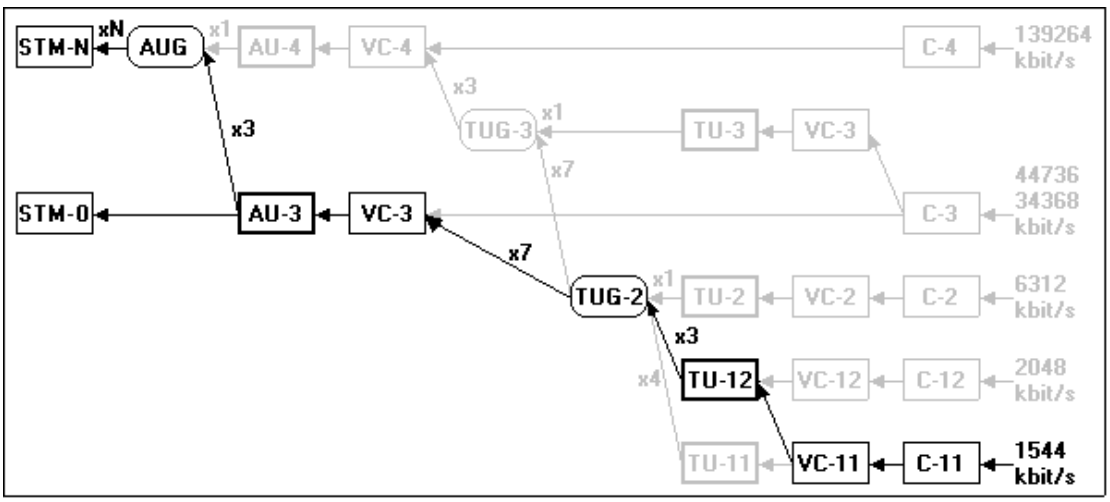

Fig. S-15 Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-3 → STM-1
Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-3 → STM-0;
option 3035/90.10 required

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating); only TU-11

Mapping structure: AU-4, TU-11

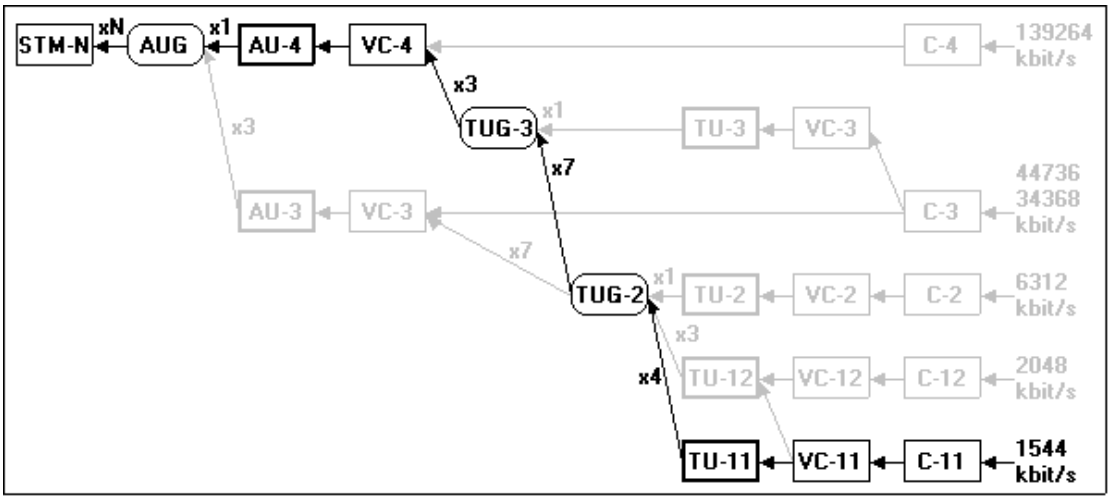

Fig. S-16 Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-4 → STM-1

Mapping structure: AU-4, TU-12

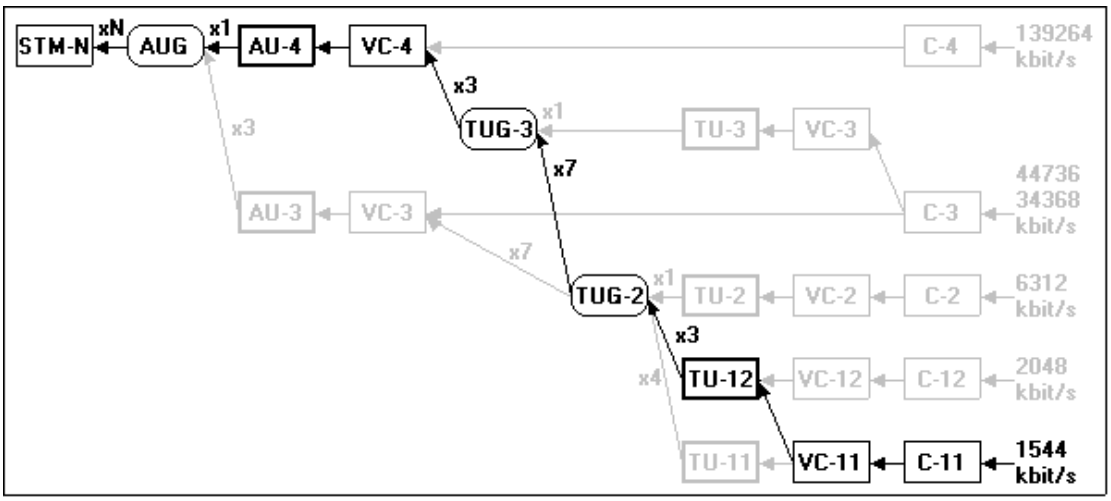

Fig. S-17 Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-4 → STM-1

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating)

1.8.1 VC-11 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “110” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-19 VC-11 POH (Standard Overhead) contents

Measurement channel byte contents (VC-11)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier (Length = 16 frames with CRC7 formation): J2
- Dynamic bytes via V.11 interface (V.11): N2

Filler channel byte contents (VC-11)

Fixed, non-editable (see Tab. S-19).

1.8.2 VC-11 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-4:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-20 Additional available anomalies (VC-11)

Error insertion refers to the selected measurement channel.

1.8.3 VC-11 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-5:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-21 Additional available defects(VC-11)

Alarm generation refers to the selected measurement channel.

1.8.4 VC-11 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-9:

Anomaly	**LED**
LP-BIP	LP-BIP
LP-REI	-

Table S-22 LED display of additional anomalies (VC-11)

Evaluation and display refer to the selected measurement channel.

1.8.5 VC-11 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-10:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-23 LED display of additional defects (VC-11)

Evaluation and display refer to the selected measurement channel.

1.8.6 VC-11 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.9 C-2 mapping (6.3 Mbit/s in STM-1, AU-3/AU-4, TU-2)

Option BN 3035/90.06

Mapping structure: AU-3, TU-2

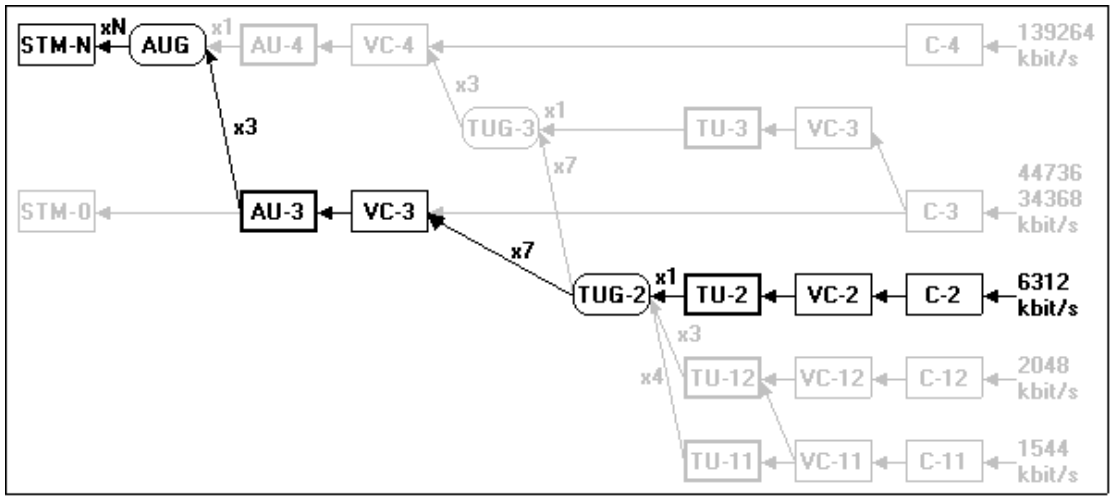

Fig. S-18 Mapping structure: 6.3 Mbit/s → C-2 → TU-2 → AU-3 → STM-1

Mapping method

The following mode is available:

- Asynchronous mode

Mapping structure: AU-4, TU-2

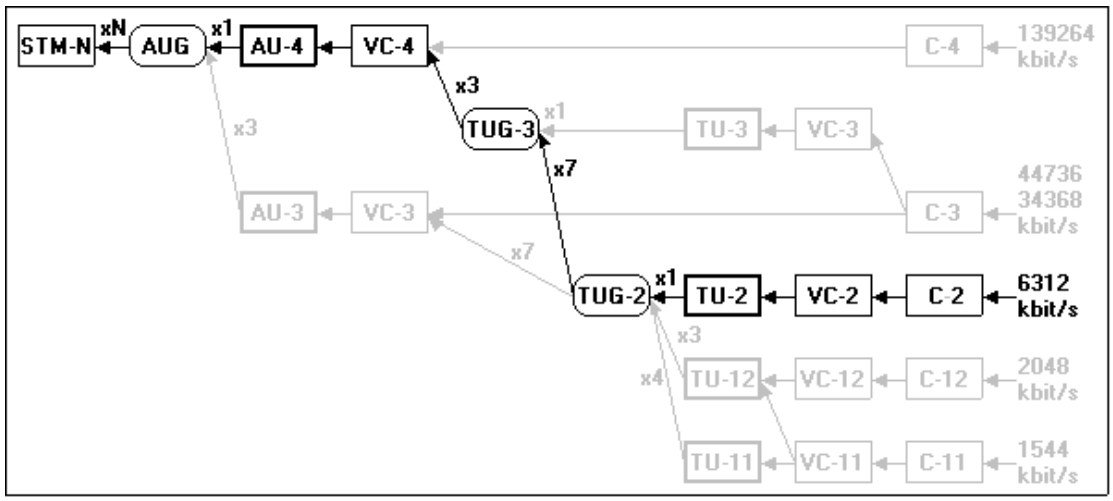

Fig. S-19 Mapping structure: 6.3 Mbit/s → C-2 → TU-2 → AU-4 → STM-1

Mapping method

The following mode is available:

- Asynchronous mode

1.9.1 VC-2 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “110” for bulk signal	“010” for asynchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-24 VC-2 POH (Standard Overhead) contents

Measurement channel byte contents (VC-2)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier: J2 (Length = 16 frames with CRC7 formation)
- Dynamic bytes via V.11 interface (V.11): N2

Filler channel byte contents (VC-2)

Fixed, non-editable (see Tab. S-24).

1.9.2 VC-2 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-4:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-25 Additional available anomalies (VC-2)

Error insertion refers to the selected measurement channel.

1.9.3 VC-2 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-5:

Defect	Test sensor function	Sensor thresholds	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-26 Additional available defects (VC-2)

Alarm generation refers to the selected measurement channel.

1.9.4 VC-2 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-9:

Anomaly	LED
LP-BIP	LP-BIP
LP-REI	-

Table S-27 LED display of additional anomalies (VC-2)

Evaluation and display refer to the selected measurement channel.

1.9.5 VC-2 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-10:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-28 LED display of additional defects (VC-2)

Evaluation and display refer to the selected measurement channel.

1.9.6 VC-2 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.10 Filler channel contents

Mapping structure as for measurement channel, test pattern PRBS11.

2 Drop & Insert / Through Mode

Option: BN 3035/90.20

2.1 Functions

This Option provides the following functions for all mapping options fitted to the ANT-20.

Drop & Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

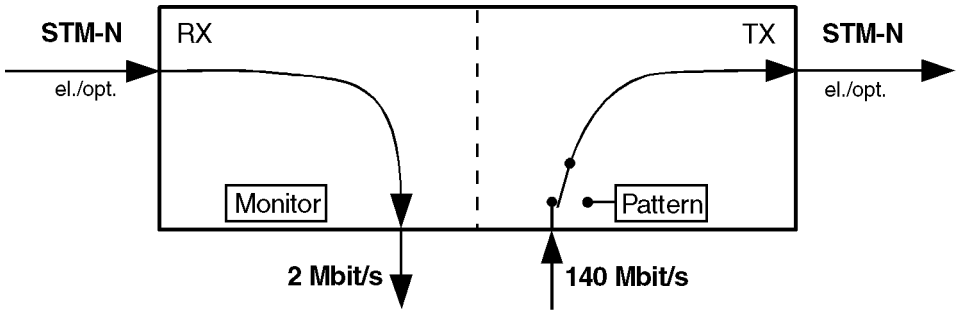

Fig. S-20 Drop & Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 2.2.1, Page S-36 and Sec. 2.3.1, Page S-37).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20 and re-transmitted by the generator. One tributary signal can be output (dropped).

The ANT-20 can also operate in Through Mode as a signal monitor without affecting the signal content.

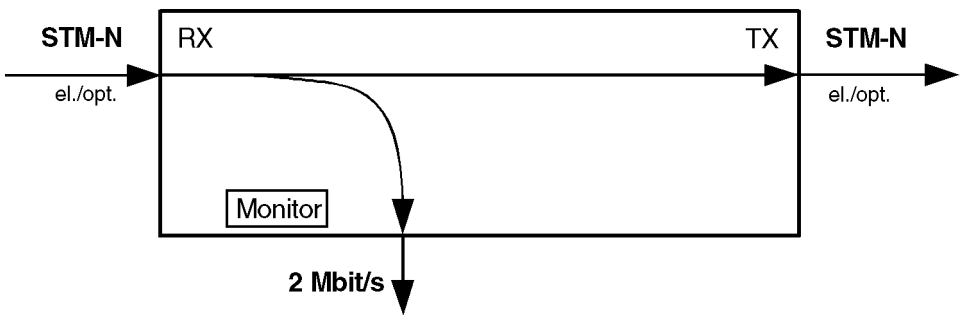

Fig. S-21 Through Mode: Generator and receiver coupled

In conjunction with the Options “PDH MUX/DEMUX” and “M13 MUX/DEMUX”, BN 3035/90.30 to BN 3035/90.32, the ANT-20 provides access to the tributary channels within the MUX/ DEMUX chain (except DS2). This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

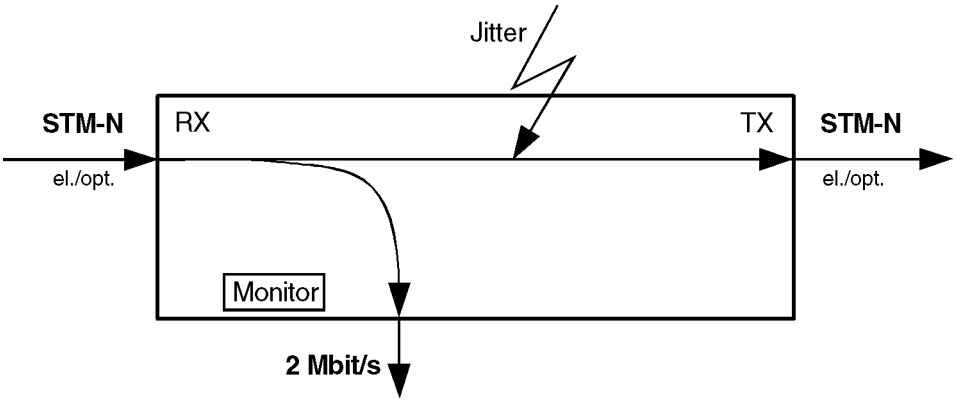

Fig. S-22 Through Mode: Adding jitter to the looped-through signal

In Through Mode, anomalies can be inserted in the SOH or the SOH bytes can be manipulated.

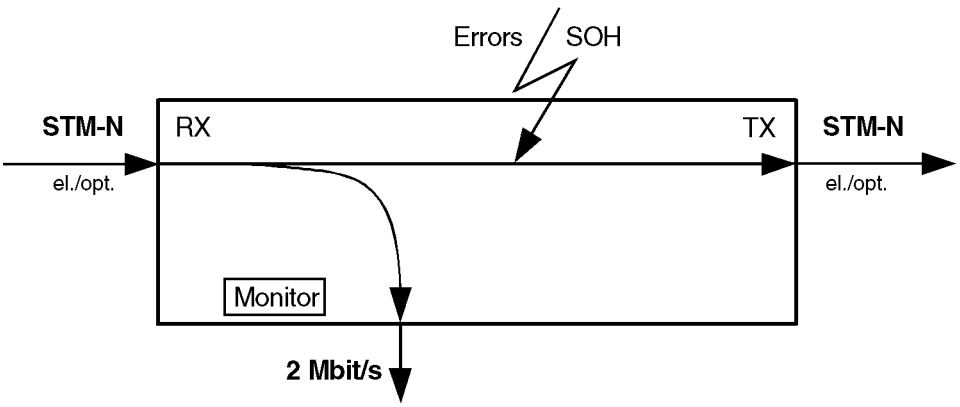

Fig. S-23 Through Mode: Inserting errors in the SOH

2.1.1 Clock generator

Drop & Insert

As specified in the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock.
No offset is possible in this operating mode (see also “Specifications” of the mainframe instrument).

2.1.2 Overhead generator

Drop & Insert

As specified in Sec. 1.4.1, Page S-3.

Through Mode

The “From Rx” function can be set in addition to the functions described in Sec. 1.4.1, Page S-3 for all bytes except bytes B1, B2 and M1.

2.1.3 Anomaly insertion

Drop & Insert

As specified in Sec. 1.4.2, Page S-4.

Through Mode

Anomaly insertion in bytes B1, B2 and MS-REI.
Insertion limits are specified in Sec. 1.4.2, Page S-4.

2.1.4 Defect generation

Drop & Insert

As specified in Sec. 1.4.3, Page S-5.

Through Mode

No direct defect generation is possible.

Alarms (defects) in the SOH can be generated by manipulating the SOH bytes.

2.1.5 Pointer generation

Drop & Insert

As specified in Sec. 1.4.4, Page S-6.

Through Mode

The receive-side pointer is re-transmitted unchanged.

2.1.6 Measurements

There are no restrictions on measurements.
See Sec. 1.4.5, Page S-9 through Sec. 1.4.10, Page S-14.

2.2 Signal outputs

2.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
DS2	6.312	B8ZS	± 2.0 V
E1	2.048	HDB3	± 2.37 V
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-29 Specifications of the AUXILIARY signal output [11], electrical

2.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-30 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used both as “LINE” and as “AUXILIARY” output.

2.3 Signal inputs

2.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
DS2	6.312	B8ZS	2.0 V ±10 %
E1	2.048	HDB3	2.37 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-31 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

2.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-32 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used both as “LINE” and as “AUXILIARY” input.