ANT-20SE
Advanced Network Tester

Specifications

Software Version 7.20

Please direct all enquiries to your local Wavetek Wandel Goltermann sales company.

Wavetek Wandel Goltermann
Eningen GmbH & Co.
Mühleweg 5, 72800 Eningen u. A.

Author: MDD/TD
Translator: John Nutley

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Specifications

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Specifications Mainframe, SDH and SONET Version

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Specifications Mainframe, SDH and SONET Version

The numbers in square brackets […] correspond to the numbers printed on the instrument.

Calibrated specifications for the SDH Version ANT-20SE 3060/01 are marked ***.
Calibrated specifications for the SONET Version ANT-20SE 3060/02 are marked **.

1 Generator section

1.1 Digital signal outputs

1.1.1 LINE signal output [15], electrical

Connector . . . . . unbalanced (coaxial)

Socket . . . . . UNI 9 (Versacon®)

Output impedance . . . . . 75 Ω

Max. applied peak voltage . . . . . ± 5 V

Interface[3]	Bit rate (Mbit/s)	Line code	Output voltage	Output voltage tolerance	Reflexion coefficient
STS-3 STM-1	155.520 *** **	CMI	± 0.5 V	± 0.05 V	≥ 15 dB 100 kHz to 240 MHz
STM-0	51.840 **	HDB3	± 1.0 V	± 0.1 V	≥ 18 dB 50 kHz to 52 MHz
STS-1		B3ZS	DS High: ± 0.909 V		
DS3	44.736[2]	B3ZS	DSX3: High + Sim 450 feet 728A cable[4] DS Low: High -13.8 dB[4]		
DS2	6.312[2]	B8ZS	± 2 V[4]	± 0.2 V	
DS1	1.544[2]	B8ZS, AMI	± 2.37 V	± 0.237 V	
E4	139.264[1]	CMI	± 0.5 V	± 0.05 V	≥ 15 dB 100 kHz to 240 MHz
E3	34.368[1] ***	HDB3	± 1.0 V	± 0.1 V	≥ 18 dB 50 kHz to 52 MHz
E2	8.448[1]	HDB3	± 2.37 V	± 0.2 V	
E1	2.048[1]	HDB3			

1 3035/02 requires option 3035/90.33
2 3035/01 requires option 3035/90.34
3 depends on ANT-20SE versions and options
4 from H series onwards

Table S-1 LINE output [15] signal specifications, electrical

1.1.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket: 3035/01 . . . . . Lemo SA
Socket: 3035/02 . . . . . Bantam

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. applied peak voltage . . . . . ± 5 V

Bit rate (Mbit/s)	Line code	Output voltage	Output voltage tolerance	Reflexion coefficient
2.048[1] ***	HDB3	± 3.0 V	± 0.3 V	≥ 18 dB 50 kHz to 3 MHz
1.544[2] **	B8ZS, AMI	DSX-1 compatible		

1 3035/02 requires option 3035/90.33
2 3035/01 requires option 3035/90.34

Table S-2 LINE/AUXILIARY output [13] signal specifications, electrical

1.2 Clock generation and bit rates

1.2.1 Internal clock generation

Bit rate range . . . . . 1.544 Mbit/s to 155.52 Mbit/s

Frequency deviation ***, ** . . . . . ± 2 ppm ±1 ppm/year

Settable offset. . . . . ± 500 ppm

Minimum setting step width . . . . . 0.001 ppm (1 ppb)

Intrinsic jitter (clock) . . . . . 0.010 UI

1.2.2 Synchronization to external signals

Derived from RX clock

The TX bit rate is derived from the RX clock. The jitter of the incoming signal is suppressed.

TX side offset setting . . . . . ± 500 ppm

Minimum setting step width . . . . . 0.001 ppm (1 ppb)

Limit frequency above which jitter is suppressed . . . . . approx. 100 Hz

Max. permissible receive clock (receive signal) offset:
TX bit rate ≥ 51.84 Mbit/s . . . . . ± 10 ppm
TX bit rate < 51.84 Mbit/s . . . . . 50 ppm

No TX offset is possible for DROP&INSERT operation (Option 3035/90.20).

Derived from reference clock

The TX bit rate is derived from:

- reference clock T3 (2.048 MHz)
- data signal 2.048 Mbit/s
- reference clock DS1 (1.544 MHz)
- data signal 1.544 Mbit/s

The jitter in the incoming signal is suppressed (see Sec. 7.3, Page S-37).

Settable offset, referred to 1.544 MHz or 2.048 MHz . . . . . ± 500 ppm

Minimum setting step width . . . . . 0.001 ppm (1 ppb)

Limit frequency above which jitter is suppressed . . . . . approx. 1 Hz

Max. permissible reference signal offset . . . . . ≤ 10 ppm

2 Receiver section

2.1 Digital signal inputs

2.1.1 LINE signal input [14], electrical

Connector . . . . . unbalanced (coaxial)

Socket . . . . . UNI 9 (Versacon®)

Input impedance . . . . . 75 Ω

Max. permissible frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for code = AMI 15

Switchable input voltage ranges ***, ** “ITU-T” (“High”) . . . . . 0 dB attenuation referred to nominal level

“PMP” (“Low”) CMI . . . . . 15 to 23 dB attenuation referred to nominal level

“PMP” (“Low”) B3ZS, B8ZS, HDB3, AMI . . . . 15 to 26 dB attenuation referred to nominal level

Max. peak input voltage . . . . . ± 5 V

Interface[3]	Bit rate (Mbit/s)	Line code	Signal equalization (adaptive)	Reflexion coefficient
STS-3 STM-1	155.520	CMI	max. 12.7 dB/78 MHz	≥ 15 dB 100 kHz to 240 MHz
STM-0	51.840	HDB3	max. 12 dB/17 MHz[4]	≥ 18 dB 50 kHz to 52 MHz
STS-1		B3ZS		
DS3	44.736[2]	B3ZS		
DS1	1.544[2]	B8ZS, AMI	max. 6 dB/0.772 MHz[5]	
DS2	6.312[2]	B8ZS	max. 6 dB/3 MHz	≥ 18 dB 100 kHz to 52 MHz
E4	139.264[1]	CMI	max. 12 dB/70 MHz	≥ 15 dB 100 kHz to 240 MHz
E3	34.368[1]	HDB3	max. 12 dB/17 MHz	≥ 18 dB 50 kHz to 52 MHz
E2	8.448[1]	HDB3	max. 6 dB/4 MHz	
E1	2.048[1]	HDB3	max. 6 dB/1 MHz	

1 3035/02 requires option 3035/90.33
2 3035/01 requires option 3035/90.34
3 depends on ANT-20SE versions and options
4 Adaptive equalizer allows ≥ 450 ft 728A cable (DSX3 level)
5 Adaptive equalizer allows ≥ 655 ft 22AWG cable

Table S-3 LINE input [14] signal specifications, electrical

Tolerance to jitter

Measured using PRBS 15 (≥ 8 Mbit/s) and PRBS 23 (> 8 Mbit/s) with “ITU-T” and “PMP” receive levels attenuated by 20 dB referred to the nominal level.

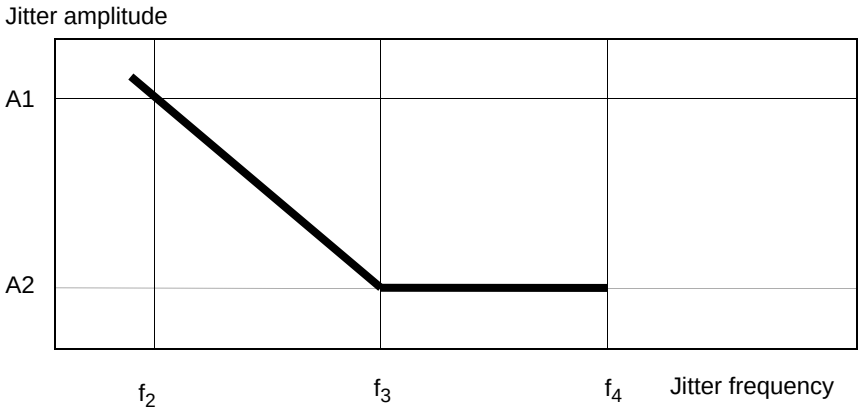


Fig. S-1 Relationship between jitter amplitude and jitter frequency

Bit rate Mbit/s	Line code	A1 Ulpp	f_2 kHz	A2 Ulpp	f_3 kHz	f_4 kHz
1.544[2]	B8ZS	5	0.5	0.25	20	200
2.048[1]	HDB3	10	0.5	0.25	20	200
6.312	B8ZS	10	1.5	0.25	60	600
8.448[1]	HDB3	10	2	0.25	80	800
34.368[1]	HDB3	10	6	0.25	240	2000
44.736[2]	B3ZS	10	6	0.25	240	2000
51.840	B3ZS	10	6	0.25	240	2000
139.264[1]	CMI	10	20	0.25	800	3500
155.520	CMI	10	22	0.25	880	3500

1 3035/02 requires option 3035/90.33
2 3035/01 requires option 3035/90.34

Table S-4 ANT-20SE tolerance to jitter at system bit rates

LOS (Loss of Signal) status display

LED is on if the signal input is active but no signal is present.

2.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket: 3035/01 . . . . . Lemo SA
Socket: 3035/02 . . . . . Bantam

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permissible frequency offset . . . . . ± 500 ppm
Max. number of
consecutive zeros for code = AMI 15

Switchable input voltage ranges
“ITU-T” (“High”) . . . . . 0 dB attenuation referred to nominal level
“PMP” (“Low”) . . . . . 15 to 26 dB attenuation referred to nominal level

Max. peak input voltage . . . . . ± 5 V

Bit rate (Mbit/s)	Line code	Reflection coefficient
2.048[1]	HDB3	≥ 18 dB 50 kHz to 3 MHz
1.544[2]	B8ZS, AMI	

1 3035/02 requires option 3035/90.33
2 3035/01 requires option 3035/90.34

Table S-5 Input signal specifications “LINE/AUXILIARY” [12], electrical

Tolerance to jitter

As per Tab. S-4, Page S-7

LOS (Loss of Signal) status display

LED is on if the signal input is active but no signal is present.

2.2.1 Clock recovery

The appropriate bit clock is derived from the input signal and the offset from the nominal clock rate is measured.

Offset display, in ppm 3-digit

Display resolution . . . . . 1 ppm

No offset measurement is possible for “Through Mode” and “TX clock from RX”.

The recovered clock can be used for synchronizing the TX bit rate (see Sec. 1.2.2, Page S-4).

3 DS1 and DS3 signals

Available with ANT-20SE version 3060/02 or
with ANT-20SE version 3060/01 and option 3035/90.34.

Test signals for bit error measurements.

Signal structure for all bit rates

- unframed test pattern
- framed test pattern (except DS2)

Test pattern

Digital word . . . . . length 16 bits

Pseudo-random bit sequences . . . . . .PRBS 11, PRBS 11 invers, PRBS 15, PRBS 15 invers, PRBS 20, PRBS 23, PRBS 23 invers, QRSS 20 (QRSS 20 with max. 14 zeros)

Frames

DS3 . . . . . M13 frame, C-Parity

DS2 . . . . . unframed only

DS1 . . . . . .D4 (SF), ESF (ANSI T1.107)

3.1 Error insertion and alarm generation (TX)

3.1.1 Error insertion (anomalies)

Error insertion (anomalies) . . . . . bit errors in test pattern (TSE), code errors (single errors only)

Trigger types . . . . . Single or Rate

Tip: When Rate triggering is selected a bit error rate is inserted.

Anomaly	**Single**	**Rate**[1]
FE-DS1	yes	2E-3 to 1E-8
CRC6	yes	2E-3 to 1E-8
FE-DS3	yes	2E-3 to 1E-8
P-Parity-DS3	yes	2E-3 to 1E-8
CP-Parity-DS3	yes	2E-3 to 1E-8
FEBE-DS3 (REI 45)	yes	2E-3 to 1E-8
TSE	yes	1E-2 to 1E-8
BPV	yes	-
1 Mantissa: 1 to 9 (only 1 for TSE), exponent: -1 to -8 (whole numbers)		

Table S-6 Available anomalies and trigger modes

The insertion of **errors** (anomalies) **and alarms** (defects) is mutually exclusive. The first action selected is active. The second action is rejected.

3.1.2 Alarm generation (defects)

Defect	Test sensor function	Test sensor threshold
AIS-DS1, AIS-DS3, IDLE-DS3, FEAC-DS3	On/Off	-
LOF-DS1	On/Off	2/4, 2/5, 2/6[1]
LOF-DS3	On/Off	2/2, 2/3, 3/3, 3/15, 3/16, 3/17[1]
YELLOW-DS1, YELLOW-DS3 (RDI)	On/Off	-
1 (see Tab. S-8)		

Table S-7 Available defects

The insertion of **errors** (anomalies) **and alarms** (defects) is mutually exclusive. The first action selected is active. The second action is rejected.

DS1	DS3	Insertion
2 in 4	-	1st and 4th Ft bit in every second (E)SF inverted
2 in 5	-	1st and 5th Ft bit in every second (E)SF inverted
2 in 6	-	1st and 6th Ft bit in every second (E)SF inverted
-	2 in 2	1st and 2nd F bit in every multiframe inverted
-	2 in 3	1st and 3rd F bit in every multiframe inverted
-	3 in 3	1st, 2nd and 3rd F bit in every multiframe inverted
-	3 in 15	1st, 8th and 15th F bit in every multiframe inverted
-	3 in 16	1st, 9th and 16th F bit in every multiframe inverted
-	3 in 17	1st, 9th and 17th F bit in every multiframe inverted

Table S-8 DS1/DS3 alarm generation

3.2 Error measurement and alarm detection (RX)

3.2.1 Error measurement (anomalies)

Evaluation

All errors (anomalies) are counted simultaneously and stored.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

of anomalies via LEDs:

CURRENT LED (red) is on when the anomaly is present

HISTORY LED (yellow) is on if the anomaly occurred at least once or is active within the started measurement interval.

Anomaly	**LED**
FE-DS1, FE-DS3, MFE-DS3	FAS/CRC
CRC6	FAS/CRC
P-DS3, CP-DS3	-
TSE	TSE
BPV	-
DS3-REI	-

Table S-9 LED display of available anomalies

3.2.2 Alarm detection (defects)

Evaluation

All alarms (defects) which occur are evaluated simultaneously where possible and stored. Storage takes place only within a started measurement interval

Time resolution of defects . . . . . .100 ms

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

Defect	**LED**
AIS-DS1, AIS-DS3	AIS
LOF-DS3, OOF-DS3 LOF-DS1, OOF-DS1	LOF/LCD
DS1-YELLOW, DS3-YELLOW	RDI(AIS-)/YELLOW
IDLE-DS3, FEAC-DS3	-

Table S-10 LED display of available defects

Tip: DS3-AIC is used for autoconfiguring the instrument and can only be read out via remote control.

3.3 Drop&Insert / Through Mode

Option: BN 3035/90.20

3.3.1 Functions

This Option provides the following functions for all PDH multiplex options fitted to the ANT-20SE.

Drop&Insert

This function is only available in conjunction with the following options:

- PDH MUX/DEMUX chain: BN 3035/90.30 to BN 3035/90.31
  M13 MUX/DEMUX chain: BN 3035/90.32

– or –

- STM-1 mappings: BN 3035/90.01 to BN 3035/90.05
  STS-1 mappings: BN 3035/90.10 to BN 3035/90.13

– or –

- Optical interfaces: BN 3035/90.40 to BN 3035/90.48
  BN 3035/90.50 and BN 3035/90.51

The characteristics and specifications for the Drop&Insert function are given in the descriptions for the various options.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator.

The ANT-20SE operates in Through Mode as a signal monitor without affecting the signal.

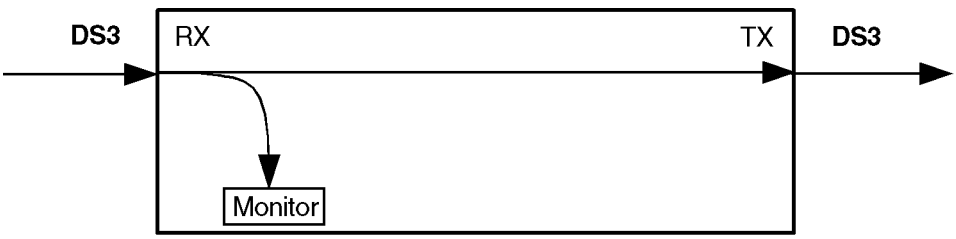


Fig. S-2 Through Mode: Generator and receiver coupled

The ANT-20SE provides access to the tributary channels within the “MUX/DEMUX” chain when used in conjunction with the “PDH MUX/DEMUX” and “M13 MUX/DEMUX” options, BN 3035/90.30 to BN 3035/90.32. This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

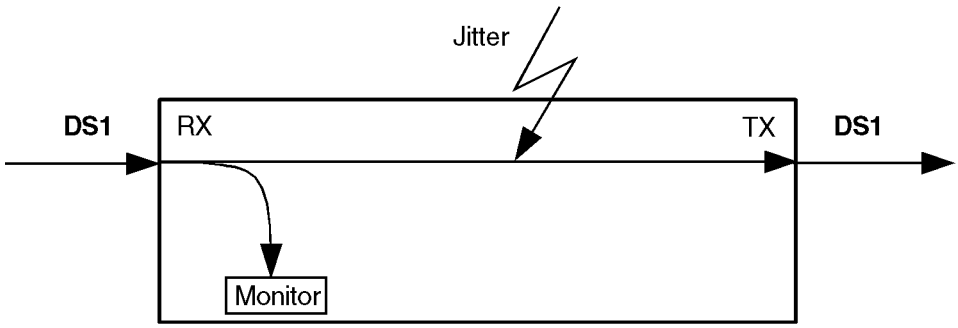


Fig. S-3 Through Mode: Adding jitter to the looped-through signal

3.3.2 Clock generator

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No offset is possible in this operating mode (see Sec. 1.2.2, Page S-4).

3.3.3 Anomaly insertion

Through Mode

Anomaly insertion . . . . . BPV, B1, B2 and REI-L

3.3.4 Defect generation

Through Mode

Defect generation is not possible.

3.3.5 Measurements

There are no restrictions on measurements (see Sec. 3.2, Page S-12).

4 E1 to E4 signals

Available with ANT-20SE version 3060/01 or
with ANT-20SE version 3060/02 and option 3035/90.33.

Test signals for bit error measurements.

Signal structure for all bit rates

- unframed test pattern
- framed test pattern

Test pattern

Digital word . . . . . length 16 bits

Pseudo-random bit sequences . . . . . PRBS 11, PRBS11 invers, PRBS 15, PRBS 20, PRBS 23, PRBS 23 invers

Frames

E1 (2.048 Mbit/s; G.704/706) . . . . . PCM 30/31 with and without CRC

E2 (8.448 Mbit/s; G.742) . . . . . PCM 120

E3 (34.368 Mbit/s; G.751) . . . . . PCM 480

E4 (139.264 Mbit/s; G.751) . . . . . PCM 1920

4.1 Error insertion and alarm generation (TX)

4.1.1 Error insertion (anomalies)

Error insertion (anomalies) . . . . . bit errors in test pattern (TSE), code errors (single errors only)

Trigger types . . . . . .Single or Rate

Tip: When Rate triggering is selected a bit error rate is inserted.

Anomaly	**Single**	**Rate**[1]
FAS-140, FAS-3, FAS-8, FAS-2	yes	2E-3 to 1E-8
TSE	yes	1E-2 to 1E-8
BPV	yes	-
1 Mantissa: 1 to 9 (only 1 for TSE), exponent: -1 to -10 (whole numbers)		

Table S-11 Available anomalies and trigger modes

The insertion of **errors** (anomalies) **and alarms** (defects) is mutually exclusive. The first action selected is active. The second action is rejected.

4.1.2 Alarm generation (defects)

Defect	**Test sensor function**	**Test sensor thresholds**
-	On/Off	M in N
AIS-140, AIS-34, AIS-8, AIS-2	yes	-
LOF-140, LOF-34, LOF-8, LOF-2	yes	M = 1 to N-1 N = 1 to 1000
RDI -140, RDI-34, RDI-8, RDI-2	yes	M = 1 to N-1 N = 1 to 1000

Table S-12 Available defects

The insertion of **alarms** (defects) **and errors** (anomalies) is mutually exclusive. The first action selected is active. The second action is rejected.

4.2 Error measurement and alarm detection (RX)

4.2.1 Error measurement (anomalies)

Evaluation

All errors (anomalies) are counted simultaneously and stored.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

of anomalies via LEDs:

CURRENT LED (red) is on when the anomaly is present

HISTORY LED (yellow) is on if the anomaly occurred at least once or is active within the started measurement interval.

Anomaly	**LED**
FAS-140, FAS-34, FAS-8, FAS-2	FAS/CRC
CRC-4[1]	FAS/CRC
E bit[1]	-
TSE	TSE
BPV	-
1 Requires option 3035/90.30 or 3035/90.31	

Table S-13 LED display of available anomalies

4.2.2 Alarm detection (defects)

Evaluation

All alarms (defects) which occur are evaluated simultaneously where possible and stored. Storage takes place only within a started measurement interval.

Time resolution of defects . . . . . .100 ms

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

Defect	**LED**
AIS-140, AIS-34, AIS-8, AIS-2, AIS-64k	AIS
LOF-140, LOF-34, LOF-8, LOF-2	LOF/LCD
LSS	LSS
RDI-140, RDI-34, RDI-8, RDI-2	RDI(AIS-)/YELLOW

Table S-14 LED display of available defects

4.3 Drop&Insert / Through Mode

Option: BN 3035/90.20

4.3.1 Functions

This Option provides the following functions for all PDH multiplex options fitted to the ANT-20SE.

Drop&Insert

This function is only available in conjunction with the following options:

- PDH MUX/DEMUX
  M13 MUX/DEMUX: BN 3035/90.30 to BN 3035/90.32

– or –

- STM-1 mappings: BN 3035/90.01 to BN 3035/90.05
  STS-1 mappings: BN 3035/90.10 to BN 3035/90.13

– or –

- Optical interfaces BN 3035/90.40 to BN 3035/90.48
  BN 3035/90.50 and BN 3035/90.51

The characteristics and specifications for the Drop&Insert function are given in the descriptions for the various options.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator.

The ANT-20SE operates in Through Mode as a signal monitor without affecting the signal.

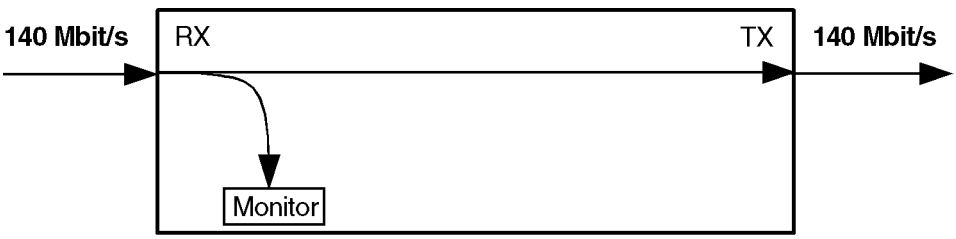


Fig. S-4 Through Mode: Generator and receiver coupled

The ANT-20SE provides access to the tributary channels within the “MUX/DEMUX” chain when used in conjunction with the “PDH MUX/DEMUX” and “M13 MUX/DEMUX” options, BN 3035/90.30 to BN 3035/90.32. This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

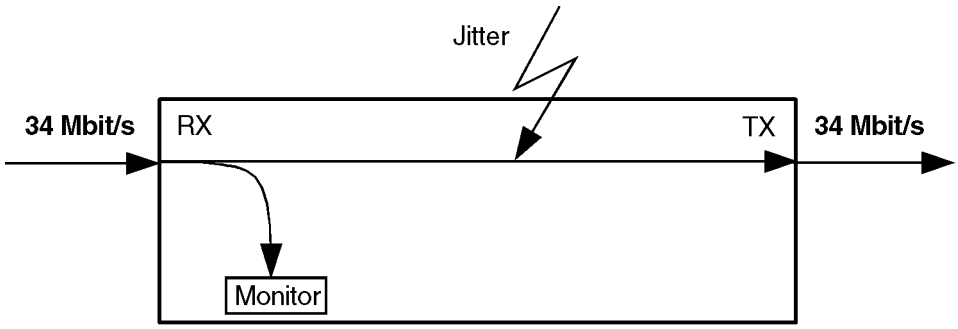


Fig. S-5 Through Mode: Adding jitter to the looped-through signal

4.3.2 Clock generator

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No offset is possible in this operating mode (see Sec. 1.2.2, Page S-4).

4.3.3 Anomaly insertion

Through Mode

Anomaly insertion . . . . . BPV, B1, B2 and MS-REI

4.3.4 Defect generation

Through Mode

Defect generation is not possible.

4.3.5 Measurements

There are no restrictions on measurements (see Sec. 4.2, Page S-18).

5 Measurement modes

5.1 Evaluation to ANSI/BELL

Evaluations can be performed on the following levels (alternatives):

- SONET: Section, line, STS path, VT path
- DS3: Line, path
- DS1: Line, path
- Bit

“Near End” and “Far End” analyses are performed simultaneously if available.

ES, SES, EFS, SEFS and UAS are evaluated.

The SES and UAS threshold settings correspond to GR-253 (Performance Monitoring) and T1.231.

5.2 Evaluation to ITU-T G.821

ES, EFS, SES and UAS are evaluated; DM (degraded minutes) are also evaluated.
The multiplex factor used in older versions of Recommendation G.821 (Annex D) can be applied if required.

G.821 evaluation can be performed on the following events:

- FAS bit errors (FAS 2, FAS 8, FAS 34, FAS 140)
- CRC errors
- E bit errors
- Bit errors (TSE, Test Sequence Error)

The following signals can be measured when performing G.821 evaluation of bit errors (TSE):

- unframed patterns
- n x 64 kbit/s
- framed patterns and bulk signals
- Overhead bytes E1, E2, F1, F2, D1 to D3 and D4 to D12

Pass/fail assessment in conjunction with path allocation of between 0.1 and 100%.

The SES threshold can be set as required.

Since G.821 evaluation requires evaluation of bit errors, facilities for evaluating block errors are disabled.

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

5.3 Evaluation to ITU-T G.826

The following are evaluated: EB, BBE, ES, EFS, SES and UAS.
Pass/Fail assessment depending on path allocation of 0.1 to 100%.
The thresholds for SES and UAS can be set by the user.

In-service measurement (ISM)

Simultaneous in-service measurement of “near end” and “far end” of a selected path:

Near end: HP-B3, LP-B3, BIP2, FAS bei 140/34/8 oder 2M, CRC 4, DS3FAS, DS3-P-Parity, DS3-C-Parity, DS1FAS, D1-CRC6

Far end: HP-REI, LP-REI, E-Bit bei 2M, DS3-FEBE

Out-of-service measurement (OOS)

Out-of-service measurement using bit errors in a test pattern (for PDH and SDH).

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

5.4 Evaluation to ITU-T G.828

ES, EFS, SES, UAS, BBE and SEP are evaluated.

Pass/fail assessment in conjunction with path allocation of between 0.1 and 100%.

The thresholds for SES and UAS can be set by the user.

G.828 evaluation can be performed on the following events:

- B1
- B2SUM
- MS-REI
- B3
- HP-REI
- LP-BIP 2/8
- LP-REI
- Biterrors (TSE)

Evaluation of the near end and the far end is simultaneous as soon as the signal structure set allows a far end measurement.

Far end evaluations can only be made if REI is available.

Bit errors can be evaluated for:

- unframed patterns
- framed patterns and bulk signals
- Overhead bytes E1, E2, F1, F2, F2L, D1 through D3 and D4 through D12 in the SOH/POH of SDH signals

As the G.828 evaluation measures block errors, bit error evaluation cannot be activated.

Display

of defects using LED indicators
(also in the Anomaly/Defect Analyzer – Summary display window):

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

5.5 Evaluation to ITU-T G.829

ES, EFS, SES, UAS and BBE are evaluated..

The SES threshold can be set as required.

G.829 evaluation can be performed on the following events:

- B1
- B2SUM
- MS-REI
- Bit errrors (TSE)

Evaluation of the near end and the far end is simultaneous as soon as the signal structure set allows a far end measurement.

Far end evaluations can only be made if REI is available.

Bit errors can be evaluated for:

- unframed patterns
- framed patterns and bulk signals
- Overhead bytes E1, E2, F1, F2, F2L, D1 through D3 and D4 through D12 in the SOH/POH of SDH signals

The special block error evaluation using BIP-1 blocks means that the instrument is run in bit error evaluation mode. It is therefore not possible to switch to block error evaluation. This does not apply to the TSE meas. point, for which real block errors are evaluated. Therefore you cannot switch to bit error evaluation when making a G.829 evaluation on TSEs.

Display

of defects using LED indicators
(also in the Anomaly/Defect Analyzer – Summary display window):

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

5.6 Evaluation to ITU-T M.2100

ES, EFS, SES and UAS are evaluated.

Pass/Unknown/Fail assessment based on the threshold values S1 and S2 for ES and SES. The threshold values are calculated internally as per M.2100 and displayed in the results window.

Settings for S1 and S2:

Path allocation . . . . . 0.1 to 100%

BISO (“Bringing into Service Objectives”) multiplication factor. . . . . .0.1 to 100

The M.2100 evaluation can be performed on the following events:

- FAS bit errors (FAS1.5, FAS2, FAS8, FAS34, FAS45 and FAS140)
- CRC-4 errors
- CRC-6 errors
- EBIT errors
- PBIT errors
- Bit errors (TSE)

For PCM30CRC signals, evaluation is made at the “Near End” and at the “Far End” simultaneously.

Bit errors can be evaluated for:

- unframed patterns
- framed patterns and bulk signals
- n x 64 kbit/s
- Overhead bytes E1, E2, F1, F2, D1 to D3 and D4 to D12

Since M.2100 evaluation requires evaluation of bit errors, facilities for evaluating block errors are disabled.

Display

of defects using LED indicators
(also in the Anomaly/Defect Analyzer – Summary display window):

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

5.7 Evaluation to ITU-T M.2101

ES, EFS, SES, UAS, BBE and SEP are evaluated.

Pass/Unknown/Fail assessment based on the threshold values S1 and S2 for ES, SES, BBE and SEP. The threshold values are calculated internally as per M.2101 and displayed in the results window.

Settings for S1 and S2:

Path allocation . . . . . 0.1 to 100%

BISO (“Bringing into Service Objectives”) multiplication factor . . . . . 0.1 to 100

The M.2101 evaluation can be performed on the following events:

- B1
- B2SUM
- MS-REI
- B3
- HP-REI
- LP-BIP 2/8
- LP-REI
- Bit errors (TSE)

Evaluation of the near end and the far end is simultaneous as soon as the signal structure set allows a far end measurement.

Far end evaluations can only be made if REI is available.

Bit errors can be evaluated for:

- unframed patterns
- framed patterns and bulk signals
- Overhead bytes E1, E2, F1, F2, F2L, D1 through D3 and D4 through D12 in the SOH/POH of SDH signals

As the M.2101 evaluation measures block errors, bit error evaluation cannot be activated. Exception: B2SUM. BIP-1 blocks are used for this. These are only accessible in the instrument via a bit error measurement. For this reason, block error evaluation is not available for a M.2101 evaluation on B2SUM.

Display

of defects via LEDs
(also in the Anomaly/Defect Analyzer – Summary display window):

CURRENT LED (red) is on when the defect is present.

HISTORY LED (yellow) is on if the defect occurred at least once or is active within the started measurement interval.

6 Automatic measurements

6.1 Auto configuration

The auto configuration function sets the ANT-20SE receiver automatically. The routine searches for the presence of standard SDH, SONET, PDH or ATM signals at the electrical inputs (for the input level ranges “ITU-T”/“High” or “PMP”/“Low”), or at the optical inputs. The instrument version and options fitted are taken into account. The main emphasis is placed on detecting the signal structure. Detailed matching to the signal contents can be carried out manually if desired.

The sequence is divided into three parts:

- Check Interface
- Check Mapping
- Check Payload

6.1.1 Check Interface

Matching to the physical parameters (bit rate/code)

Allowed-for defects . . . . . LOS

Other factors . . . . . input bit rate frequency offset > 150 ppm

6.1.2 Check Mapping

A check is made for the mapping structure using the Signal Label and the pointer bytes (to differentiate between AU-4 and AU-3). The check is always made in channel #1.

With STM-16 / OC-48 signals, a check is made for an AU-4 structure only in “ITU-T” mode or for an AU-3 structure only in “ANSI” mode.

OC-12c/STM-4c Virtual Concatenation is not recognized by the autoconfiguration function.

Allowed-for defects:

Defect (SDH)	Defect (SONET)
LOF/OOF	LOF/OOF
AU-AIS	AIS-P
MS-AIS	AIS-L
TU-AIS	AIS-V
AU-LOP	LOP-P
TU-LOP	LOP-V
LOM	LOM

Table S-15 Defects allowed for during auto configuration

If UNEQuipped is detected, the mapping previously selected or a default mapping will be set.

Auto configuration recognizes “C-11 via TU-12” mapping as “C-12” mapping.

6.1.3 Check Payload

The check only takes account of the test patterns recommended in the relevant standards.

6.1.3.1 PDH signals

Checks for unframed or framed payload signals on all hierarchy levels

Allowed-for defects . . . . . LOF/(OOF)
AIS

6.1.3.2 ATM signals

Checks for ATM signals

Allowed-for defects . . . . . LOF/(OOF), AIS, LCD
LOF PLCP, AIC, IDLE DS3

6.1.4 Structure and results

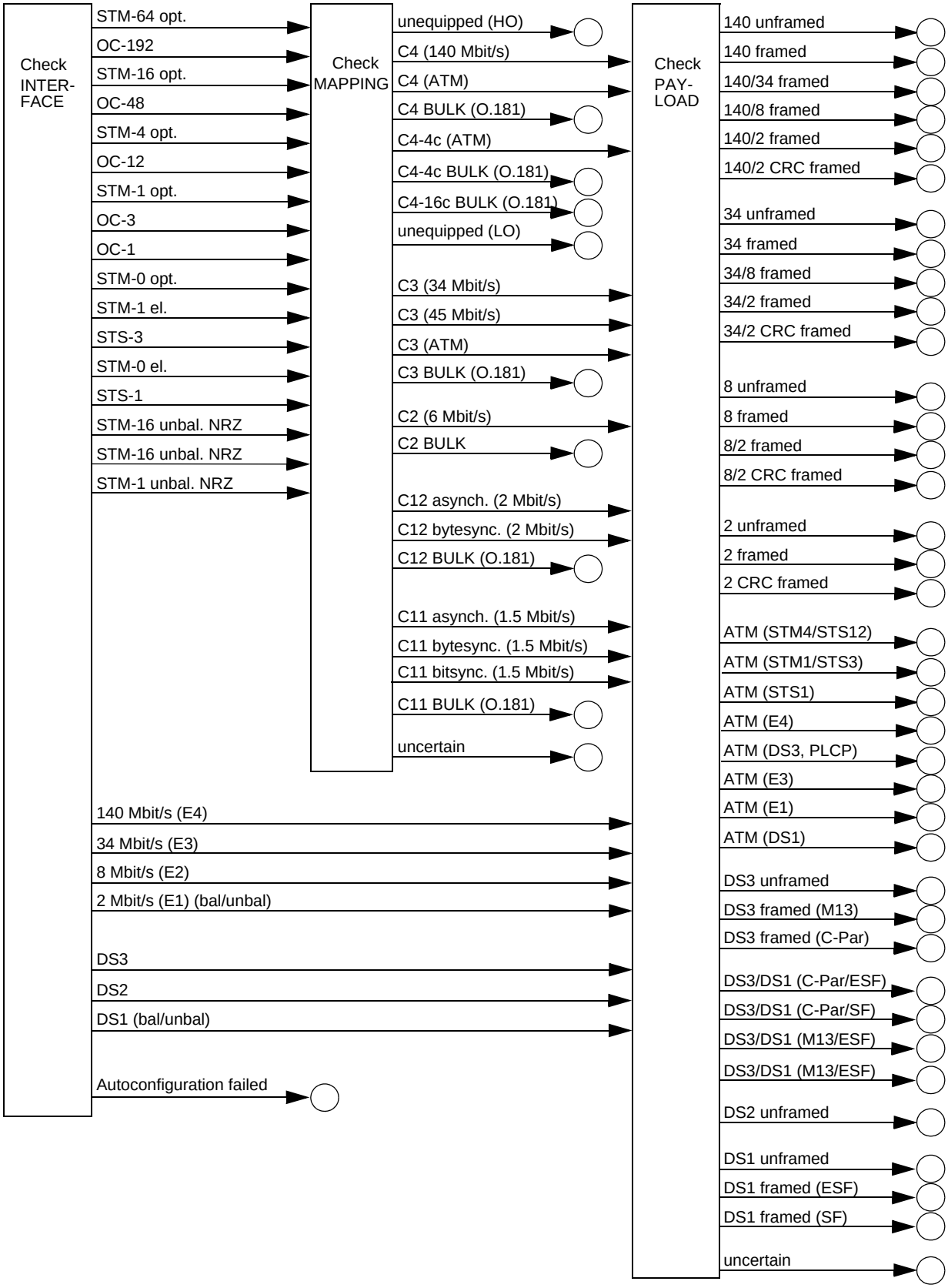


Fig. S-6 Structure and results

6.2 Automatic “Scan” function

The “Scan” function permits sequential testing of all tributary channels in an SDH or SONET signal. The appropriate mapping options are needed for this.

SDH signals . . . . . C-12 mapping
C-11 mapping
C-11/TU-12 mapping
C2 mapping

SONET signals . . . . . VT1.5 mapping
VT2 mapping
VT6 mapping

The test is performed within an AU (SDH version) or a SPE (SONET version). Selection of the various AUs / SPEs for signals with higher bit rates is done manually.

The settings for the generator and receiver must be matched for loop measurements.

The channel scan takes place synchronously on the transmit and receive sides. If the signal structure settings differ, only the receive channel settings will be altered.

The ANT-20SE receiver checks the receive signal defects and those of the corresponding SDH or SONET structure and of the channel and enters the results of the single channels in a matrix.

Allowed-for defects:

Defect (SDH)	**Defect (SONET)**
LOS	LOS
LOF/OOF (SDH)	LOF/OOF (SONET)
AU-AIS	AIS-P
MS-AIS	AIS-L
TU-AIS	AIS-V
AU-LOP	LOP-P
TU-LOP	LOP-V
HP-UNEQ	UNEQ-P
LP-UNEQ	UNEQ-V
TU-LOM	LOM
AIS (2 Mbit/s)	AIS (E1)
LOF (2 Mbit/s)	LOF (E1)
AIS (1.5 Mbit/s)	AIS (DS1)
LOF (1.5 Mbit/s)	LOF (DS1)
OOF (1.5 Mbit/s)	OOF (DS1)
AIS (64 kbit/s)	AIS (64 kbit/s)
LSS	LSS

Table S-16 Defects allowed for during the “Scan” function

6.3 Automatic “Search” function

The “Search” function allows you to search for a tributary channel in a SDH or SONET signal. The appropriate mapping options are needed for this.

SDH signals . . . . . C-12 mapping
C-11 mapping
C-11/TU-12 mapping
C2 mapping

SONET signals . . . . . VT1.5 mapping
VT2 mapping
VT6 mapping

The test is performed within an AU (SDH version) or a SPE (SONET version). Selection of the various AUs / SPEs for signals with higher bit rates is done manually.

During the search, only the receive channels are altered.

The ANT-20SE receiver checks the receive signal defects and those of the corresponding SDH or SONET structure and of the channel and enters the results of the single channels in a matrix.

Allowed-for defects:

Defect (SDH)	**Defect (SONET)**
LOS	LOS
LOF/OOF (SDH)	LOF/OOF (SONET)
AU-AIS	AIS-P
MS-AIS	AIS-L
TU-AIS	AIS-V
AU-LOP	LOP-P
TU-LOP	LOP-V
HP-UNEQ	UNEQ-P
LP-UNEQ	UNEQ-V
TU-LOM	LOM
AIS (2 Mbit/s)	AIS (E1)
LOF (2 Mbit/s)	LOF (E1)
AIS (1.5 Mbit/s)	AIS (DS1)
LOF (1.5 Mbit/s)	LOF (DS1)
OOF (1.5 Mbit/s)	OOF (DS1)
AIS (64 kbit/s)	AIS (64 kbit/s)
LSS	LSS

Table S-17 Defects allowed for in the “Search” function

6.4 Automatic “Trouble Scan” function

The “Trouble Scan” function permits sequential testing of all tributary channels in an SDH or SONET signal. The appropriate mapping options are needed for this.

SDH signals . . . . . C-12 mapping
C-11 mapping
C-11/TU-12 mapping
C2 mapping

SONET signals . . . . . VT1.5 mapping
VT2 mapping
VT6 mapping

The test is performed within an AU (SDH version) or a SPE (SONET version). Selection of the various AUs / SPEs for signals with higher bit rates is done manually.

During the “Trouble Scan”, only the receive channels are altered.

The ANT-20SE receiver checks the receive signal defects and those of the corresponding SDH or SONET structure and of the channel and enters the results of the single channels in a matrix. You can display a detailed alarm history by selecting an individual channel from within the matrix.

Allowed-for defects:

Defect (SDH)	**Defect (SONET)**
LOS	LOS
LOF/OOF (SDH)	LOF/OOF (SONET)
AU-AIS	AIS-P
MS-AIS	AIS-L
TU-AIS	AIS-V
AU-LOP	LOP-P
TU-LOP	LOP-V
MS-RDI	RDI-L
HP-RDI	RDI-P
LP-RDI	RDI-V
HP-UNEQ	UNEQ-P
LP-UNEQ	UNEQ-V
TU-LOM	LOM
HP-PDI	PDI-P
LP-PDI	PDI-V
AIS (2 Mbit/s)	AIS (E1)
LOF (2 Mbit/s)	LOF (E1)
RDI (2 Mbit/s)	RDI (E1)

Table S-18 Defects allowed for in the “Trouble Scan” function

Defect (SDH)	Defect (SONET)
AIS (1.5 Mbit/s)	AIS (DS1)
LOF (1.5 Mbit/s)	LOF (DS1)
OOF (1.5 Mbit/s)	OOF (DS1)
YELLOW (1.5 Mbit/s)	YELLOW (DS1)

Table S-18 Defects allowed for in the “Trouble Scan” function *(continued)*

6.5 Automatic “Signal Delay” measurement

The ANT-20SE measures the signal delay between the generator and receiver using characteristic sequences in the selected PRBS. The signal delay measurement is automatic and continuous, i.e. individual measurements are repeatedly performed. Practically any signal structure that can be set on the ANT-20SE can be used for the measurement.

Exceptions:

- ATM signal structures
- Overhead measurements
- Through Mode
- ADM test

The measurement range and measurement time depend on the pattern bit rate and the selected pattern.
The maximum possible measurement value depends on the length of the PRBS. The maximum value is calculated and shown in the results window. This value can be influenced by selecting a shorter or a longer test pattern.

Signal structure	Short test pattern	Max. measured value, in ms	Long test pattern	Max. measured value, in ms
C4 Bulk	PRBS23[1]	56	-	56
C3 Bulk	PRBS23[1]	173	-	173
C2 Bulk	PRBS20	154	PRBS23	1236
C12 Bulk	PRBS20	481	PRBS23	3855
C11 Bulk	PRBS20	655	PRBS23	5242
140M unframed	PRBS23[1]	60	-	60
140M framed	PRBS23[1]	60	-	60
45M unframed	PRBS23[1]	187	-	187
45M framed	PRBS23[1]	189	-	189
34M unframed	PRBS23[1]	244	-	244
34M framed	PRBS23[1]	246	-	246
8M unframed	PRBS20	124	PRBS23	992
8M framed	PRBS20	125	PRBS23	985
6M unframed	PRBS20	166	PRBS23	1328
6M framed	PRBS20	169	PRBS23	1356
2M unframed	PRBS20	512	PRBS23	4096
2M framed PCM30	PRBS20	546	PRBS23	4369
2M framed PCM31	PRBS20	528	PRBS23	4228
1.5M unframed	PRBS20	679	PRBS23	5433
1.5M framed	PRBS20	682	PRBS23	5461

1 Measurement only possible with this test pattern
2 depending on n

Table S-19 Max. measurement values as a function of signal structure and test pattern

Signal structure	Short test pattern	Max. measured value, in ms	Long test pattern	Max. measured value, in ms
n x 64 k unframed (25 ≤ n ≤ 32)	PRBS20	511 to 655[2]	PRBS23	4095 to 5242[2]
n x 64 k unframed (17 ≤ n ≤ 24)	PRBS20	682 to 963[2]	PRBS23	5461 to 7710[2]
n x 64 k unframed (9 ≤ n ≤ 16)	PRBS15	31 to 56[2]	PRBS23	8191 to 14563[2]
n x 64 k unframed (2 ≤ n ≤ 8)	PRBS15	255 to 63[2]	PRBS20	2047 to 8191[2]
64k unframed	PRBS15	511	PRBS20	16383

1 Measurement only possible with this test pattern
2 depending on n

Table S-19 Max. measurement values as a function of signal structure and test pattern *(continued)*

The accuracy and display resolution also depend on the pattern bit rate.

Pattern bit rate	Accuracy	Resolution
64 kbit/s < 1.544 Mbit/s	± 200 µsec	100 µsec
1.544 Mbit/s ≤ 8.448 Mbit/s	± 10 µsec	10 µsec
> 8.448 Mbit/s	± 1 µsec	1 µsec

Table S-20 Delay measurement accuracy as a function of pattern bit rate

7 Other inputs and outputs

7.1 DCC/ECC [21]

Interface for inserting/outputting TOH/POH bytes.

The bytes are filled dynamically in real-time with a contradirectional clock and synchronization signal for n x 64 kbit/s channels per frame.

The clock signal is smoothed. The RX data signal is sampled on the falling edge of the RX clock. Exchange of TX data takes place on the rising edge of the TX clock.

64 kbit/s: 1 byte/frame
128 kbit/s: 2 bytes/frame
192 kbit/s: 3 bytes/frame
576 kbit/s: 9 bytes/frame

Interface to. . . . . V.11 (ITU-T X.24 and X.27)

Socket [21]. . . . . .MINI DELTA RIBBON, 20-pole

Pin no.	Signal	Input/Output
1	Ground	
2	Ground	
3	RX data	Input
4	RX data (inv)	Input
5	RX control	Output
6	RX control (inv)	Output
7	RX clock	Input/Output
8	RX clock (inv)	Input/Output
9	RX synch	Input/Output
10	RX synch (inv)	Input/Output
11	TX data	Output
12	TX data (inv)	Output
13	TX control	Output
14	TX control (inv)	Output
15	TX clock	Output
16	TX clock (inv)	Output
17	TX synch	Output
18	TX synch (inv)	Output
19	Ground	
20	+5 V/100 mA	
(inv): inverted signal		

Table S-21 DCC/ECC interface pin signals (V.11)

7.2 TRIGGER [26]

Socket . . . . . BNC

Input

Input impedance . . . . . 75 Ω

Permitted pulse amplitude range . . . . . HCMOS level

Max. peak input voltage . . . . . ± 6 V

Output

Reference clock . . . . . 2.048 MHz
(derived form internal reference or from external reference clock [25])

TSE (Test Sequence Error) . . . . . RZ pulses

TX frame trigger (SDH and SONET signal) . . . . . RZ pulses

TX pattern trigger . . . . . RZ pulses
(not for “140 Mbit/s unframed/framed” with digital word)

Input impedance . . . . . 75 Ω

Pulse amplitude . . . . . HCMOS level

Max. permitted peak applied voltage level . . . . . ± 6 V

7.3 REF CLOCK IN [25]

Reference clock input

SDH version 3035/01

Socket . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted peak input voltage . . . . . ± 6 V

Input signal	Line code, pulse shape	Amplitude	Coupling	Max. permitted offset
2.048 Mbit/s	HDB3	2.34 V ± 10%	DC	± 10 ppm
2.048 MHz (clock)	square, sinewave	1 Vpp to 5 Vpp	AC	± 10 ppm
1.544 Mbit/s	B8ZS	2.34 V ± 10%	DC	± 10 ppm
1.544 MHz (clock)	square, sinewave	1 Vpp to 5 Vpp	AC	± 10 ppm

Table S-22 Specifications for reference clock signals

SONET Version BN 3035/02

Socket . . . . . Bantam

Input impedance . . . . . 110 Ω

Max. permitted peak input voltage. . . . . ± 6 V

Input signal	Line code, pulse shape	Amplitude	Coupling	Max. permitted offset
2.048 Mbit/s	HDB3	3.0 V ± 10%	DC	± 10 ppm
2.048 MHz (Clock)	square, sinewave	1 Vpp to 5 Vpp	AC	± 10 ppm
1.544 Mbit/s	B8ZS	3.0 V ± 10%	DC	± 10 ppm
1.544 MHz (Clock)	square, sinewave	1 Vpp to 5 Vpp	AC	± 10 ppm

Table S-23 Specifications for reference clock signals

LTI (Loss of Timing Interval) status display

The LED is on when TX clock generation is set to “Derived from reference clock [25]” and no clock or signal is present. The LED is also on if the clock or signal has a frequency offset of more than 10 ppm (trigger threshold is between 10 and 30 ppm).

7.4 CLOCK [22]

Clock output with unjittered TX clock

Socket . . . . . BNC

Bit rate range . . . . . 1.544 MHz to 155.52 MHz

at STM-4/OC-12, STM-16/OC-48, STM-64/OC-192 . . . . . 155.52 MHz

Output impedance . . . . . approx. 10 Ω

Pulse amplitude . . . . . ≥ 400 mV into 75 Ω, AC coupled

Max. permitted peak applied voltage . . . . . ± 6 V

8 Built-in operation and control computer (PC)

Operating system

ANT-20SE . . . . . Windows 95™

The relevant copyright conditions must be observed.

CPU

The CPU is constantly being updated. The current CPU and hard disk characteristics are displayed after switching on the instrument during the boot-up screen display.

CPU . . . . . 486/DX 4-100 or better
3.3 V technology

Memory

DRAM . . . . . 32 MB, PS/2 module

expandable to . . . . . max. 64 Mbyte

Hard disk . . . . . at least 540 Mbyte

Floppy drive

Disk drive . . . . . 3.5"; 1.44 Mbyte

PCMCIA interface [02]

Controller conforms to . . . . . PCMCIA 2.1

Drive A . . . . . PCMCIA Type I + II + III cards

Drive B . . . . . PCMCIA Type I + II cards

The PCMCIA interface provides access to a wide range of remote-control interfaces:

- IEEE bus remote control, BN 3035/92.10
- For using other PCMCIA cards, “Card and Socket Services” are required. These are included with the remote-control options.

Display

Color TFT screen . . . . . 9.5"; 512 colors

Resolution . . . . . 640 x 480 pixels (standard VGA)

Connector for external display [04]

The built-in and external displays can be operated simultaneously

Interface. . . . . standard VGA

Resolution . . . . . 640 x 480 pixels

Refresh rate. . . . . approx. 60 Hz

Socket . . . . . 15-way 3-row submin. D socket

Keyboard

Built-in

Standard PC keyboard . . . . . US-ASCII

External keyboard connector [03]

The PC configuration must be matched to the type of external keyboard used.

Interface. IBM-AT/PS/2

Connector . . . . . 6-pole Mini-DIN socket

Mouse connector [01]

Interface. . . . . PS/2 mouse interface

Connector . . . . . 6-pole Mini-DIN socket

Parallel interface [05]

Interface. . . . . IEEE 1284

Socket . . . . . 25-way 2-row submin. D socket

Serial interface [06]

Interface. V.24/RS 232

Socket . . . . . 9-way 2-row submin. D socket

Battery

Type. . . . . Lithium
Life time . . . . . >5 years

The battery serves as the buffer for the PC clock's supply voltage and for saving the CMOS setup.

9 General specifications

9.1 Power supply

Nominal voltage (automatic range switching). . . . . 100 to 125 V and 200 to 240 V

Operating range . . . . . 90 to 140 V and 193 to 264 V

AC line frequency . . . . . 50 or 60 Hz ±5%

Power consumption ANT-20SE . . . . . < 600 VA

Safety class to IEC 1010-1. 1

9.2 Climatic and mechanical ambient conditions

	IEC 721-3	**ETS 300 019-1**
Storage	Class IE 12	Class 1.1
Transport	Class IE 23[1]	Class 2.3[1]
Operation	Class IE 72	Class 7.1

1 With temperature range restrictions (see Tab. S-25))

Table S-24 Applicable IEC and ETS classes

9.2.1 Climatic and mechanical data

	Storage: IE 12 (1K3, 1M2) ETS 1.1	**Transport: IE 23 (2K4, 2M3) ETS 2.3**	**Operation: IE 72 (7K1, 7M2) ETS 7.1**
Temperature	-5 to +45 °C	-40 to +70 °C (limited to -25 to +70 °C)	+5 to +40 °C (limits operating range: 0 to +50 °C)
Humidity: < 30 °C Humidity: > 30 °C	5 to 95% 1 to 29 g/m^3	5 to 95% 1 to 29 g/m^3	5 to 85% 1 to 25 g/m^3
Condensation	yes	yes	yes
Precipitation	no	6 mm/min	no
Water	no	1 m/s	no
Ice formation	yes	yes	no
Damp	-	damp loading surface	-
Sinusoidal vibration	9 to 200 Hz: 5 m/s^2	8 to 200 Hz: 20 m/s^2 200 to 500 Hz: 40 m/s^2	9 to 200 Hz: 10 m/s^2 200 to 500 Hz: 15 m/s^2
Shock: 11 ms duration Shock: 6 ms duration	- -	300 m/s^2 1000 m/s^2	100 m/s^2 300 m/s^2
Free drop	-	1.0 m	0.1 m
Toppling	-	all edges	all edges

Table S-25 Major parameters for the classes (see Fig. S-24)

9.3 EC conformance declaration/CE mark

Interference generation . . . . . to EN 50 081-1

Interference immunity . . . . . to EN 50 082-1

9.3.1 EMC interference suppression

Interference suppression

This instrument meets the requirements of EN 50 081-1 and hence limit value class B of EN 55 022 (identical with CISPR 22:1985 modif., DIN VDE 0878 part 3) and FCC Rules Part 15 Subpart J Class A. The instrument conforms to the safety aims of European regulation 89/336/EWG of 03.05.89 in respect of interference suppression. A special permit for operation is not required.

The instrument has been tested such that the requirements in respect of interference suppression for this instrument will also be met if it is operated in a system.

This is conditional upon the correct construction of the system and the use of the specified connecting cables, with particular attention being paid to adequate screening.

If the device under test connected to this instrument is in itself capable of generating interfering radiation, e.g. when the screening to the device under test is not continuous, the user must ensure that any interference generated remains within the prescribed limits. Suitable screening precautions may be additionally required.

Interference suppression corresponds to . . . . . EN 55022/CISPR 22 class B

Intrinsic magnetic scatter field

at AC line frequency and a distance of 30 cm . . . . . < 3 A/m

9.3.2 EMC interference immunity

Tip: Reduced functionality, self-recovering:
During the presence of interference, the signal received by the instrument can be affected to such an extent that an error is detected. This may, for example, be a code error, and depending on the time of occurrence may be a bit, FAS or parity error. Error bursts may lead to alarms.
Such errors and alarms only occur when interference is present.
To keep the effects of interference as small as possible, the system must be correctly constructed using the prescribed cables, with particular attention being paid to adequate screening.
When using standard PC accessories, make sure that these meet the requirements of the EMC regulations (CE mark).

Immunity to electrostatic discharge

to IEC 1000-4-2 or IEC 801 - 2

Reduced functionality (self-recovering) . . . . . up to 4 kV direct contact discharge
or up to 8 kV air path discharge

Immunity to radiated interference

to IEC 1000-4-3 or IEC 801-3

Full functionality . . . . . up to 3 V/m

in the frequency range . . . . . 27 MHz to 1000 MHz
and at 1890 MHz

Rapid transient interference immunity

to IEC 1000-4-4 or IEC 801-4

on signal circuits

Reduced functionality (self-recovering) . . . . . up to 500 V

on AC line circuits

Reduced functionality (self-recovering) . . . . . up to 1kV

External magnetic field immunity

to IEC 1000-4-8

Full functionality . . . . . 3 A/m at 50 or 60 Hz

9.4 Noise emission

A-weighted noise pressure level at 1 m distance . . . . . approx. 48 dB (A)

9.5 Calibration/Maintenance

Recommended confirmation interval . . . . . 2 years

9.6 Dimensions/Weight

Weight
including protective cover . . . . . approx. 15 kg

Dimensions (w x h x d) in mm
including protective cover . . . . . approx. 360 x 370 x 290

9.7 Ordering information

9.7.1 Mainframe ANT-20SE

Advanced Network Tester ANT-20SE
SDH version . . . . . BN 3060/01

One STM-1 mapping is included in the price; select the mapping option you require.

The following options are included:

Touchscreen . . . . . BN 3035/93.11
CPU-RAM-Erweiterung 32 MB . . . . . BN 3035/92.15

Advanced Network Tester ANT-20SE
SONET version . . . . . BN 3060/02

One STS-1 mapping is included in the price; select the mapping option you require.

The following options are included:

Touchscreen . . . . . BN 3035/93.11
CPU-RAM-Erweiterung 32 MB . . . . . BN 3035/92.15

9.7.2 Options

Touchscreen . . . . . BN 3035/93.11
CPU RAM expansion to 32 MB . . . . . BN 3035/93.15

SONET mappings

STS-1 mappings for ANSI tributaries

VT1.5 SPE/STM-0 (1.5 Mbit/s in STS-1) . . . . . BN 3035/90.10
VT6 SPE (6 Mbit/s, unframed in STS-1) . . . . . BN 3035/90.11
STS-1 SPE (45 Mbit/s in STS-1) . . . . . BN 3035/90.12

STS-1 mappings for ETSI tributaries

VT2 SPE/STM-0 (2 Mbit/s in STS-1) . . . . . BN 3035/90.13

DS1 and DS3 interface

Bit error rate tests 1.5 /45 Mbit/s
(included in SONET version 3035/02) . . . . . BN 3035/90.34

STM-1 mappings

for ETSI tributaries

C-12 (2 Mbit/s in STM-1, AU-3/AU-4) . . . . . BN 3035/90.01
C-3 (34 Mbit/s in STM-1, AU-3/AU-4) . . . . . BN 3035/90.02
C-4 (140 Mbit/s in STM-1) . . . . . BN 3035/90.03

for ANSI tributaries

C-11 (1.5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12) . . . . . BN 3035/90.04
C-3 (45 Mbit/s in STM-1, AU-3/AU-4) . . . . . BN 3035/90.05
C-2 (6 Mbit/s, unframed in STM-1, AU-3/AU-4) . . . . . BN 3035/90.06

Extended Overhead Analysis . . . . . BN 3035/90.15

Drop&Insert . . . . . BN 3035/90.20

PDH functions

PDH MUX/DEMUX chain 64k/140M . . . . . BN 3035/90.30
PDH DEMUX chain 64k/140M . . . . . BN 3035/90.31
M13 MUX/DEMUX chain . . . . . BN 3035/90.32
Bit error rate tests 2/8/34/140 Mbit/s
(included in SDH version 3035/01) . . . . . BN 3035/90.33

Optical interfaces

Optical STM-1, OC-1/3, 1310 nm . . . . . BN 3035/90.43
Optical STM-1, OC-1/3, 1550 nm . . . . . BN 3035/90.44
Optical STM-1, OC-1/3, 1310 and 1550 nm . . . . . BN 3035/90.45

Optical STM-1/4, OC-1/3/12, 1310 nm . . . . . BN 3035/90.46
Optical STM-1/4, OC-1/3/12, 1550 nm . . . . . BN 3035/90.47
Optical STM-1/4, OC-1/3/12, 1310 and 1550 nm . . . . BN 3035/90.48

STM-16/OC-48 1550 nm . . . . . BN 3035/90.53
STM-16/OC-48 1310 nm . . . . . BN 3035/90.54
STM-16/OC-48 1310 and 1550 nm . . . . . BN 3035/90.59

STM-64/OC-192 1550 nm Generator/Analyzer . . . . . BN 3035/91.40
STM-64/OC-192 1550 nm Generator . . . . . BN 3035/91.41
STM-64/OC-192 1550 nm Analyzer . . . . . BN 3035/91.42

Optical power splitter (90/10%) . . . . . BN 3035/90.49

Optical Attenuator (plug in)
SC-PC, 1310 nm, 15 dB . . . . . BN 3035/90.61

OC-12c/STM-4c Options

OC-12c/STM-4c Bit Error Tester
(requires Optical Module BN 3035/90.46, 90.47 or 90.48) . . . . . BN 3035/90.90
OC-12c/STM-4c ATM Testing
(requires Optical Module BN 3035/90.46, 90.47 or 90.48 and
ATM-Modul BN 3035/90.70) . . . . . BN 3035/90.91
OC-12c/STM-4c Virtual Concatenation
(requires Optical Module BN 3035/90.90 oder 90.91;
the optiones BN 3035/90.38, 91.53, 91.54, 91.59 are alternatives) . . . . BN 3035/90.92
Optical STM-16/OC-48, 15... nm
(Select a wavelength between 1530,33 nm and
1560,61 nm to G.692.) . . . . . BN 3035/90.38
OC-48c/STM-16c Bit Error Tester (Bulk)
(requires Optical Module BN 3035/90.46, 90.47 or 90.48) . . . . . BN 3035/90.93

Optical test adapters

ST Type (AT&T) . . . . . BN 2060/00.32
HMS-10/A, HFS-13/A (Diamond) . . . . . BN 2060/00.34
HMS-10, HFS-13 (Diamond) . . . . . BN 2060/00.35
“KEYED BICONIC”, with anti-twist device (AT&T) . . . . . BN 2060/00.37
D4 (NEC) . . . . . BN 2060/00.40
DIN 47256 . . . . . BN 2060/00.50
FC, FC-PC (NTT) . . . . . BN 2060/00.51
SC, SC-PC (NTT) . . . . . BN 2060/00.58
E 2000 (Diamond) . . . . . BN 2060/00.61

Wavetek Wandel Goltermann can supply a wide selection of optical power level meters, sources, attenuators and accessories. Please ask your local sales office for information.

O.172 Jitter and wander

O.172 Jitter Generator up to 155 Mbit/s . . . . BN 3035/90.81
O.172 Jitter Meter up to 155 Mbit/s . . . . BN 3035/90.82
O.172 Jitter Generator 622 Mbit/s
(requires BN 3035/90.81) . . . . BN 3035/90.83
O.172 Jitter Meter 622 Mbit/s
(requires BN 3035/90.82) . . . . BN 3035/90.84
O.172 Wander Generator up to 622 Mbit/s
(requires BN 3035/90.81 for up to 155 Mbit/s and 90.83 for 622 Mbit/s) . . . . BN 3035/90.85
O.172 Wander Analysator up to 622 Mbit/s
(requires BN 3035/90.82 for up to 155 Mbit/s and 90.84 for 622 Mbit/s) . . . . BN 3035/90.86
O.172 Wander Generator 2488 Mbit/s
(requires ANT-20E and BN 3035/90.81 and BN 3035/90.88) . . . . BN 3035/90.87
O.172 Jitter Generator/Analysator 2488 Mbit/s
(requires ANT-20E) . . . . BN 3035/90.88
O.172 Wander Analysator 2488 Mbit/s
(requires ANT-20E and BN 3035/90.88) . . . . BN 3035/90.89
O.172 MTIE/TDEV Analysis
(requires BN 3035/90.86 for up to 622 Mbit/s
and BN 3035/90.89 for 2488 Mbits/s) . . . . BN 3035/95.21

ATM functions

ATM module
Includes ATM mapping STM-1/STS-3c . . . . BN 3035/90.70

ATM Broadband Analyzer/Generator. . . . . BN 3035/90.80

Additional ATM-Mappings

requires ATM-Module 3035/90.70 or BN 3035/90.80

STS-1 (51 Mbit/s) . . . . BN 3035/90.71
E4 (140 Mbit/s)[1]. . . . . BN 3035/90.72
DS3 (45 Mbit/s)[2] . . . . BN 3035/90.73
E3 (34 Mbit/s)[1]. . . . . BN 3035/90.74
E1 (2 Mbit/s)[1]. . . . . BN 3035/90.75
DS1 (1,5 Mbit/s)[2] . . . . BN 3035/90.76
VC-3 in STM-1 (AU-3/AU-4) . . . . BN 3035/90.77

1 For SONET versions BN 3035/42, BN 3035/22 and BN 3038/12, option BN 3035/90.33 is required.
2 For SDH versions BN 3035/41, BN 3035/21 and BN 3038/11, option BN 3035/90.34 is required.

9.7.3 Remote control

V.24 remote control . . . . BN 3035/91.01

GPIB remote control . . . . BN 3035/92.10

LabWindows/CVI Driver . . . . BN 3038/95.99

9.7.4 Remote operation

Remote operation via modem . . . . . .BN 3035/95.30

Remote operation via LAN (TCP/IP) . . . . . .BN 3035/95.31

9.7.5 Test automation

CATS Test Sequencer and test case library. . . . . .BN 3035/95.90

9.7.6 Calibration

Calibration report . . . . . .BN 3035/94.01

9.7.7 Accessories

Included with instrument

- Filter pads
- AC line cord
- 2 cables
- Operating manual

Optional accessories

Carry bag for ANT-20SE . . . . . .BN 3035/92.02

External keyboard (US/English) . . . . . .BN 3035/92.04

Decoupler, -20 dB, m-f 1.6/5.6 . . . . . BN 3903/63

TKD-1 probe, 48 to 8500 kbit/s . . . . . BN 882/01

WG PenBERT Mini-PCM-Monitor (E1). . . . . BN 4555/11

9.7.8 Retrofitting of options

All options can be retrofitted by the Wavetek Wandel Goltermann worldwide service network.

9.7.9 Note for ANT-20SE users

The following hardware and software bundles have been formed for the ANT-20SE.

Assignments of modules and software ANT-20SE – ANT-20/ANT-20E:

	Module / Software	BN number ANT-20SE	Equivalent BN number
ANT-20SE Mainframe	Mainframe, SDH	3060/01	3035/41 or 3035/21 + 3035/92.15 + 3035/93.11 + 3035/90.01
	Mainframe, SONET	3060/02	3035/42 or 3035/22 + 3035/92.15 + 3035/93.11 + 3035/90.10
	Extended SDH Testing	3060/90.01	3035/90.02, 3035/90.03, 3035/90.04, 3035/90.05, 3035/90.06, 3035/90.15
	Extended SONET Testing	3060/90.02	3035/90.11, 3035/90.12, 3035/90.13, 3035/90.03, 3035/90.15
	Add SONET (SONET expansion for SDH mainframe)	3060/90.03	3035/90.10, 3035/90.11, 3035/90.12, 3035/90.13, 3035/90.34
	Add SDH (SDH expansion for SONET mainframe)	3060/90.04	3035/90.01, 3035/90.02, 3035/90.04, 3035/90.05, 3035/90.06, 3035/90.33
	Drop&Insert (Through mode, Block&Replace)	3060/90.10	3035/90.20
	PDH MUX/DEMUX (64/140)	3060/90.11	3035/90.30
	M13 MUX/DEMUX	3060/90.12	3035/90.32
Optics STM-1/4, OC-1/3/12	STM-1, OC-1/3 1310 nm	3060/91.01	3035/90.43 + 2 Adapters
	STM-1, OC-1/3 1310 nm & 1550 nm	3060/91.02	3035/90.45 + 2 Adapters
	STM-1/4, OC-1/3/12 1310 nm	3060/91.11	3035/90.46 + 2 Adapters
	STM-1/4, OC-1/3/12 1310 nm & 1550 nm	3060/91.12	3035/90.48 + 2 Adapters
	Optical power splitter	3060/91.05	3035/90.49 + 3 Adapters
	OC-12c BULK	3060/90.90	3035/90.90
	OC-12c Virtual concatenation	3060/90.92	3035/90.92

Table S-26 Assignments of modules and software

	Module / Software	BN number ANT-20SE	Equivalent BN number
Optics STM-16, OC-48	STM-16, OC-48 1550 nm	3060/91.50	3035/91.53 + 2 Adapters
	STM-16, OC-48 1310 nm	3060/91.51	3035/91.54 + 2 Adapters
	STM-16, OC-48 1310 nm & 1550 nm	3060/91.52	3035/91.59 + 2 Adapters
	STM-16, OC-48 15... nm, special	3060/91.53	3035/90.38 + 2 Adapters
	OC-48c BULK	3060/90.93	3035/90.93
	Package: STM-0/1/4/16 1310 nm + Concatenation	3060/90.55	3035/90.46, 3035/91.54, 3035/90.90, 3035/90.93, + 4 Adapters
	Package: STM-0/1/4/16 1550 nm + Concatenation	3060/90.56	3035/90.47, 3035/91.53, 3035/90.90, 3035/90.93, + 4 Adapters
	Package: STM-0/1/4/16 1310 nm & 1550 nm + Concatenation	3060/90.57	3035/90.48, 3035/91.59, 3035/90.90, 3035/90.93, + 4 Adapters
	Package: STM-0/1/4 1310 nm STM-16 1550 nm + Concatenation	3060/90.58	3035/90.46, 3035/91.53, 3035/90.90, 3035/90.93, + 4 Adapters
Jitter O.172	Package: O.172 Jitter/Wander up to 155 Mbit/s	3060/91.30	3035/90.81, 3035/90.85, 3035/90.82, 3035/90.86
	Package: O.172 Jitter/Wander up to 622 Mbit/s	3060/91.31	3035/91.31
	Package: O.172 Jitter/Wander up to 2488 Mbit/s	3060/91.32	3035/91.32
	MTIE/TDEV Analysis Part of 3060/91.30 to 91.32	-	3035/95.21
ATM	ATM Basic	3060/90.50	3035/90.70
	ATM Comprehensive	3060/90.51	3035/91.80
	Add ATM SDH	3060/90.52	3035/90.72, 3035/90.74, 3035/90.75, 3035/90.77, 3035/90.33
	Add ATM SONET	3060/90.53	3035/90.71, 3035/90.73, 3035/90.76, 3035/90.34,
	OC-12c ATM Testing	3060/90.91	3035/90.91
Accessories	Remote control, V.24	3035/91.01	
	Remote control, GPIB	3035/92.10	
	Remote Operation Modem	3035/95.30	
	Remote Operation LAN/PCMCIA	3035/95.31	
	PDH/SDH NEXT Expert	3035/95.40	
	Test Sequencer	3035/95.90	
	LabWindows/CVI drivers	3035/95.99	
	Calibration report	3035/94.01	
	Transport case	3035/92.03	

Table S-26 Assignments of modules and software *(continued)*

Notes:

ANT-20SE
Advanced Network Tester

Extended Overhead Analysis STM-1 Mappings

BN 3060/90.01

Extended Overhead Analysis STS-1 Mappings

BN 3060/90.02

Drop&Insert

BN 3060/90.10
in combination with
STM-1/STS-1 Mappings

Software Version 7.20

Specifications

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications Extended Overhead Analysis

Specifications STM-1 Mappings

Specifications STS-1 Mappings

Specifications Extended Overhead Analysis

1 Overhead Capture

Function

The Capture function is used to record one byte of the SOH/TOH (or two bytes simultaneously when recording K1, K2) or one byte of the low/high path POH.

Capture bytes

STS-1,STM-0,STM-1,STS3,STS3c . . . . . all SOH/TOH/POH bytes
STM-4, STM-16[1] . . . . . all SOH #1 bytes
except A1, A2, B1
all POH bytes

OC-12, OC-48[1] . . . . . all TOH #1 bytes
except A1, A2, B1
all POH bytes

Buffer length . . . . . 265 bytes for single byte recording
200 bytes for double byte recording
Triggering . . . . . recording starts manually or
when trigger condition occurs

1 STM-16, OC-48: ANT-20SE

Trigger events

Alarms . . . . . .MS-AIS (AIS-L),
AU-AIS (AIS-P),
MS-RDI (RDI-L)
AU-LOP (LOP-P)
Compare/Compare not . . . . . occurrence of a certain value in the capture byte or
non-occurrence of this value
(don't care values also possible)
N1/N2 - TCM (N1/Z6 - TCM) . . . . . all bytes including the detected FAS bytes are
recorded when the TCM FAS word is detected

Resolution . . . . . frame
Time display . . . . . frame number,
hh:mm:ss.ms
Maximum recording time . . . . . 99 h
Result display . . . . . number, frames since trigger,
time elapsed since trigger,
byte value in hexadecimal,
binary and ASCII codes,
plain text for K1, K2 (APS)

2 APS switching time measurement

Sensor selection . . . . . MS-AIS, AU-AIS, TU-AIS, TSE, AIS-L, AIS-P, AIS-V
Resolution . . . . . 1 ms
Measurement error . . . . . (see Tab. S-1)
Minimum detectable switching time . . . . . 125 µs
Maximum measurable switching time . . . . . 2 s
Maximum permitted base BER for TSE sensor 2 E-4

Hierarchy	**Sensor**	**Maximum error**
SDH	MS-AIS, AU-AIS, TU-AIS	± 1 ms
SONET	AIS-L, AIS-P, AIS-V	± 1 ms
PDH unframed	BE	± 2 ms
PDH framed	TSE	± 2 ms + T_{sync} [1]
DSn unframed	TSE	± 2 ms
DSn framed	TSE	± 2 ms + T_{sync} [1]

1 T_{sync} is the frame synchronization time included in the measurement

Table S-1 Maximum measurement error

Hierarchy	**T_{sync} (typ.)**
E4 (140 Mbit/s)	0.1 ms
E3 (34 Mbit/s)	0.1 ms
E2 (8 Mbit/s)	1 ms
E1 (2 Mbit/s)	2 ms
DS3 (45 Mbit/s)	6 ms
DS1 SF (1.5 Mbit/s)	3 ms
DS1 ESF (1.5 Mbit/s)	6 ms

Table S-2 Typical values of T_{sync}

Specifications STM-1 Mappings

These specifications apply to the options:

STM-1 Mapping

for ETSI tributaries

C-12 (2 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.01
C-3 (34 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.02
C-4 (140 Mbit/s in STM-1) . . . . . .BN 3035/90.03
C-2 (6 Mbit/s, unframed, in STM-1, AU-3/AU-4). . . . . .BN 3035/90.06

for ANSI tributaries

C-11 (1,5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12) . . . . . .BN 3035/90.04
C-3 (45 Mbit/s in STM-1, AU-3/AU-4). . . . . .BN 3035/90.05

Drop & Insert . . . . . .BN 3035/90.20

1 STM-1 Mapping

1.1 General information

Mapping/Demapping

The PDH tributaries are mapped into a STM-1 signal via the AU-4 or the AU-3 layer.

Container contents for all mapping options:

- Framed or unframed PDH test signal in one selected container
  (6 Mbit/s, unframed only)
- PDH multiplex signal in one selected container
  (together with Mux/Demux Chain 64k/140M or M13 option)
- Filling one selected container with a test pattern without justification bits
  (Bulk Signal to O.181)

Drop & Insert

An additional Drop & Insert Option (BN 3035/90.20) for dropping or inserting tributary signals (via sockets) is available in conjunction with the mapping options.

1.2 Tributary channel numbering

TU-3	TU-2	TU-12	TU-11	TS #
100	110	111	111	1
		112	112	22
		113	113	43
			114	64
	120	121	121	4
		122	122	25
		123	123	46
			124	67
	130	131	131	7
		132	132	28
		133	133	49
			134	70
	140	141	141	10
		142	142	31
		143	143	52
			144	73
	150	151	151	13
		152	152	34
		153	153	55
			154	76
	160	161	161	16
		162	162	37
		163	163	58
			164	79
	170	171	171	19
		172	172	40
		173	173	61
			174	82

TU-3	TU-2	TU-12	TU-11	TS #
200	210	211	211	2
		212	212	23
		213	213	44
			214	65
	220	221	221	5
		222	222	26
		223	223	47
			224	68
	230	231	231	8
		232	232	29
		233	233	50
			234	71
	240	241	241	11
		242	242	32
		243	243	53
			244	74
	250	251	251	14
		252	252	35
		253	253	56
			254	77
	260	261	261	17
		262	262	38
		263	263	59
			264	80
	270	271	271	20
		272	272	41
		273	273	62
			274	83

TU-3	TU-2	TU-12	TU-11	TS #
300	310	311	311	3
		312	312	24
		313	313	45
			314	66
	320	321	321	6
		322	322	27
		323	323	48
			324	69
	330	331	331	9
		332	332	30
		333	333	51
			334	72
	340	341	341	12
		342	342	33
		343	343	54
			344	75
	350	351	351	15
		352	352	36
		353	353	57
			354	78
	360	361	361	18
		362	362	39
		363	363	60
			364	81
	370	371	371	21
		372	372	42
		373	373	63
			374	84

Table S-3 Channel numbers to G.707 (relationship between TU and time slot TS #)

1.3 Scrambling/Descrambling

The STS-N signal is scrambled/descrambled as described in ITU-T G.707.

1.4 Overhead generation

1.4.1 Section Overhead (SOH)

Standard Overhead, STM-1 (hex)

SOH										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	
1	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	J0 01	— AA	— AA	
2	B1 XX	— 00	— 00	E1 00	— 00	— 00	F1 00	— 00	— 00	
3	D1 00	— 00	— 00	D2 00	— 00	— 00	D3 00	— 00	— 00	
4a	H1 68	Y 9B	Y 9B	H2 00	— FF	— FF	H3 00	H3 00	H3 00	for AU-4
4b	H1 68	H1 68	H1 68	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	for AU-3
5	B2 XX	B2 XX	B2 XX	K1 00	— 00	— 00	K2 00	— 00	— 00	
6	D4 00	— 00	— 00	D5 00	— 00	— 00	D6 00	— 00	— 00	
7	D7 00	— 00	— 00	D8 00	— 00	— 00	D9 00	— 00	— 00	
8	D10 00	— 00	— 00	D11 00	— 00	— 00	D12 00	— 00	— 00	
9	S1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	E2 00	— 00	— 00	

Table S-4 SOH contents

XX: Inserted by parity formation (B1, B2)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown), H3 depends on whether or not a pointer action takes place.

SOH byte contents

- Static bytes: all except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: all except B1, B2, H1, H2, H3
- Trace Identifier (Length = 16 frames with CRC7 formation): J0
- Dynamic bytes filled using PRBS 11: E1, F1, E2
- Dynamic byte groups filled using PRBS 11: D1 to D3, D4 to D12
- Dynamic bytes filled via DCC/ECC interface (V.11): E1, F1, E2
- Dynamic byte groups filled via DCC/ECC interface (V.11): D1 to D3, D4 to D12, K1 to K2

1.4.2 STM-1 error insertion (anomalies)

Error insertion (anomalies) . . . . . B1, B2, B3 parity errors, FAS word errors, MS-REI, HP-REI, bit errors in test pattern (TSE), code errors (single errors only)

Trigger types . . . . . Single or Rate

When Rate triggering is selected a bit error rate is inserted.

Anomaly	**Single**	**Rate[1]**	**Burst m, n (frames)**
FAS	yes	2E-3 to 1E-10	m = 1 to 196000
B1	yes	2E-4 to 1E-10	m = 1 to 196000
B2	yes	2E-3 to 1E-10	m = 1 to 196000
MS-REI	yes	2E-3 to 1E-10	m = 1 to 196000
B3[2]	yes	2E-4 to 1E-10	m = 1 to 196000
HP-REI	yes	2E-4 to 1E-10	m = 1 to 196000
TSE	yes	1E-2 to 1E-8	-
CODE	yes	-	-

1 Mantissa: 1 to 9 (only 1 for TSE), exponent: -1 to -10 (whole numbers)
2 Static error insertion, can be edited using an 8-bit mask (x = don't care, 1 = insert error)

Table S-5 Available anomalies (STM-1) and trigger modes

The insertion of **errors** (anomalies) **and alarms** (defects) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.3 STM-1 alarm generation (defects)

Defect	Test sensor function	Test sensor thresholds	
	On/Off	M in N	|----t1----| |------t2------|
LOS[1]	yes	M = 800 bis 7200 N = 1600 bis 8000	t1 = 0.1 bis 60.0 s t2 = 0.2 bis 600 s
LOF	yes	M = 1 to N - 1 N = 1 to 8000[2]	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RS-TIM	yes	-	-
MS-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
MS-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-UNEQ	yes	M = 1N to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-PLM	yes	M = 1N to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
HP-TIM	yes	-	-

1 Only in conjunction with an optical interface
2 Included in mainframe (no option required)

Table S-6 Available defects (STM-1)

The insertion of **alarms** (defects) **and errors** (anomalies) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.4 Pointer action generation

Stimulation

Pointer sequences

On all pointer levels to ITU-T G.783

T1, T4: 0.25 ms to 600 s . . . . . (2 to 4800000 frames)

T2, T3: 0.25 ms to 10 s . . . . . (2 to 80000 frames)

T5: 0 ms to 600 s. . . . . (0 to 4800000 frames)

n: 1 to 2000

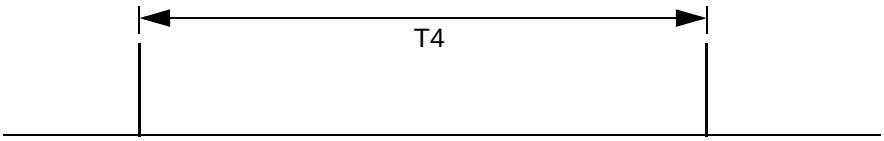


Fig. S-1 Perodic (single/multiple) pointers with identical polarity

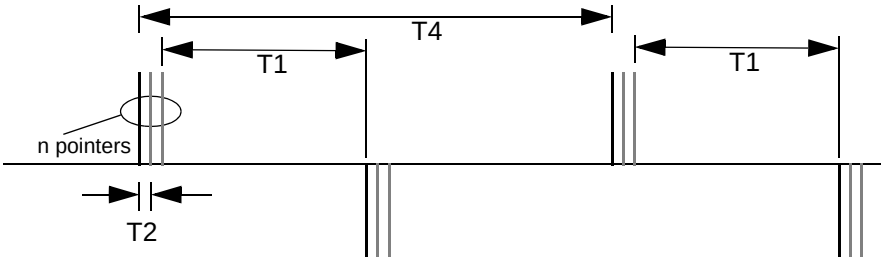


Fig. S-2 Periodic (single/multiple) pointers with different polarity

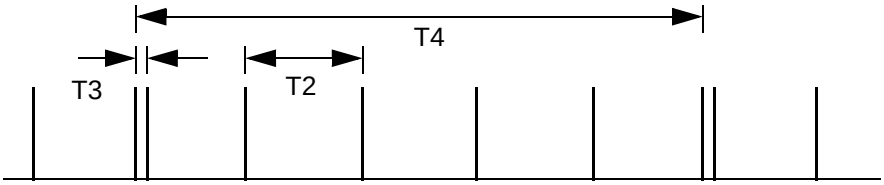


Fig. S-3 Periodic pointers with one double pointer

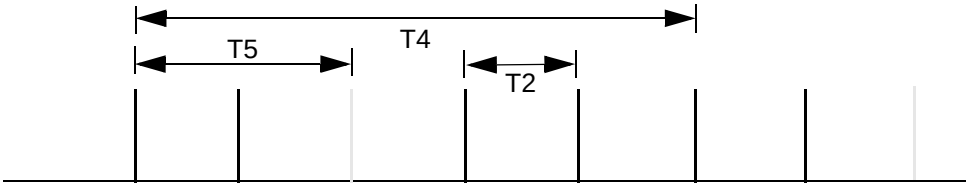


Fig. S-4 Periodic pointers with one missing pointer

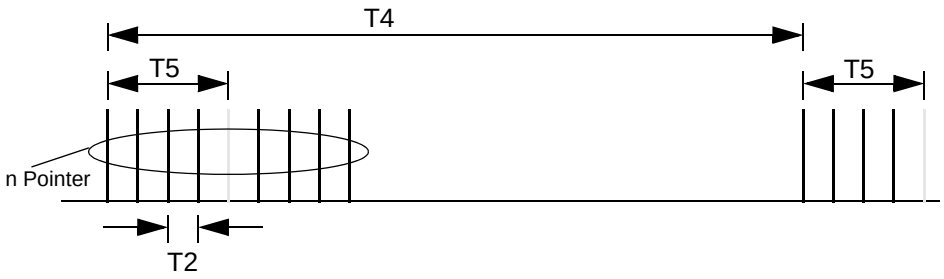


Fig. S-5 Pointer burst with missing pointers

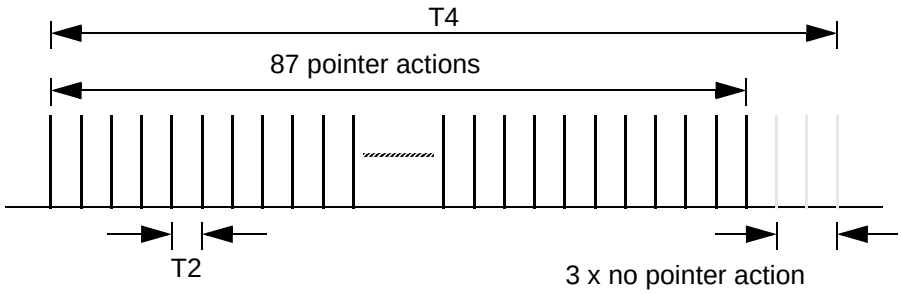


Fig. S-6 ”87-3” sequence

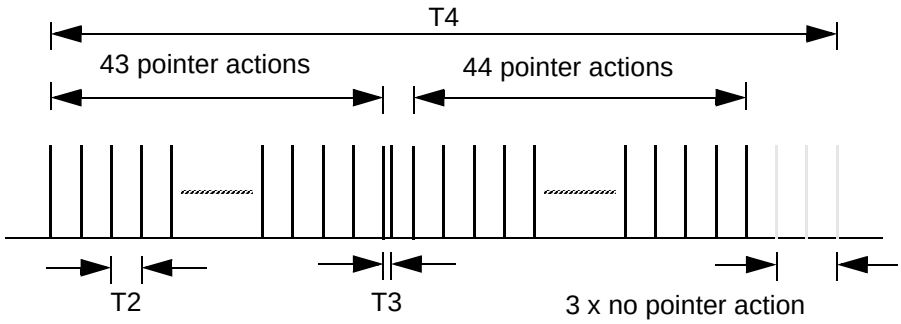


Fig. S-7 ”43-44” sequence with double pointer

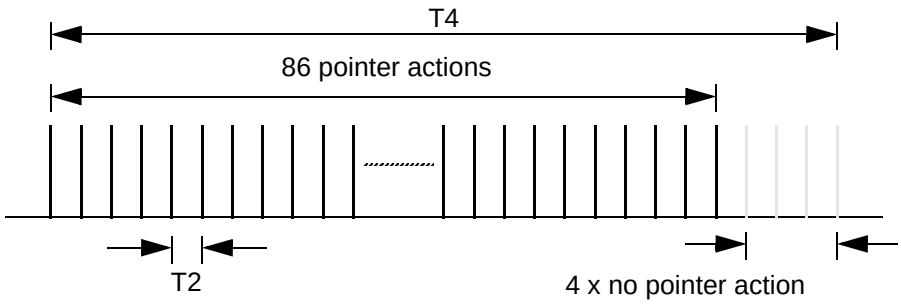


Fig. S-8 ”86-4” sequence with missing pointer

Pointer jumps

Pointer jump from pointer value A to pointer value B (also setting a new pointer).

Pointer jumps are executed with NDF.
Pointer range A + B:

AU-4/AU-3 pointer	0 to 782
TU-3 pointer	0 to 764
TU-2 pointer	0 to 427
TU-12 pointer	0 to 139
TU-11 pointer	0 to 103

1.4.5 STM-1 error measurements (anomalies)

Evaluation

All errors (anomalies) are counted simultaneously and stored.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

of anomalies via LEDs:

CURRENT LED (red) is on when the anomaly is present

HISTORY LED (yellow) is on if the anomaly has occurred at least once during the current measurement interval.

Display of errors as count or ratio values (equivalent bit error ratio): When calculating the ratio value, correction formulae are used for the anomalies B1, B2, B3 and BIP-2 as well as MS-REI, HP-REI and LP-REI. These take into account that a multiple error in the same bit can lead to clearance of the error.

Anomaly	**LED**
OOF -155	LOF/OOF
FAS-155	-
B1	B1/B2
B2	B1/B2
MS-REI	-
B3	B3
HP-REI	-
CRC-4	FAS/CRC
E-Bit	-
TSE	TSE
CODE	-

Table S-7 LED display of possible anomalies (STM-1)

1.4.6 STM-1 alarm detection (defects)

Evaluation

All alarms (defects) which occur are evaluated simultaneously where possible and stored. Storage takes place only within a started measurement interval.

Time resolution of defects . . . . . 100 ms

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present

HISTORY LED (yellow) is on if the defect has occurred at least once during the current measurement interval.

Defect	**LED**
LOS	LOS
LOF-155	LOF/OOF
RS-TIM	-
MS-AIS	MS-AIS
MS-RDI	MS-RDI
AU-LOP	AU-LOP
AU-AIS	AU-AIS
HP-UNEQ	HP-UNEQ
HP-PLM	HP-PLM
HP-RDI	HP-RDI
HP-TIM	-
LSS	LSS

Table S-8 LED display of possible defects (STM-1)

1.4.7 Measurement of AU and TU pointer actions

Evaluation

All pointers in the selected path are shown as absolute values and the direction and number of pointer movements is detected and counted.

NDF (New Data Flag) is recorded and counted.

Display

of:

- Number of pointer operationsseparated for AU and TU pointer:
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address
- Number of NDF events
- Corresponding clock deviation
- AU-NDF and TU-NDF can be indicated by the LED display (front panel)
  (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP”
  – the “TU-LOP/LOP-V” LED indicates “TU-NDF” in addition to “TU-LOP”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are displayed as a histogram with selectable time resolution in seconds, minutes, hours or days.

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are printed out as a table with 1 second time resolution.

1.4.8 VC-4 Path Overhead (POH), High Order

Standard overhead

POH byte	Option 3035/90.01, Option 3035/90.04, Option 3035/90.06	Option 3035/90.02 and Option 3035/90.05	Option 3035/90.03
J1 (ASCII)	“WG HP-TRACE”		“VC-4 MAPPING” “VC-4 BULK”
B3 (hex)	Inserted by parity formation		
C2 (hex)	“02”	“04”	“12” for MAPPING “FE” for BULK
G1 (hex)	“00”		
F2 (hex)	“00”		
H4 (hex)	“FC”, ”FD”, ”FE”, ”FF” sequence across 4 frames	“FF”	
	48-byte-sequence as G.709		
F3 (hex)	“00”		
K3 (hex)	“00”		
N1 (hex)	“00”		

Table S-9 POH contents

VC-4 POH byte contents

- Static bytes: all except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using PRBS 11: F2
- Dynamic bytes filled via DCC/ECC interface (V.11): F2, K3, N1
- H4 sequence, switchable, 4/48 byte

1.4.9 VC-3 Path Overhead (POH), High Order

Standard overhead

POH byte	Option 3035/90.01, Option 3035/90.04 and Option 3035/90.06		Option 3035/90.02 and Option 3035/90.05	
	Measured channels	**Fill channels**	**Measured channels**	**Fill channels**
J1 (ASCII)	“WG HP-TRACE”	“WG IDLE”	“VC-3 Mapping” “VC-3 Bulk”	“WG IDLE”
B3 (hex)	Inserted by parity formation			
C2 (hex)	“02”	“02”	“04” for mapping “FE” for bulk	“04”
G1 (hex)	“00”			
F2 (hex)	“00”			
H4 (hex)	“FC”, “FD”, “FE”, “FF” sequence across 4 frames		“FF”	
	48-byte-sequence asG.709			
F3 (hex)	“00”			
K3 (hex)	“00”			
N1 (hex)	“00”			

Table S-10 POH contents

VC-3 POH byte contents

- Static bytes: all except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using a pseudo-random sequence: F2
- Dynamic bytes filled by DCC/ECC interface (V.11): F2, K3, N1
- H4 sequence, switchable, 4/48 byte

1.4.10 Evaluation of Section Overhead (SOH) and VC-4/VC-3 Path Overhead (POH)

Display

of complete SOH and POH . . . . . hexadecimal
of Trace Identifier J0, J1 . . . . . ASCII, plain text

Evaluation

Bit error measurement

using PRBS 11 (bytes). E1, F1, E2, F2
using PRBS 11 (byte groups) . . . . . D1 to D3, D4 to D12

Output

as bytes via DCC/ECC interface (V.11) E1, F1, E2, F2, K3, N1
as byte groups via DCC/ECC interface (V.11). . . . . D1 to D3, D4 to D12, K1 to K2

1.5 C-12 mapping (2 Mbit/s in STM-1, AU-3/AU-4)

Option: BN 3035/90.01

Mapping structure: AU-4

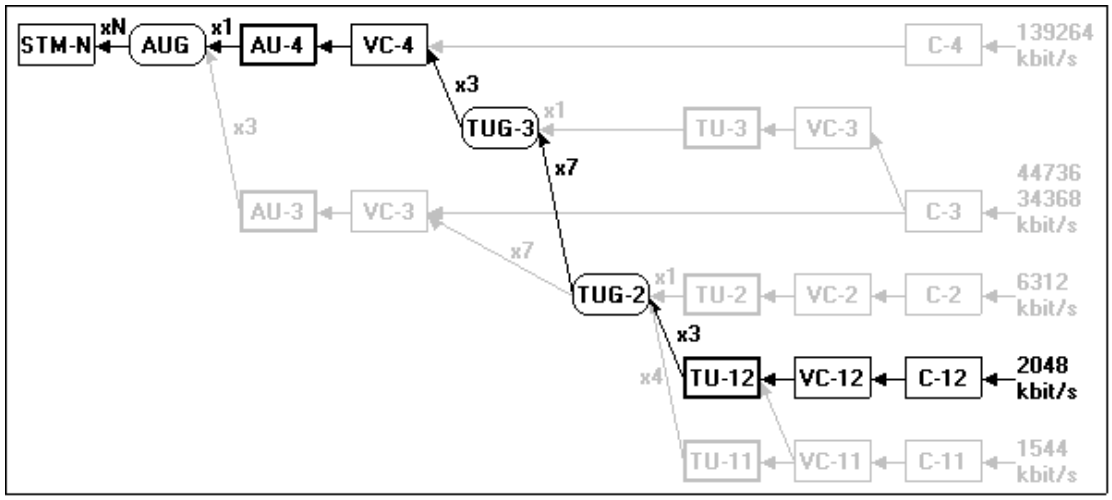


Fig. S-9 Mapping structure: 2 Mbit/s → C-12 → AU-4 → STM-1

Mapping structure: AU-3

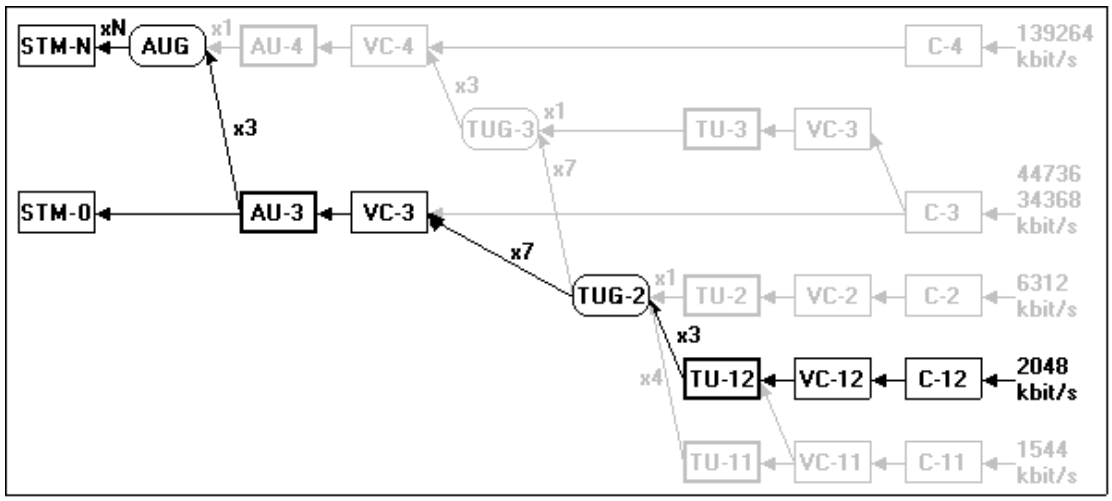


Fig. S-10 Mapping structure: 2 Mbit/s → C-12 → AU-3 → STM-1
Mapping structure: 2 Mbit/s → C-12 → AU-3 → STM-0; option 3035/98.13 required

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating)

1.5.1 VC-12 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “110” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-11 VC-12 POH (Standard Overhead) contents

Measurement channel byte contents (VC-12)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier (Length = 16 frames with CRC7 formation): J2
- Dynamic bytes filled by DCC/ECC interface (V.11): N2

Filler channel byte contents (VC-12)

Fixed, non-editable as in (see Tab. S-11).

1.5.2 VC-12 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-6:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-12 Additional available anomalies (VC-12)

Error insertion refers to the selected measurement channel.

1.5.3 VC-12 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-7:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-13 Addition available defects (VC-12)

Alarm generation refers to the selected measurement channel.

1.5.4 VC-12 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-11:

Anomaly	**LED**
LP-BIP	LP-BIP
LP-REI	-

Table S-14 LED display of additional anomalies (VC-12)

Evaluation and display refer to the selected measurement channel.

1.5.5 VC-12 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-12:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-15 LED display of additional alarms (VC-12)

Evaluation and display refer to the selected measurement channel.

1.5.6 VC-12 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.6 C-3 mapping (34/45 Mbit/s in STM-1, AU-3/AU-4)

Option: BN 3035/90.02 for 34 Mbit/s
Option: BN 3035/90.05 for 45 Mbit/s

Mapping structure: AU-4

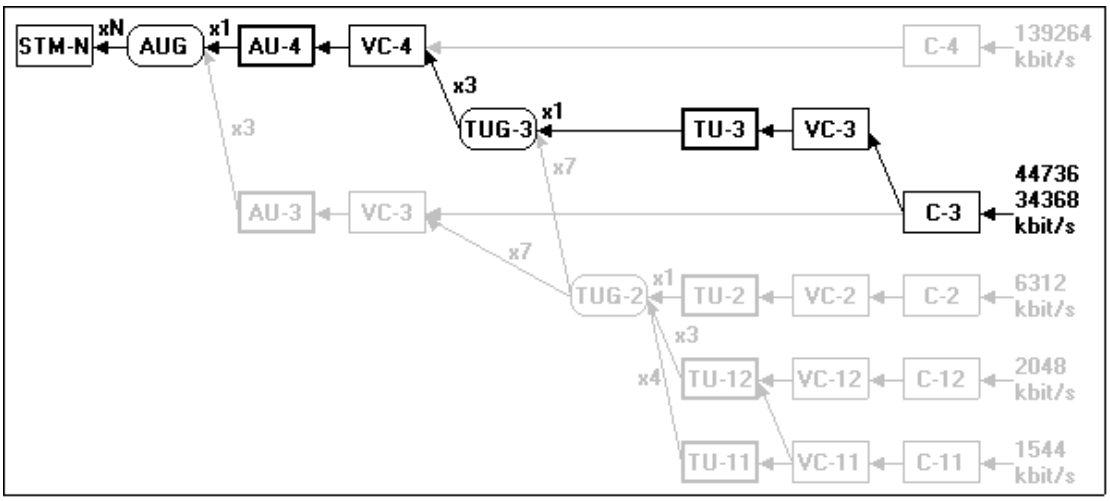


Fig. S-11 Mapping structure: 34/45 Mbit/s → C-3 → AU-4 → STM-1

Mapping structure: AU-3

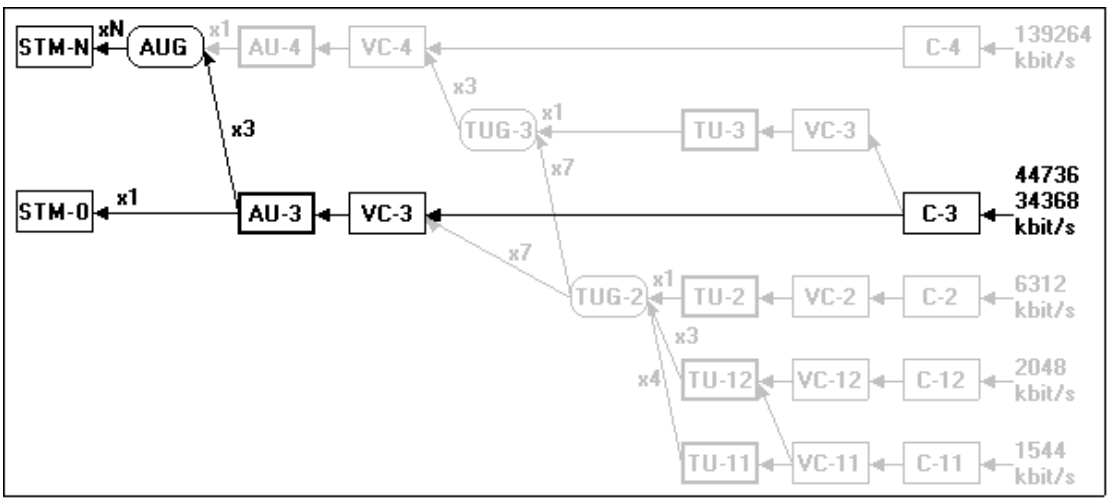


Fig. S-12 Mapping structure: 34/45 Mbit/s → C-3 → AU-3 → STM-1
Mapping structure: 34/45 Mbit/s → C-3 → AU-3 → STM-0;
option 3035/90.12 required

1.6.1 VC-3 Path Overhead contents (Low Order)

POH byte	Measurement channel	Filler channels
J1 (ASCII)	“WG TRACE”	“WG IDLE”
B3 (hex)	Inserted by parity formation	
C2 (hex)	“04” for mapping signal “FE” for bulk signal	“04”
G1 (hex)	“00”	
F2 (hex)	“00”	
H4 (hex)	”FF”	
Z3 (hex)	“00”	
K3 (hex)	“00”	
N1 (hex)	“00”	

Table S-16 VC-3 POH (Standard Overhead) contents

Test channel byte contents (VC-3)

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, K3, N1
- Trace Identifier (Length = 16 frames with CRC7 formation): J1
- Dynamic byte filled using pseudo-random bit sequence: F2
- Dynamic bytes via V.11 interface (V.11): F2, K3, N1

Filler channel byte contents

Fixed, non-editable (see Tab. S-16).

1.6.2 VC-3 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-6:

Anomaly	Single	Rate
LP-B3[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 8-bit mask (x = don’t care, 1 = insert error)

Table S-17 Additional available anomalies (VC-3)

Error insertion refers to the selected measurement channel.

1.6.3 VC-3 alarm generation (defects)

The following defects can be inserted in addition to the defects specified in Sec. 1.4.3, Page S-7:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-

Table S-18 Additional available defects (VC-3)

Alarm generation refers to the selected measurement channel.

1.6.4 VC-3 error measurement (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-11:

Anomaly	**LED**
LP-B3	LP-BIP
LP-REI	-

Table S-19 LED display of additional anomalies (VC-3)

Evaluation and display refer to the selected measurement channel.

1.6.5 VC-3 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-12:

Defect	LED
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-

Table S-20 LED display of additional defects (VC-3)

Evaluation and display refer to the selected measurement channel.

1.6.6 VC-3 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J1

Output

- Bit error measurement using PRBS 11: F2 (byte)
- Byte output via DCC/ECC interface (V.11): F2, K3, N1

1.7 C-4 mapping (140 Mbit/s in STM-1/STS-3c)

Option BN 3035/90.03

STS-3c see also
Operating Manual “STS-1 mappings”, section “STS-3c SPE mappings”.

Mapping structure

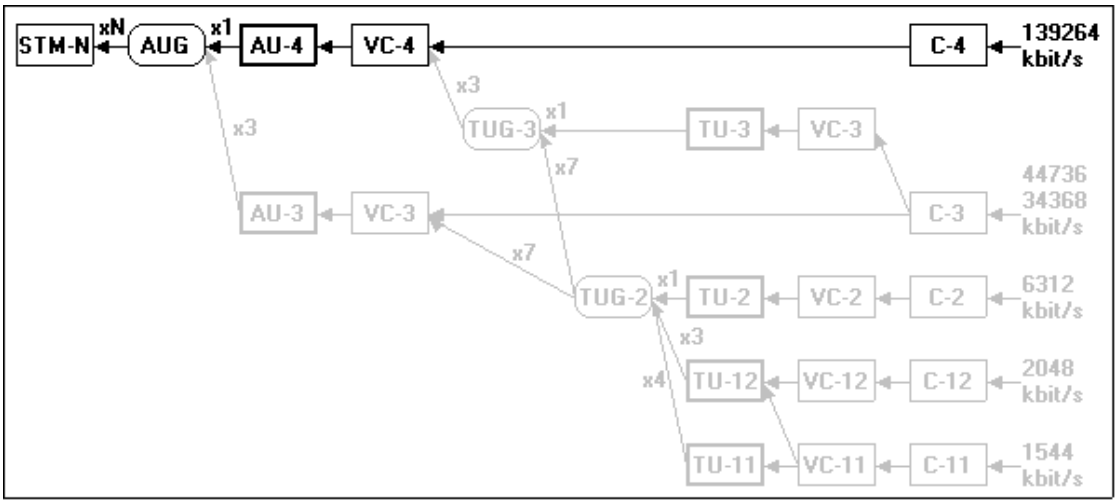


Fig. S-13 Mapping structure: 140 Mbit/s → AU-4 → STM-1

The mapping characteristics are described in Sec. 1.4, Page S-5.

1.8 C-11 mapping (1.5 Mbit/s in STM-1, AU-3/AU-4, TU-11/TU-12)

Option BN 3035/90.04

Mapping structure: AU-3, TU-11

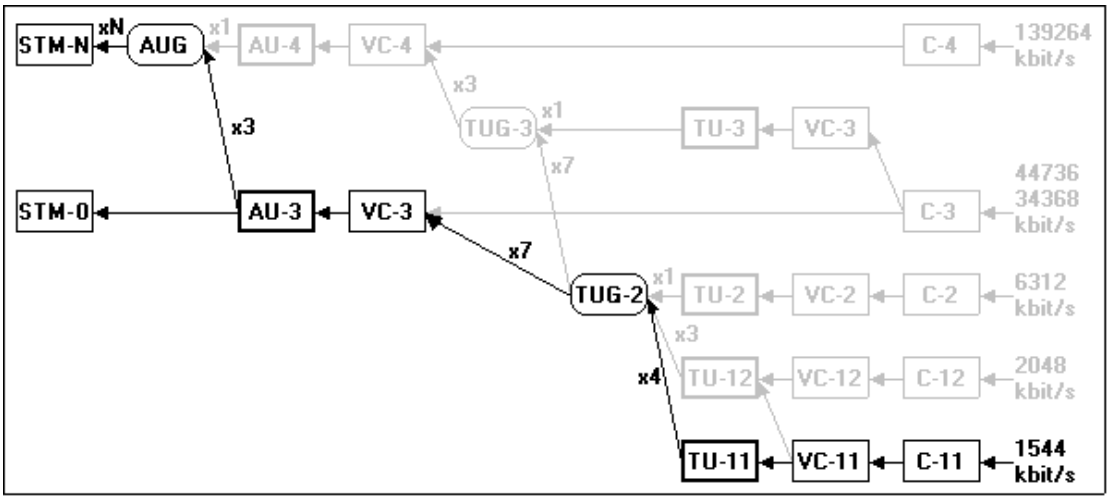


Fig. S-14 Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-3 → STM-1
Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-3 → STM-0;
option 3035/90.10 required

Mapping structure: AU-3, TU-12

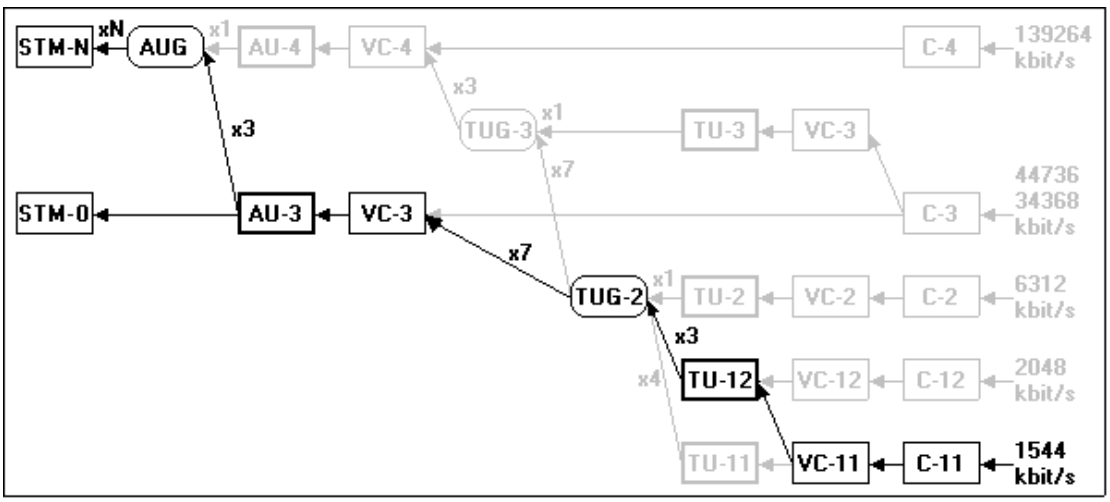


Fig. S-15 Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-3 → STM-1
Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-3 → STM-0;
option 3035/90.10 required

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating); only TU-11

Mapping structure: AU-4, TU-11

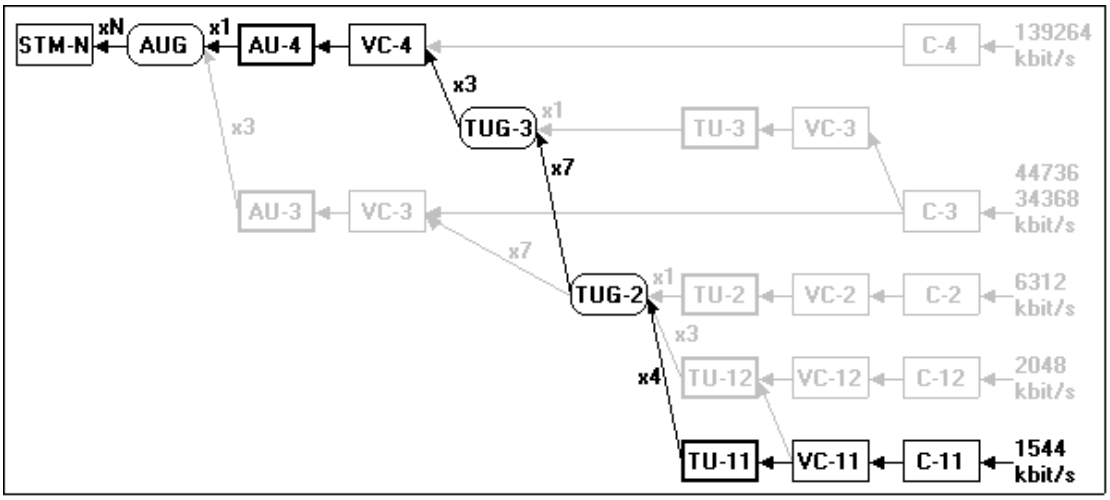


Fig. S-16 Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-4 → STM-1

Mapping structure: AU-4, TU-12

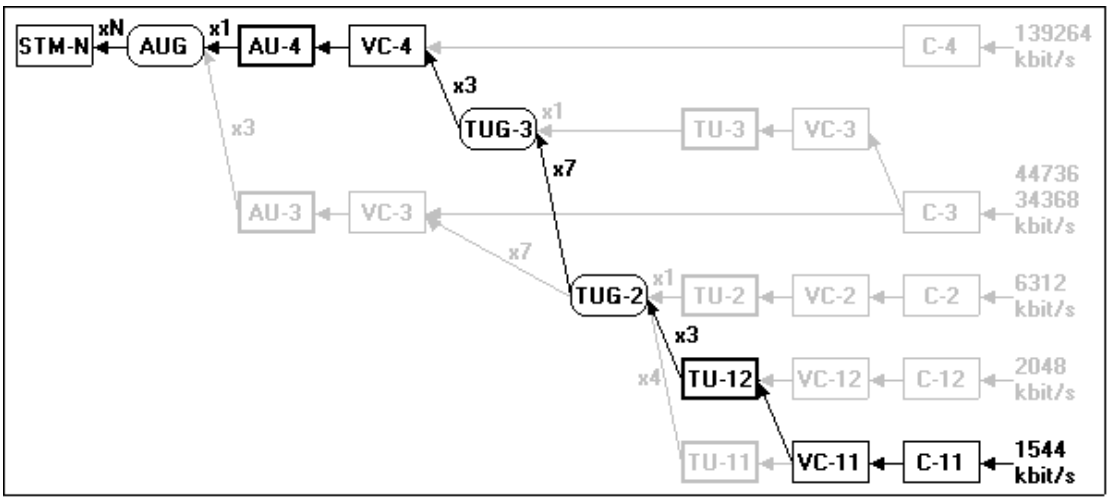


Fig. S-17 Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-4 → STM-1

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating)

1.8.1 VC-11 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “110” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-21 VC-11 POH (Standard Overhead) contents

Measurement channel byte contents (VC-11)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier (Length = 16 frames with CRC7 formation): J2
- Dynamic bytes via V.11 interface (V.11): N2

Filler channel byte contents (VC-11)

Fixed, non-editable (see Tab. S-21).

1.8.2 VC-11 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-6:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-22 Additional available anomalies (VC-11)

Error insertion refers to the selected measurement channel.

1.8.3 VC-11 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-7:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-23 Additional available defects(VC-11)

Alarm generation refers to the selected measurement channel.

1.8.4 VC-11 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-11:

Anomaly	**LED**
LP-BIP	LP-BIP
LP-REI	-

Table S-24 LED display of additional anomalies (VC-11)

Evaluation and display refer to the selected measurement channel.

1.8.5 VC-11 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-12:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-25 LED display of additional defects (VC-11)

Evaluation and display refer to the selected measurement channel.

1.8.6 VC-11 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.9 C-2 mapping (6.3 Mbit/s in STM-1, AU-3/AU-4, TU-2)

Option BN 3035/90.06

Mapping structure: AU-3, TU-2

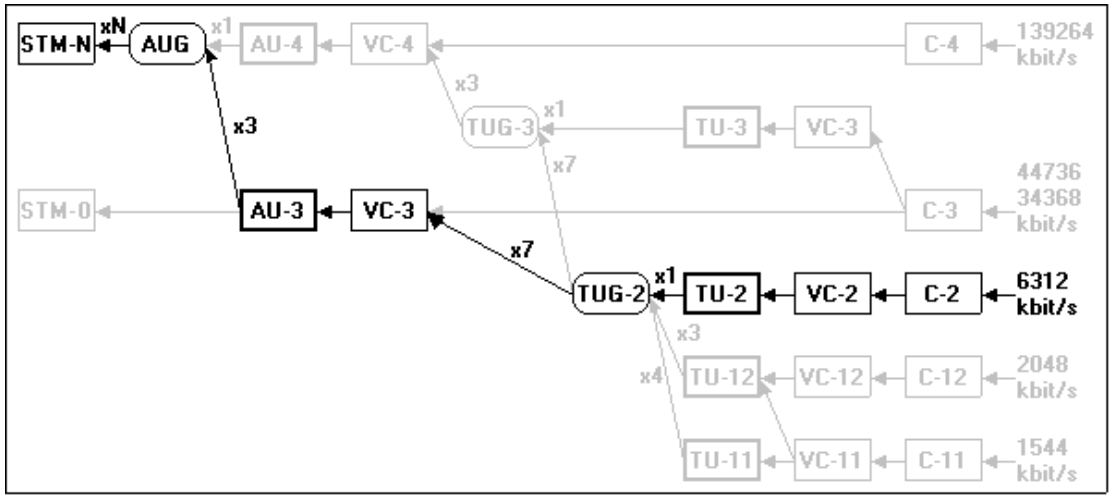


Fig. S-18 Mapping structure: 6.3 Mbit/s → C-2 → TU-2 → AU-3 → STM-1

Mapping method

The following mode is available:

- Asynchronous mode

Mapping structure: AU-4, TU-2

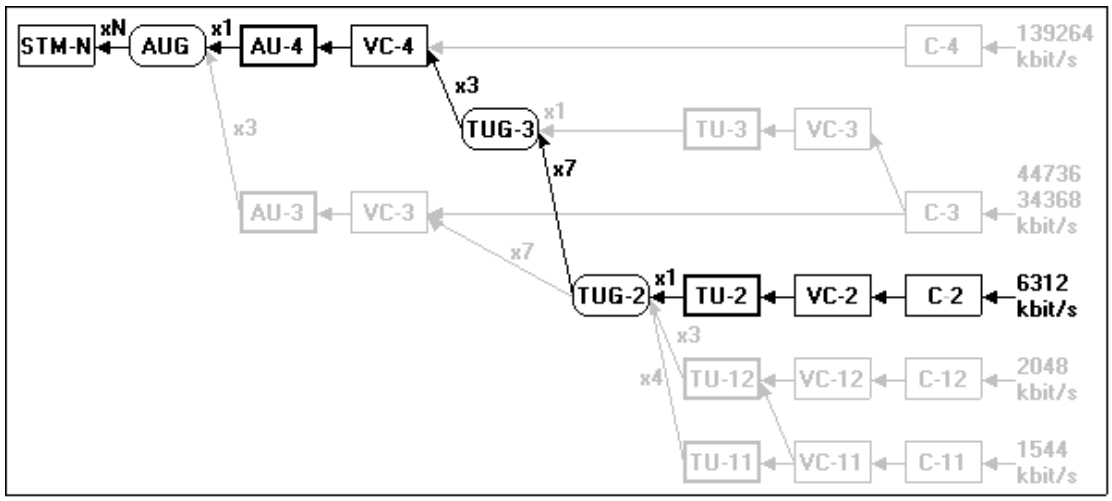


Fig. S-19 Mapping structure: 6.3 Mbit/s → C-2 → TU-2 → AU-4 → STM-1

Mapping method

The following mode is available:

- Asynchronous mode

1.9.1 VC-2 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
LP-BIP (bits 1-2)	Inserted by parity formation	Inserted by parity formation
LP-REI (bit 3)	“0”	“0”
LP-RFI (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “110” for bulk signal	“010” for asynchronous mode
LP-RDI (bit 8)	“0”	“0”
J2 (ASCII)	“WG LP-TRACE”	“WG IDLE”
N2 (hex)	“00”	“00”
K4 (hex)	“00”	“00”

Table S-26 VC-2 POH (Standard Overhead) contents

Measurement channel byte contents (VC-2)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier: J2 (Length = 16 frames with CRC7 formation)
- Dynamic bytes via V.11 interface (V.11): N2

Filler channel byte contents (VC-2)

Fixed, non-editable (see Tab. S-26).

1.9.2 VC-2 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-6:

Anomaly	Single	Rate
BIP-2[1]	yes	2E-4 to 1E-10
LP-REI	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-27 Additional available anomalies (VC-2)

Error insertion refers to the selected measurement channel.

1.9.3 VC-2 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-7:

Defect	Test sensor function	Sensor thresholds	
	On/Off	M in N	I----t1----I I------t2------I
TU-LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-LOP	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TU-AIS	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-UNEQ	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-PLM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-RDI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LP-TIM	yes	-	-
LP-RFI	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-28 Additional available defects (VC-2)

Alarm generation refers to the selected measurement channel.

1.9.4 VC-2 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-11:

Anomaly	LED
LP-BIP	LP-BIP
LP-REI	-

Table S-29 LED display of additional anomalies (VC-2)

Evaluation and display refer to the selected measurement channel.

1.9.5 VC-2 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-12:

Defect	LED
TU-LOM	TU-LOM
TU-LOP	TU-LOP
TU-AIS	TU-AIS
LP-UNEQ	LP-UNEQ
LP-PLM	LP-PLM
LP-RDI	LP-RDI
LP-TIM	-
LP-RFI	-

Table S-30 LED display of additional defects (VC-2)

Evaluation and display refer to the selected measurement channel.

1.9.6 VC-2 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): N2

1.10 Filler channel contents

Mapping structure as for measurement channel, test pattern PRBS11.

2 Drop & Insert / Through Mode

Option: BN 3035/90.20

2.1 Functions

This Option provides the following functions for all mapping options fitted to the ANT-20SE.

Drop & Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

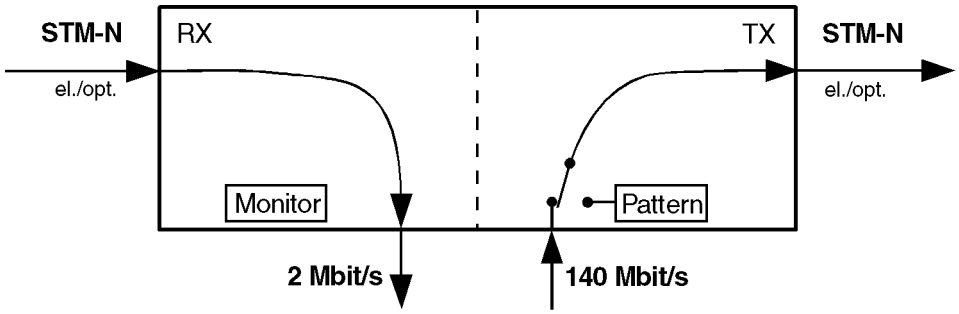


Fig. S-20 Drop & Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 2.2.1, Page S-38 and Sec. 2.3.1, Page S-39).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator. One tributary signal can be output (dropped).

The ANT-20SE can also operate in Through Mode as a signal monitor without affecting the signal content.

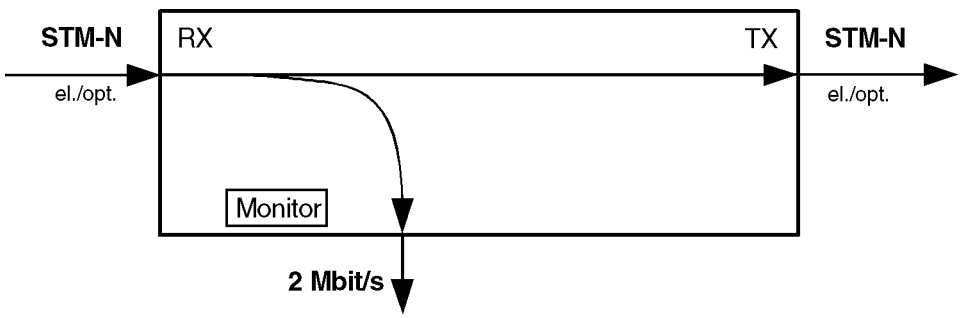


Fig. S-21 Through Mode: Generator and receiver coupled

In conjunction with the Options “PDH MUX/DEMUX” and “M13 MUX/DEMUX”, BN 3035/90.30 to BN 3035/90.32, the ANT-20SE provides access to the tributary channels within the MUX/DEMUX chain (except DS2). This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

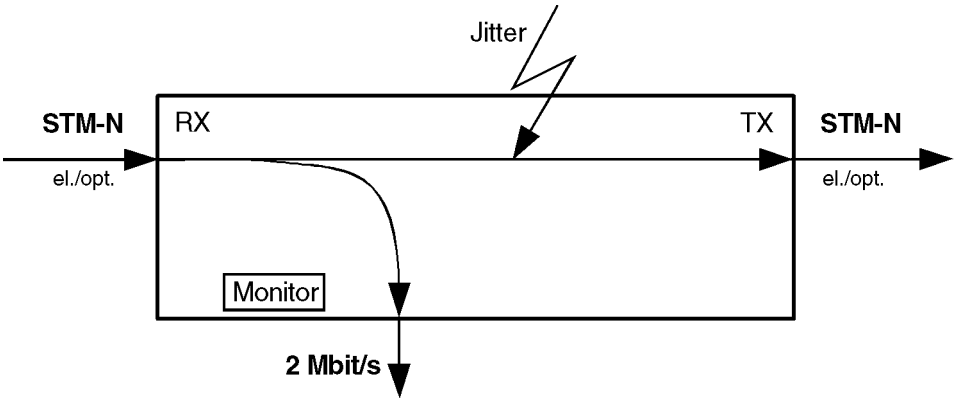


Fig. S-22 Through Mode: Adding jitter to the looped-through signal

In Through Mode, anomalies can be inserted in the SOH or the SOH bytes can be manipulated.

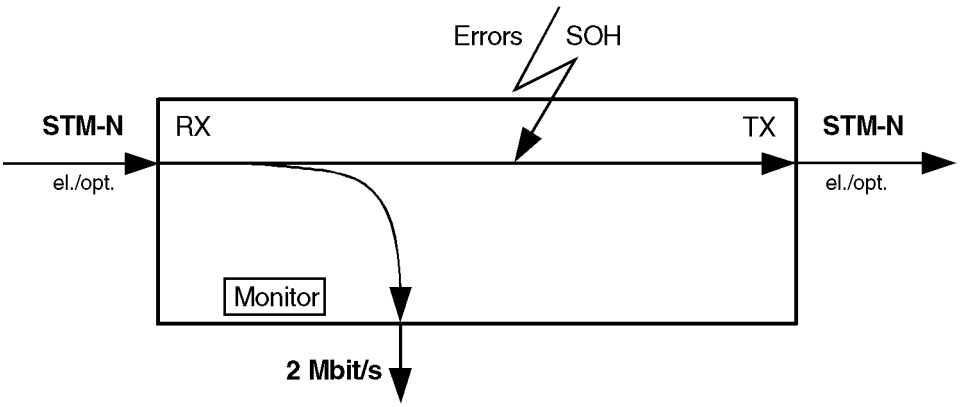


Fig. S-23 Through Mode: Inserting errors in the SOH

2.1.1 Clock generator

Drop & Insert

As specified in the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock.
No offset is possible in this operating mode (see also “Specifications” of the mainframe instrument).

2.1.2 Overhead generator

Drop & Insert

As specified in Sec. 1.4.1, Page S-5.

Through Mode

The “From Rx” function can be set in addition to the functions described in Sec. 1.4.1, Page S-5 for all bytes except bytes B1, B2 and M1.

2.1.3 Anomaly insertion

Drop & Insert

As specified in Sec. 1.4.2, Page S-6.

Through Mode

Anomaly insertion in bytes B1, B2 and MS-REI.
Insertion limits are specified in Sec. 1.4.2, Page S-6.

2.1.4 Defect generation

Drop & Insert

As specified in Sec. 1.4.3, Page S-7.

Through Mode

No direct defect generation is possible.

Alarms (defects) in the SOH can be generated by manipulating the SOH bytes.

2.1.5 Pointer generation

Drop & Insert

As specified in Sec. 1.4.4, Page S-8.

Through Mode

The receive-side pointer is re-transmitted unchanged.

2.1.6 Measurements

There are no restrictions on measurements.
See Sec. 1.4.5, Page S-11 through Sec. 1.4.10, Page S-16.

2.2 Signal outputs

2.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
DS2	6.312	B8ZS	± 2.0 V
E1	2.048	HDB3	± 2.37 V
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-31 Specifications of the AUXILIARY signal output [11], electrical

2.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-32 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used both as “LINE” and as “AUXILIARY” output.

2.3 Signal inputs

2.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
DS2	6.312	B8ZS	2.0 V ±10 %
E1	2.048	HDB3	2.37 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-33 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

2.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-34 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used both as “LINE” and as “AUXILIARY” input.

Specifications STS-1 Mappings

These specifications apply to the options:

SONET mappings

STS-1 mapping for ANSI tributaries

STS-1 mapping for ETSI tributaries

1 STS-1 mapping

1.1 General information

STS-1 and STS-3 signals

STS-1 and STS-3 signals are generated and evaluated to conform with Bellcore GR-253 and ANSI T1.105.

The STS-3 signal consists of one STS-1 tributary equipped with a selected payload and two unequipped STS-1 tributaries.

Mapping/Demapping

One selected STS-1 mapping is included in the mainframe instrument. Other mappings can be added as required.

Container contents:

- Framed or unframed asynchronous payload in a selected container.
- Filling of a selected container with a test pattern,
  without justification bits (bulk signal).

Drop & Insert

An additional Drop & Insert Option (BN 3035/90.20) for dropping or inserting tributary signals (via sockets) is available in conjunction with the mapping options.

1.2 Tributary channel numbering

VT1.5 locations

VT1.5#	Group #/VT #	Column[1] #s	VT1.5#	Group #/VT #	Column[1] #s
1	1, 1	2, 31, 60	15	1, 3	16, 45, 74
2	2, 1	3, 32, 61	16	2, 3	17, 46, 75
3	3, 1	4, 33, 62	17	3, 3	18, 47, 76
4	4, 1	5, 34, 63	18	4, 3	19, 48, 77
5	5, 1	6, 35, 64	19	5, 3	20, 49, 78
6	6, 1	7, 36, 65	20	6, 3	21, 50, 79
7	7, 1	8, 37, 66	21	7, 3	22, 51, 80
8	1, 2	9, 38, 67	22	1, 4	23, 52, 81
9	2, 2	10, 39, 68	23	2, 4	24, 53, 82
10	3, 2	11, 40, 69	24	3, 4	25, 54, 83
11	4, 2	12, 41, 70	25	4, 4	26, 55, 84
12	5, 2	13, 42, 71	26	5, 4	27, 56, 85
13	6, 2	14, 43, 72	27	6, 4	28, 57, 86
14	7, 2	15, 44, 73	28	7, 4	29, 58, 87

1 Column 1 = STS POH
Column 30, 59 = Fixed stuff

Table S-35 VT1.5 locations

VT2 locations

VT2#	Group #/VT #	Column[1] #s	VT2#	Group #/VT #	Column[1] #s
1	1, 1	2, 23, 45, 67	12	5, 2	13, 35, 56, 78
2	2, 1	3, 24, 46, 68	13	6, 2	14, 36, 57, 79
3	3, 1	4, 25, 47, 69	14	7, 2	15, 37, 58, 80
4	4, 1	5, 26, 48, 70	15	1, 3	16, 38, 60, 81
5	5, 1	6, 27, 49, 71	16	2, 3	17, 39, 61, 82
6	6, 1	7, 28, 50, 72	17	3, 3	18, 40, 62, 83
7	7, 1	8, 29, 51, 73	18	4, 3	19, 41, 63, 84
8	1, 2	9, 31, 52, 74	19	5, 3	20, 42, 64, 85
9	2, 2	10, 32, 53, 75	20	6, 3	21, 43, 65, 86
10	3, 2	11, 33, 54, 76	21	7, 3	22, 44, 66, 87
11	4, 2	12, 34, 55, 77	-	-	-

1 Column 1 = STS POH
Column 30, 59 = Fixed stuff

Table S-36 VT2 locations

VT6 locations

VT6#	Group #/VT #	Column[1] #s
1	1, 1	2, 9, 16, 23, 31, 38, 45, 52, 60, 67, 74, 81
2	2, 1	3, 10, 17, 24, 32, 39, 46, 53, 61, 68, 75, 82
3	3, 1	4, 11, 18, 25, 33, 40, 47, 54, 62, 69, 76, 83
4	4, 1	5, 12, 19, 26, 34, 41, 48, 55, 63, 70, 77, 84
5	5, 1	6, 13, 20, 27, 35, 42, 49, 56, 64, 71, 78, 85
6	6, 1	7, 14, 21, 28, 36, 43, 50, 57, 65, 72, 79, 86
7	7, 1	8, 15, 22, 29, 37, 44, 51, 58, 66, 73, 80, 87

1 Column 1 = STS-1 POH
Colunm 30, 59 = Fixed stuff

Table S-37 VT6 locations

1.3 Scrambling/Descrambling

The STS-N signal is scrambled/descrambled as described in Bellcore GR-253 and ANSI T1.105.

1.4 Overhead generation

1.4.1 Transport Overhead (TOH)

Standard overhead, STS-1 (hex)

TOH			
	1	**2**	**3**
1	A1 F6	A2 28	J0 01
2	B1 XX	E1 00	F1 00
3	D1 00	D2 00	D3 00
4	H1 60	H2 00	H3 00
5	B2 XX	K1 00	K2 00
6	D4 00	D5 00	D6 00
7	D7 00	D8 00	D9 00
8	D10 00	D11 00	D12 00
9	S1 00	M0 00	E2 00

Table S-38 TOH contents, STS-1

Standard overhead, STS-3 (hex), STS-3c

TOH										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	
1	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	J0 01	— 02	— 03	
2	B1 XX	— 00	— 00	E1 00	— 00	— 00	F1 00	— 00	— 00	
3	D1 00	— 00	— 00	D2 00	— 00	— 00	D3 00	— 00	— 00	
4a	H1 60	H1 60	H1 60	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	at STS-3
4b	H1 60	Y 93	Y 93	H2 00	— FF	— FF	H3 00	H3 00	H3 00	at STS-3c
5	B2 XX	B2 XX	B2 XX	K1 00	— 00	— 00	K2 00	— 00	— 00	
6	D4 00	— 00	— 00	D5 00	— 00	— 00	D6 00	— 00	— 00	
7	D7 00	— 00	— 00	D8 00	— 00	— 00	D9 00	— 00	— 00	
8	D10 00	— 00	— 00	D11 00	— 00	— 00	D12 00	— 00	— 00	
9	S1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	E2 00	— 00	— 00	

Table S-39 TOH contents, STS-3

XX: Inserted by parity formation (B1, B2)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown), H3 depends on whether or not a pointer action takes place.

TOH byte contents

- Static bytes: all except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: all except B1, B2, H1, H2, H3
- Dynamic bytes filled using PRBS 11: E1, F1, E2
- Dynamic byte groups filled using PRBS 11: D1 to D3, D4 to D12
- Dynamic bytes filled via DCC/ECC interface (V.11): E1, F1, E2
- Dynamic byte groups filled via DCC/ECC interface (V.11): D1 to D3, D4 to D12, K1 to K2

1.4.2 STS-N error insertion (anomalies)

Error insertion (anomalies) . . . . . B1, B2, B3 parity errors, FAS word errors, REI-L, REI-P, bit errors in test pattern (TSE), code errors (single errors only)

Trigger types . . . . . Single or Rate

When Rate triggering is selected a bit error rate is inserted.

Anomaly	**Single**	**Rate**[1]	**Burst m, n (frames)**
FAS	yes	2E-3 to 1E-10	m = 1 to 196000
B1	yes	2E-4 to 1E-10	m = 1 to 196000
B2	yes	2E-3 to 1E-10	m = 1 to 196000
REI-L	yes	2E-3 to 1E-10	m = 1 to 196000
B3[2]	yes	2E-4 to 1E-10	m = 1 to 196000
REI-P	yes	2E-4 to 1E-10	m = 1 to 196000
TSE	yes	1E-2 to 1E-8	-
BPV (code error)	yes	-	-

1 Mantissa: 1 to 9 (only 1 for TSE), exponent: -1 to -10 (whole numbers)
2 Static error insertion, can be edited using a 8-bit mask (x = don't care, 1 = insert error)

Table S-40 Available anomalies and trigger modes (STS-N)

The insertion of **errors** (anomalies) **and alarms** (defects) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.3 STS-N alarm generation (defects)

Defect	Test sensor function	Test sensor thresholds	
	On/Off	M in N	|----t1----| |------t2------|
LOS[1]	ja	M = 800 bis 7200 N = 1600 bis 8000	t1 = 0.1 bis 60.0 s t2 = 0.2 bis 600 s
LOF	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-L	yes	-	-
AIS-L	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-L	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-P	yes	-	-
PDI-P	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s or t1 = 0.5 to 250 ms t2=1 to 8000 ms

1 Only in conjunction with an optical interface

Table S-41 Available defects (STS-N)

The insertion of **alarms** (defects) **and errors** (anomalies) are mutually exclusive. The first action selected is active. The second action is rejected.

1.4.4 Pointer action generation

Stimulation

Pointer sequences

On all pointer levels to ANSI T1.105.03

T1, T4: 0.25 ms to 600 s . . . . . (2 to 4800000 frames)

T2, T3: 0.25 ms to 10 s . . . . . (2 to 80000 frames)

T5: 0 ms to 600 s. . . . . (0 to 4800000 frames)

n: 1 to 2000

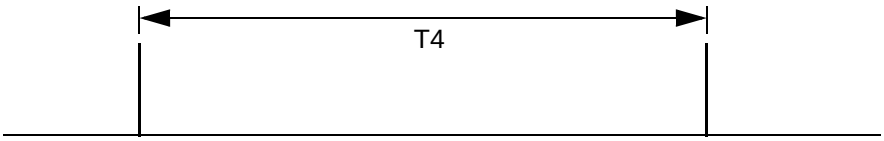


Fig. S-24 Perodic (single/multiple) pointers with identical polarity

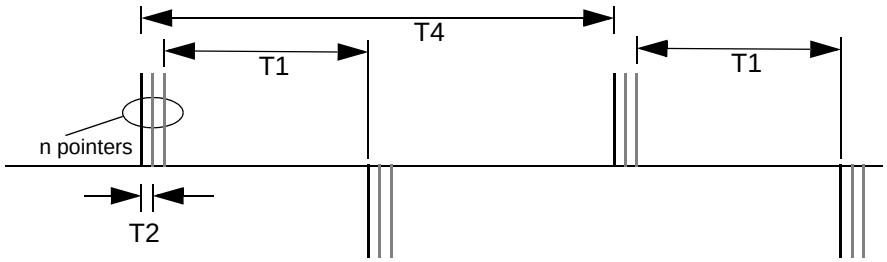


Fig. S-25 Perodic (single/multiple) pointers with different polarity

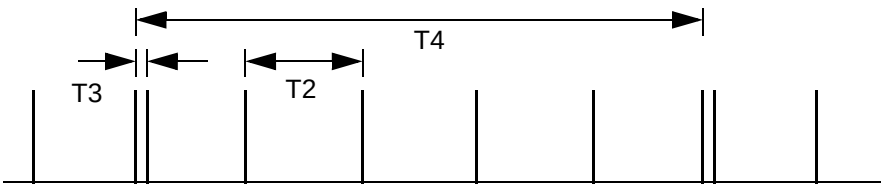


Fig. S-26 Periodic pointers with one double pointer

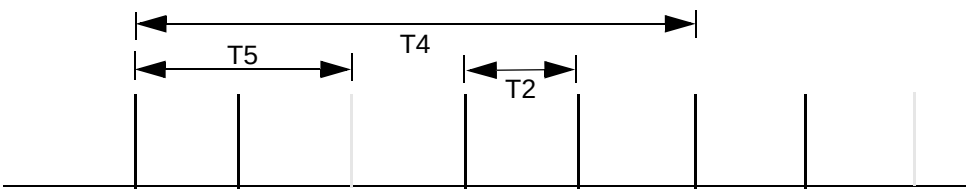


Fig. S-27 Periodic pointers with one missing pointer

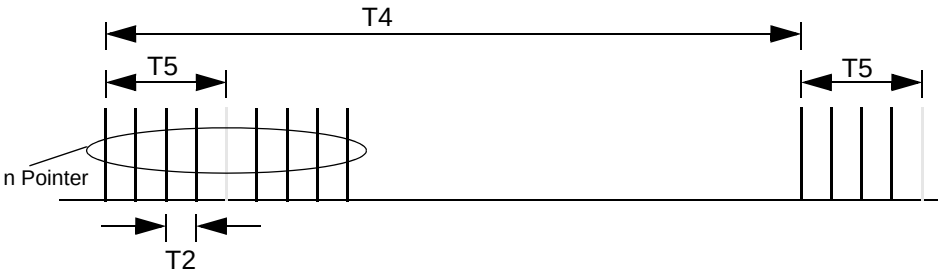


Fig. S-28 Pointer burst with missing pointers

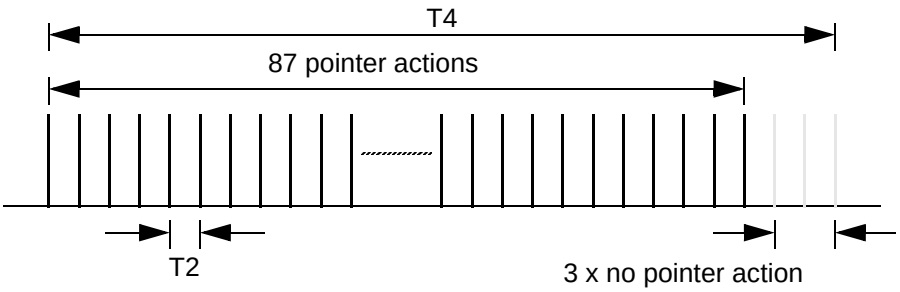


Fig. S-29 ”87-3” sequence

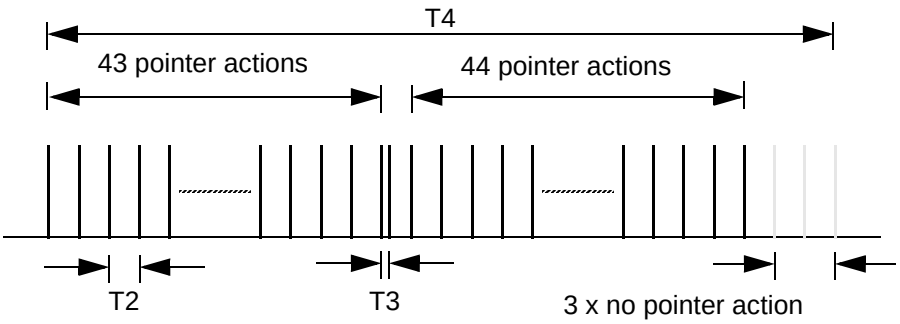


Fig. S-30 ”43-44” sequence with double pointer

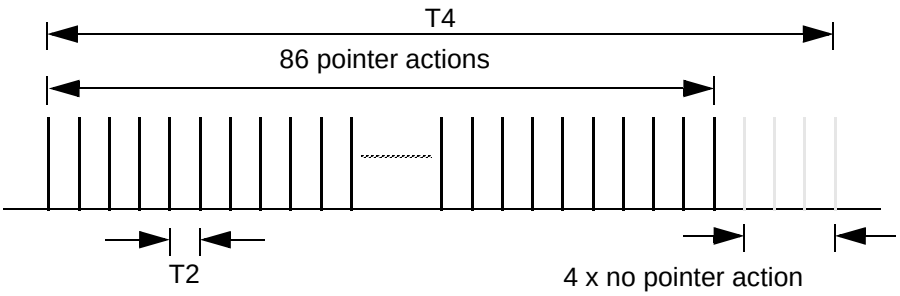


Fig. S-31 ”86-4” sequence with missing pointer

Pointer jumps

Pointer jump from pointer value A to pointer value B (also setting a new pointer).

Pointer jumps are executed with or without NDF.

Pointer range A + B:
STS pointer . . . . . 0 to 782
VT6 pointer . . . . . 0 to 427
VT2 pointer . . . . . 0 to 139
VT1.5 pointer . . . . . 0 to 103

1.4.5 STS-N error measurements (anomalies)

Evaluation

All errors (anomalies) are counted simultaneously and stored.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

of anomalies via LEDs:

CURRENT LED (red) is on when the anomaly is present

HISTORY LED (yellow) is on if the anomaly has occurred at least once during the current measurement interval.

Display of errors as count or ratio values (equivalent bit error ratio): When calculating the ratio value, correction formulae are used for the anomalies B1, B2, B3 and BIP-2 as well as REI-L and REI-P. These take into account that a multiple error in the same bit can lead to clearance of the error.

Anomaly	**LED**
OOF	LOF/OOF
FAS	-
B1	B1/B2
B2	B1/B2
REI-L	-
B3	B3
REI-P	-

Table S-42 LED display of available anomalies (STS-N)

Evaluation and display refer to the selected measurement channel.

1.4.6 STS-N alarm detection (defects)

Evaluation

All alarms (defects) which occur are evaluated simultaneously where possible and stored. Storage takes place only within a started measurement interval.

Time resolution of defects . . . . . 100 ms

Display

of defects via LEDs:

CURRENT LED (red) is on when the defect is present

HISTORY LED (yellow) is on if the defect has occurred at least once during the current measurement interval.

Defect	**LED**
LOS	LOS
LOF	LOF/OOF
TIM-L	-
AIS-L	MS-AIS/AIS-L
RDI-L	MS-RDI/RDI-L
LOP-P	AU-LOP/LOP-P
AIS-P	AU-AIS/AIS-P
UNEQ-P	HP-UNEQ/UNEQ-P
PLM-P	HP-PLM/PLM-P
RDI-P	HP-RDI/RDI-P
TIM-P	-
PDI-P	-

Table S-43 LED display of available defects (STS-N)

Evaluation and display refer to the selected measurement channel.

1.4.7 Evaluation of STS and VT pointer actions

Evaluation

All pointers in the selected path are shown as absolute values and the direction and number of pointer movements is detected and counted.

NDF (New Data Flag) is detected and counted.

Display

of:

- Number of pointer operations separate for STS and VT pointers:
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address
- Number of NDF events
- Corresponding clock deviation
- NDF-P and NDF-V can be indicated by the LED display on the front panel
  (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “NDF-P” in addition to “LOP-P”
  – the “TU-LOP/LOP-V”LED indicates “NDF-V” in addition to “LOP-V”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are displayed as a histogram with selectable time resolution in seconds, minutes, hours or days.

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are printed out as a table with 1 second time resolution.

1.4.8 Evaluation of Transport Overhead (TOH) and Path Overhead (POH)

Evaluation

Bit error measurement

using PRBS 11 (bytes) E1, F1, E2, F2
using PRBS 11 (byte groups) . . . . . D1 to D3, D4 to D12

Output

as bytes via DCC/ECC interface (V.11) E1, F1, E2, F2, K3
as byte groups via DCC/ECC interface (V.11) . . . . . .D1 to D3, D4 to D12, K1 to K2

Display

of complete TOH and POH . . . . . hexadecimal
of Trace Identifier J0, J1. . . . . .ASCII, plain text

1.4.9 STS Path Overhead (POH)

Standard overhead

POH Byte	Option 3035/90.10 Option 3035/90.11 Option 3035/90.13	Option 3035/90.12	Option 3035/90.03	Option 3035/90.70 Option 3035/90.71
J1 (ASCII)	“WG STS-TRACE”			
B3 (hex)	Inserted by parity formation			
C2 (hex)	“02”	“04”	“12” at mapping “01” at bulk	“13”
G1 (hex)	“00”			
F2 (hex)	“00”			
H4 (hex)	“FC”, ”FD”, ”FE”, ”FF” sequence across 4 frames	“FF”	“FF”	“FF”
	48-frames-sequence as GR253			
F3 (hex)	“00”			
Z4 (hex)	“00”			

Table S-44 POH contents

STS POH byte contents

- Static bytes: all except B3, H4
- Overhead sequence m, n, p: J1, C2, G1, F2, F3, Z4
- Trace Identifier (Length = 64 frames): J1
- Dynamic byte filled using PRBS 11: F2
- Dynamic bytes filled via DCC/ECC interface (V.11): F2, Z4, N1
- H4 sequence, switchable, 4/48 Bytes

1.5 STS-3c mapping (E4 in STS-3c, ATM in STS-3c)

Option BN 3035/90.03 or BN 3035/90.70 required

STS-3c SPE mapping structure

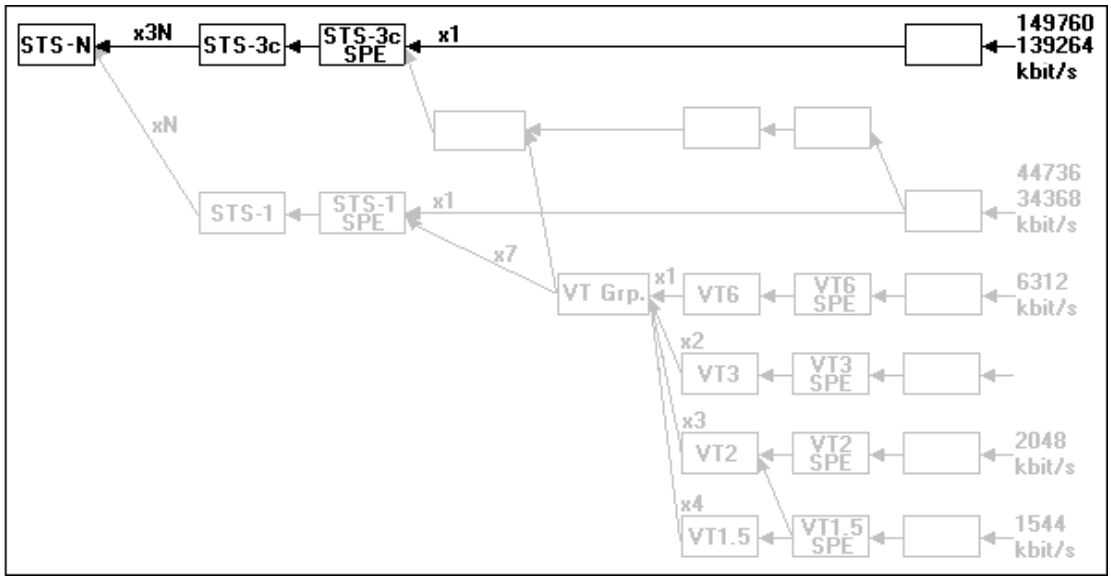


Fig. S-32 Mapping structure: 139 MBits/s → STS-3c SPE → STS-3c

Path overhead contents Sec. 1.4, Page S-44.

1.6 STS-1 SPE mapping (DS3 in STS-1, 34/45 Mbit in STM-0)

Option BN 3035/90.12 required

34/45 Mbit/s in STM-0 see also: “STM-1 mapping” Operating Manual”.

STS-3c SPE mapping structure

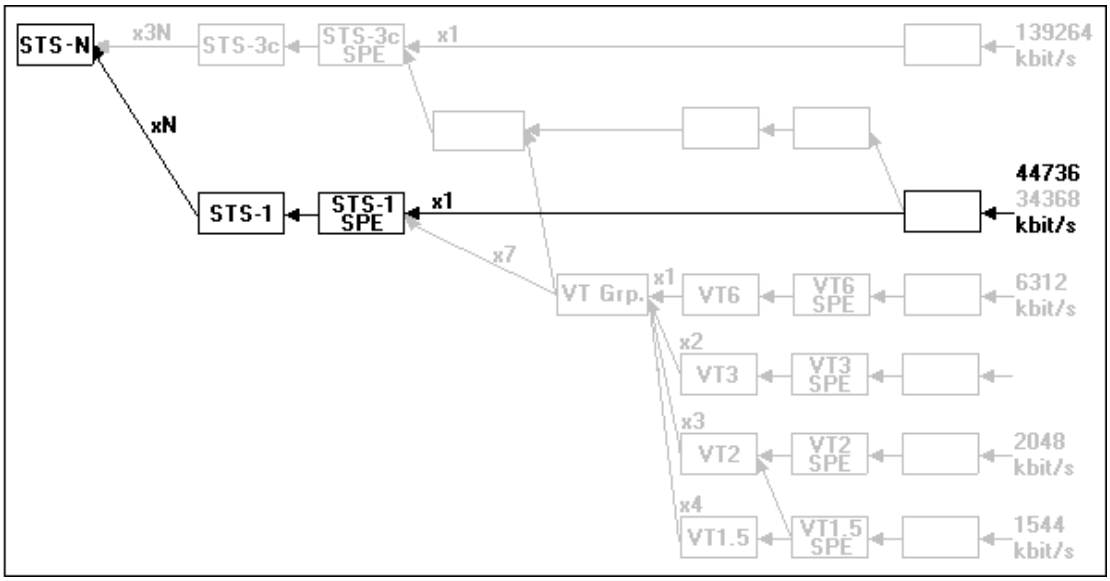


Fig. S-33 Mapping structure: DS3 → STS-1 SPE → STS-1/3

Path overhead contents Sec. 1.4, Page S-44.

1.7 VT1.5 SPE mapping (DS1 in STS-1/3, 1.5 Mbit in STM-0)

Option BN 3035/90.10

1.5 Mbit/s in STM-0 see also: “STM-1 mapping” Operating Manual, section “C-11 mapping”.

VT1.5 mapping structure

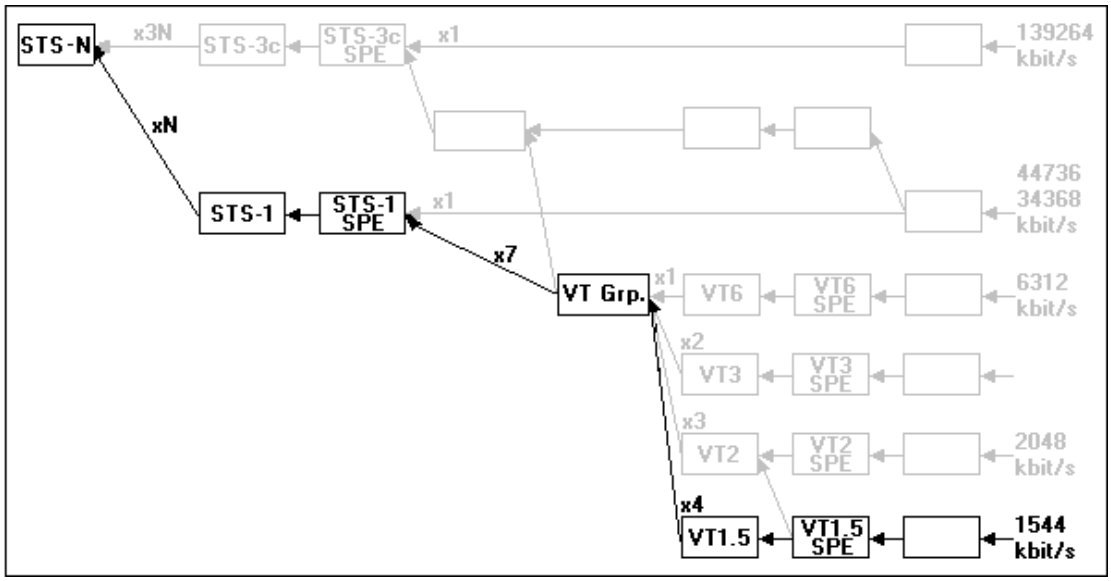


Fig. S-34 Mapping structure: DS1 → VT1.5 → STS-1 SPE → STS-1/3

1.5 Mbit/s in STM-0 mapping structure (AU-3, TU-11)

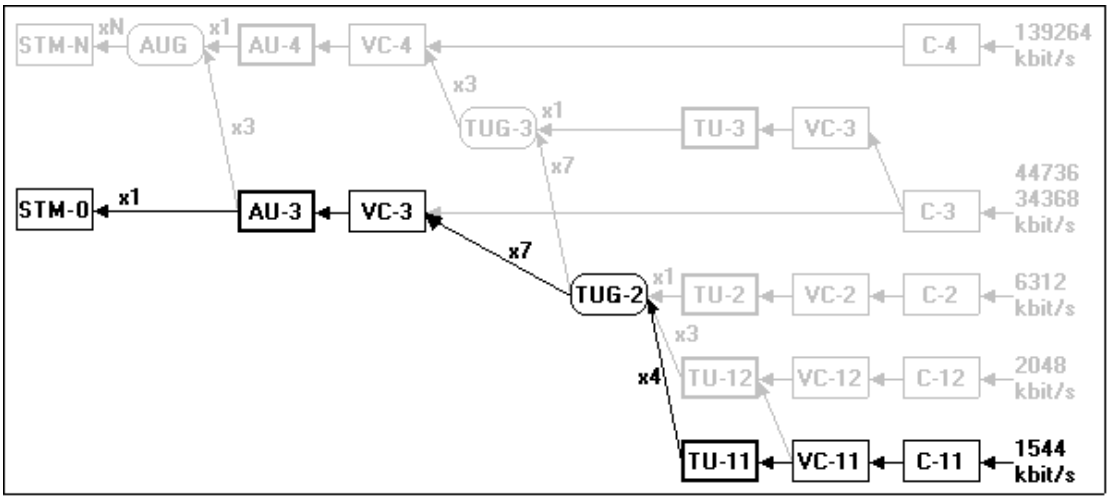


Fig. S-35 Mapping structure: 1.5 Mbit/s → C-11 → TU-11 → AU-3 → STM-0

1.5 Mbit/s in STM-0 mapping structure (AU-3, TU-12)

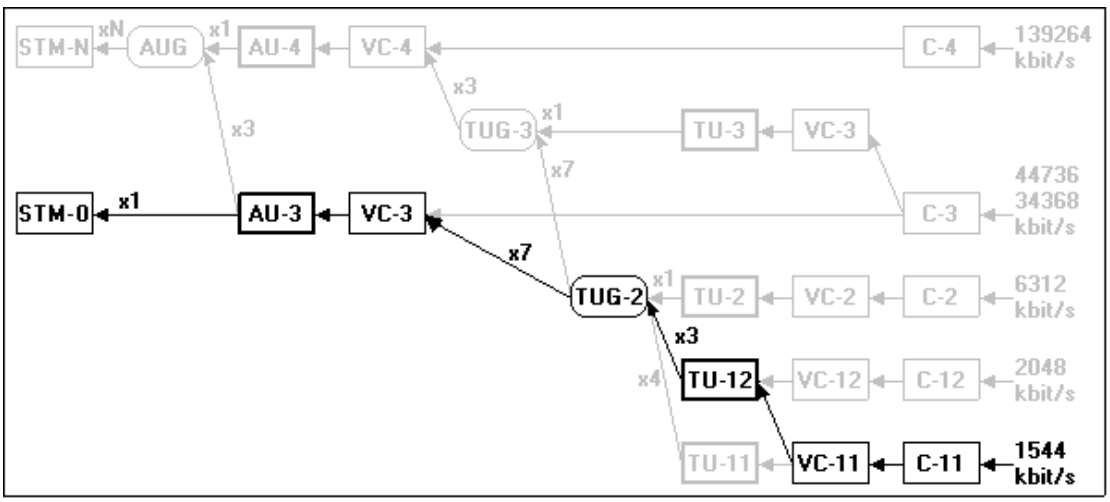


Fig. S-36 Mapping structure: 1.5 Mbit/s → C-11 → TU-12 → AU-3 → STM-0

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating); TU-11

1.7.1 VT1.5 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
BIP-V (bits 1-2)	Inserted by parity formation	Inserted by parity formation
REI-V (bit 3)	“0”	“0”
RFI-V (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “001” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
RDI-V (bit 8)	“0”	“0”
J2	“WG VT-TRACE” (ASCII)	“00” (hex)
Z6 (hex)	“00”	“00”
Z7 (hex)	“00”	“00”

Table S-45 VT1.5 POH (Standard Overhead) contents

Measurement channel byte contents (VT1.5)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier (Length = 64 frames): J2
- Dynamic bytes filled via DCC/ECC interface (V.11): Z6

Filler channel byte contents (VT1.5)

Fixed (non-editable) as in (see Tab. S-45)

1.7.2 VT1.5 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-46:

Anomaly	Single	Rate
BIP-V[1]	yes	2E-4 to 1E-10
REI-V	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-46 Additional anomalies (VT1.5)

Error insertion refers to the selected measurement channel.

1.7.3 VT1.5 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-47:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
LOM-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-V	yes	-	-
RFI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PDI-V	yes	M = 1 toN - 1 N = 1 to 8000	t1 = 0,1 to 60,0 s t2 = 0.2 to 600 s or t1 = 0.5 to 250 ms t2=1 to 8000 ms

Table S-47 Additional defects (VT1.5)

Alarm generation refers to the selected measurement channel.

1.7.4 VT1.5 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): Z6

1.7.5 VT1.5 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-50:

Anomaly	**LED**
BIP-V	LP-BIP/BIP-V
REI-V	-

Table S-48 LED display of additional anomalies (VT1.5)

Evaluation and display refer to the selected measurement channel.

1.7.6 VT1.5 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-52:

Defect	**LED**
LOM	TU-LOM
LOP-V	TU-LOP/LOP-V
AIS-V	TU-AIS/AIS-V
UNEQ-V	LP-UNEQ/UNEQ-V
PLM-V	LP-PLM/PLM-V
RDI-V	LP-RDI/RDI-V
TIM-V	-
RFI-V	-
PDI-V	-

Table S-49 LED display of additional defects (VT1.5)

Evaluation and display refer to the selected measurement channel.

1.8 VT2 mapping (E1 in STS-1/3, 2 Mbit/s in STM-0)

Option: BN 3035/90.13

2 Mbit/s in STM-0: see also “STM-1 mappings” Operating Manual, section “C-12 mapping”.

VT2 mapping structure

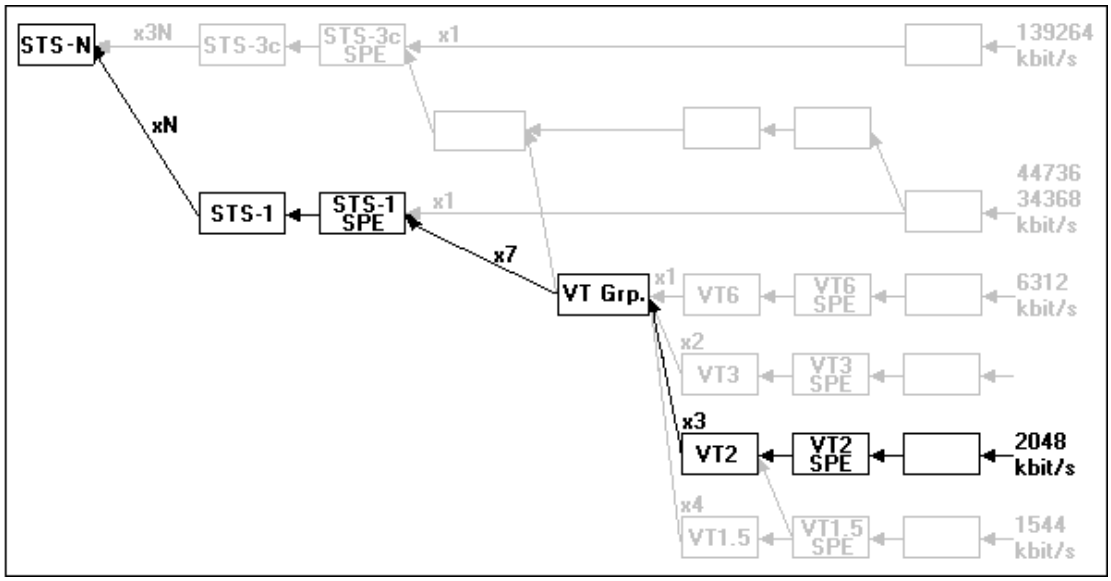


Fig. S-37 Mapping structure: 2 Mbit/s → VT2 SPE → STS-1 SPE → STS-1/3

2 Mbit/s in STM-0 mapping structure

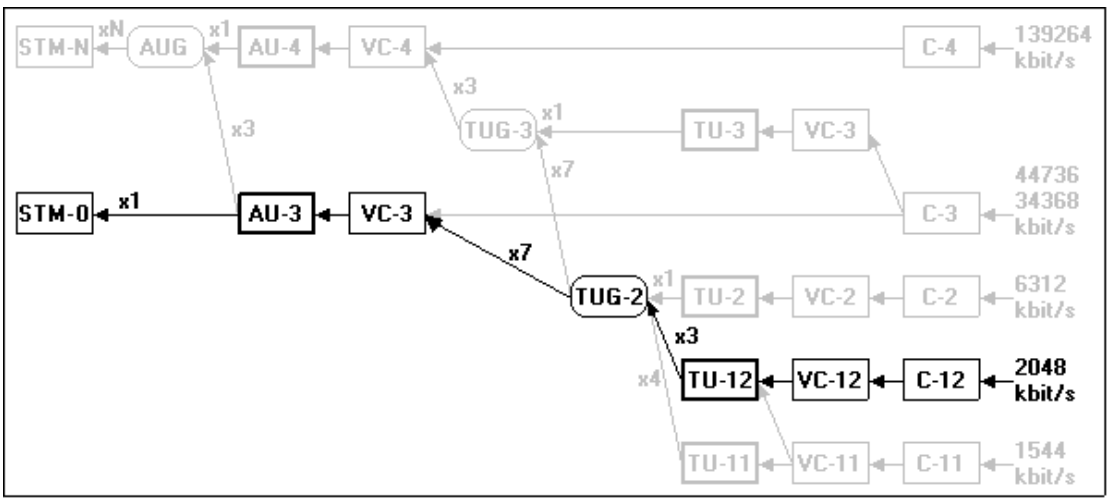


Fig. S-38 Mapping structure: 2 Mbit/s → AU-3 → STM-0

Mapping method

The following modes are available:

- Asynchronous mode
- Byte-synchronous mode (floating)

1.8.1 VT2 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
BIP-V (bits 1-2)	Inserted by parity formation	Inserted by parity formation
REI-V (bit 3)	“0”	“0”
RFI-V (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “100” for byte-synchronous mode “001” for bulk signal	“010” for asynchronous mode “100” for byte-synchronous mode
RDI-V (bit 8)	“0”	“0”
J2	“WG VT-TRACE” (ASCII)	“00” (hex)
Z6 (hex)	“00”	“00”
Z7 (hex)	“00”	“00”

Table S-50 VT2 POH (Standard Overhead) contents

Measurement channel byte contents (VT2)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier: J2 (Length = 64 frames)
- Dynamic bytes filled via DCC/ECC interface (V.11): Z6

Filler channel byte contents (VT2)

Fixed (non-editable) as in Tab. S-50, Page S-63

1.8.2 VT2 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in Sec. 1.4.2, Page S-46:

Anomaly	Single	Rate
BIP-V[1]	yes	2E-4 to 1E-10
REI-V	yes	2E-4 to 1E-10

1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)

Table S-51 Additional anomalies (VT2)

Error insertion refers to the selected measurement channel.

1.8.3 VT2 alarm generation (defects)

2 Mbit/s in STM-0: see “STM-1 mapping” Operating Manual, section “C-12 mapping”.

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-47:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-V	yes	-	-
RFI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s or t1 = 0.5 to 250 ms t2 = 1 to 8000 ms
PDI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-52 Additional defects (VT2)

Alarm generation refers to the selected measurement channel.

1.8.4 VT2 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): Z6

1.8.5 VT2 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-50:

Anomaly	**LED**
BIP-V	LP-BIP/BIP-V
REI-V	-

Table S-53 LED display of additional anomalies (VT2)

Evaluation and display refer to the selected measurement channel.

1.8.6 VT2 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in Sec. 1.4.6, Page S-52:

Defect	**LED**
LOM	LOM
LOP-V	TU-LOP/LOP-V
AIS-V	TU-AIS/AIS-V
UNEQ-V	LP-UNEQ/UNEQ-V
PLM-V	LP-PLM/PLM-V
RDI-V	LP-RDI/RDI-V
TIM-V	-
RFI-V	-
PDI-V	-

Table S-54 LED display of additional defects (VT2)

Evaluation and display refer to the selected measurement channel.

1.9 VT6 mapping (6 Mbit/s in STS-1/3)

Option BN 3035/90.11

Mapping structure: VT6

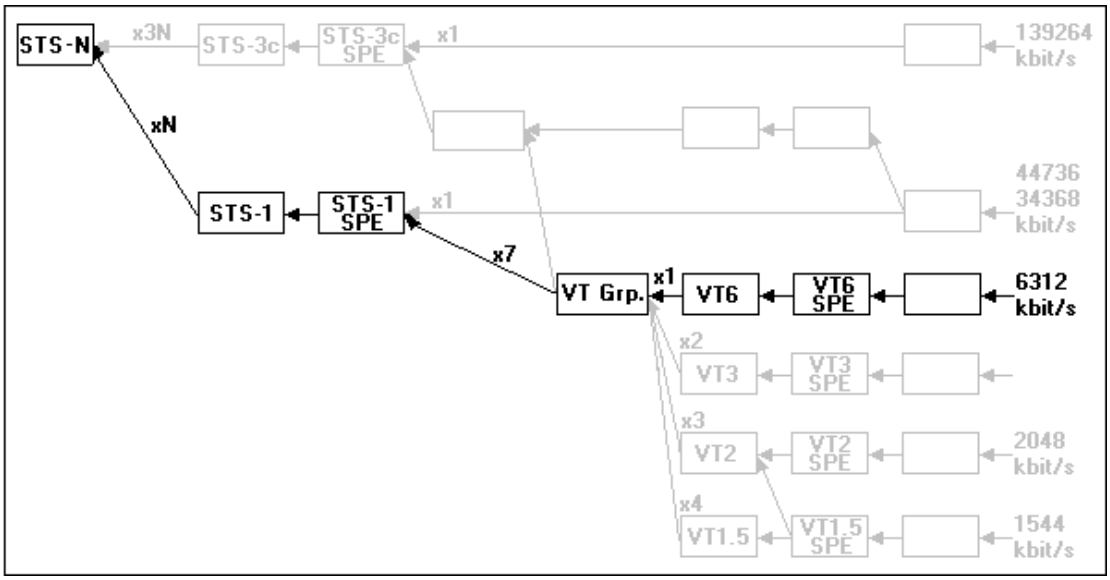


Fig. S-39 Mapping structure: 6 Mbit/s → VT6 SPE → STS-1 SPE → STS-1/3

Mapping method

The following mode is available:

- Asynchronous mode

1.9.1 VC-6 Path Overhead contents

POH byte	Measurement channel	Filler channels
V5 (binary)		
BIP-V (bits 1-2)	Inserted by parity formation	Inserted by parity formation
REI-V (bit 3)	“0”	“0”
RFI-V (bit 4)	“0”	“0”
Path Label (bit 5-7)	“010” for asynchronous mode “001” for bulk signal	“010” for asynchronous mode
RDI-V (bit 8)	“0”	“0”
J2	“WG VT-TRACE” (ASCII)	“00” (hex)
Z6 (hex)	“00”	“00”
Z7 (hex)	“00”	“00”

Table S-55 VT6 POH (Standard Overhead) contents

Measurement channel byte contents (VT6)

- Static bytes: all except bits 1-2 of V5
- Overhead sequence m, n, p: J2, N2, K4
- Trace Identifier: J2 (Length = 64 frames)
- Dynamic bytes filled via DCC/ECC interface (V.11): Z6

Filler channel byte contents (VT6)

Fixed (non-editable) as in (see Tab. S-55)

1.9.2 VT6 error insertion (anomalies)

The following anomalies can be inserted in addition to the error types specified in section 1.4.2 “STS-N error insertion (anomalies)”:

Anomaly	Single	Rate
BIP-V[1]	yes	2E-4 to 1E-10
REI-V	yes	2E-4 to 1E-10
1 Static error insertion, can be edited using a 2-bit mask (x = don’t care, 1 = insert error)		

Table S-56 Additional anomalies (VT6)

Error insertion refers to the selected measurement channel.

1.9.3 VT6 alarm generation (defects)

The following defects can be generated in addition to the alarm types specified in Sec. 1.4.3, Page S-47:

Defect	**Test sensor function**	**Sensor thresholds**	
	On/Off	M in N	I----t1----I I------t2------I
LOM	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-V	yes	-	-
RFI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s or t1 = 0.5 to 250 ms t2 = 1 to 8000 ms
PDI-V	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-57 Additional defects (VT6)

Alarm generation refers to the selected measurement channel.

1.9.4 VT6 Path Overhead evaluation

Display

- of the complete POH (hexadecimal)
- of the Trace Identifier (ASCII, plain text): J2

Output

- via DCC/ECC interface (V.11): Z6

1.9.5 VT6 error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements specified in Sec. 1.4.5, Page S-50:

Anomaly	LED
BIP-V	LP-BIP/BIP-V
REI-V	-

Table S-58 LED display of additional anomalies (VT6)

Evaluation and display refer to the selected measurement channel.

1.9.6 VT6 alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm detection specified in section 1.4.6 “STS-N alarm detection (defects)”:

Defect	LED
LOM	LOM
LOP-V	TU-LOP/LOP-V
AIS-V	TU-AIS/AIS-V
UNEQ-V	LP-UNEQ/UNEQ-V
PLM-V	LP-PLM/PLM-V
RDI-V	LP-RDI/RDI-V
TIM-V	-
RFI-V	-
PDI-V	-

Table S-59 LED display of additional defects (VT6)

Evaluation and display refer to the selected measurement channel.

1.10 Filler channel contents

Mapping structure like measurement channel, test pattern PRBS11.

2 Drop & Insert / Through Mode

Option BN 3035/90.20

2.1 Function

This option provides the following functions for all the mapping options included in the ANT-20SE.

Drop & Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

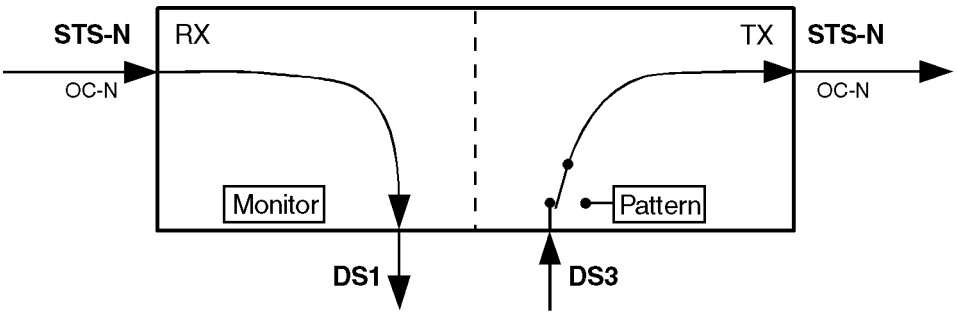


Fig. S-40 Drop & Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 2.2.1, Page S-73 and Sec. 2.3.1, Page S-74).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator. One tributary signal can be output (dropped).

The ANT-20SE can also operate in Through Mode as a signal monitor without affecting the signal content.

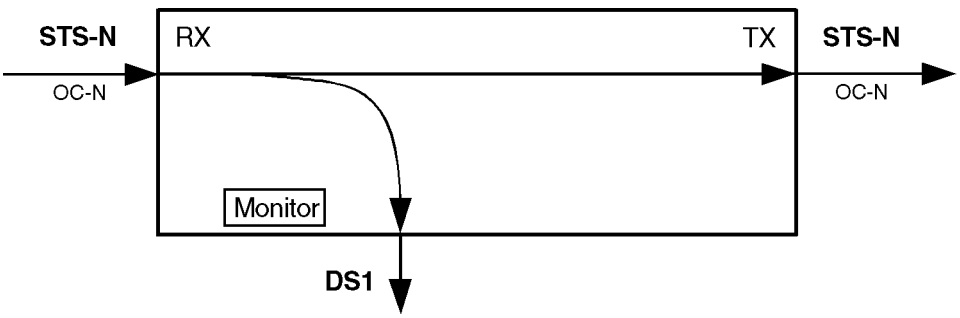


Fig. S-41 Through Mode: Generator and receiver coupled

In conjunction with the Options “PDH MUX/DEMUX” and “M13 MUX/DEMUX”, BN 3035/90.30 to BN 3035/90.32, the ANT-20SE provides access to the tributary channels within the MUX/DEMUX chain (except DS2). This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

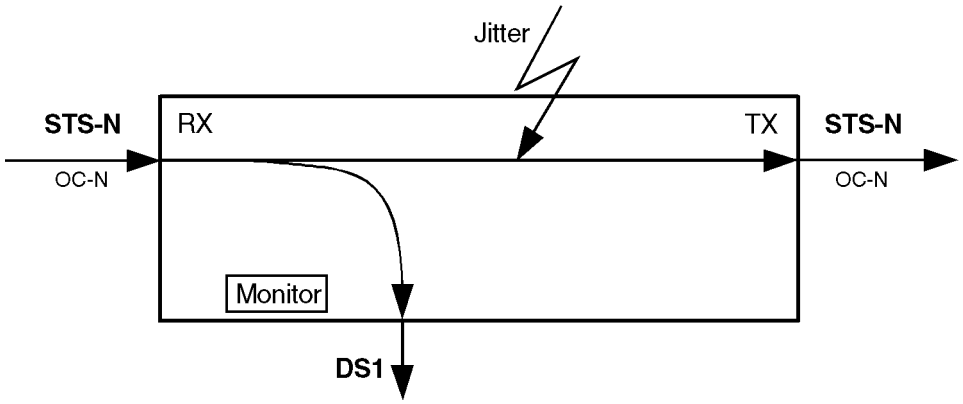


Fig. S-42 Through Mode: Adding jitter to the looped-through signal

In Through Mode, anomalies can be inserted in the SOH or the SOH bytes can be manipulated.

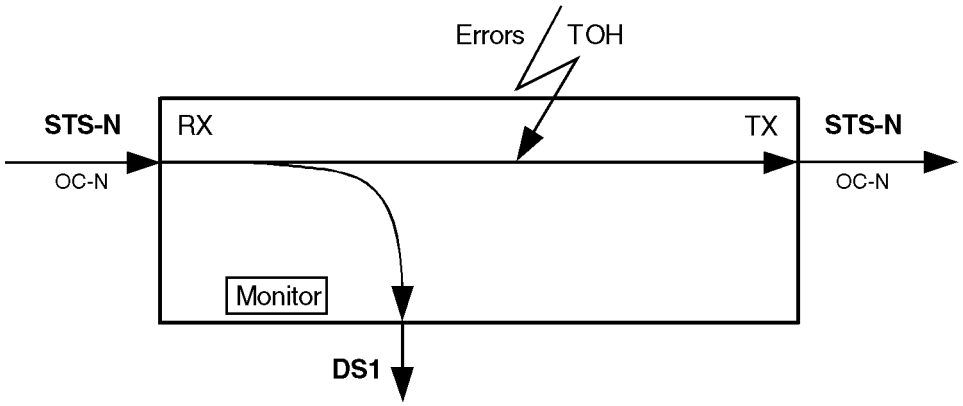


Fig. S-43 Through Mode: Inserting errors in the TOH

2.1.1 Clock generator

Drop & Insert

As specified in the “Specifications” of the mainframe instrument, section 1.2.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock.
No offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

2.1.2 Overhead generator

Drop & Insert

As specified in Sec. 1.4.1, Page S-44.

Through Mode

The “From Rx” function can be set in addition to the functions described in Sec. 1.4.1, Page S-44 for all bytes except bytes B1, B2 and M1.

Dynamic filling of the byte group D4 to D12 via DCC/ECC interface is not possible for STS-1.

2.1.3 Anomaly insertion

Drop & Insert

As specified in Sec. 1.4.2, Page S-46.

Through Mode

Anomaly insertion in bytes B1, B2 and REI-L.
Insertion limits are specified in Sec. 1.4.2, Page S-46.

2.1.4 Defect generation

Drop & Insert

As specified in Sec. 1.4.3, Page S-47.

Through Mode

No direct defect generation is possible.

Alarms (defects) in the TOH can be generated by manipulating the TOH bytes.

2.1.5 Pointer generation

Drop & Insert

As specified in Sec. 1.4.4, Page S-48.

Through Mode

The receive-side pointer is re-transmitted unchanged.

2.1.6 Measurements

There are no restrictions on measurements.
See Sec. 1.4.5, Page S-50 through Sec. 1.4.9, Page S-54.

2.2 Signal outputs

2.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
DS2	6.312	B8ZS	± 2.0 V
E1	2.048	HDB3	± 2.37 V
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-60 Specifications of the AUXILIARY signal output [11], electrical

2.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-61 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used both as “LINE” and as “AUXILIARY” output.

2.3 Signal inputs

2.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
DS2	6.312	B8ZS	2.0 V ±10 %
E1	2.048	HDB3	2.37 V ±10 %
DS1	1.544	B8ZS	
Available bitrates depending on mapping options			

Table S-62 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED is on if the signal input is active but no signal is present.

2.3.2 LINE/AUXILIARY signal output [12], electrical

Connector . . . . . balanced
Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-63 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED is on if the signal input is active but no signal is present.

The balanced input is used both as “LINE” and as “AUXILIARY” input.

Notes:

ANT-20SE
Advanced Network Tester

PDH MUX/DEMUX

BN 3060/90.11

Drop & Insert

BN 3060/90.10
in combination with
PDH MUX/DEMUX

Software Version 7.20

Specifications

Contents

Specifications PDH MUX DEMUX

Specifications PDH MUX DEMUX

Options BN 3035/90.30 to BN 3035/90.32

1 Generator section

1.1 Frame generator, 64k/140M PDH MUX/DEMUX Chain (option BN 3035/90.30)

The following frames are available:

Bit ratekbit/s	Frame conforming to:	Notes
2048	ITU-T G.704	PCM 30, PCM 30 CRC, PCM 31 and PCM 31 CRC systems
8448	ITU-T G.742	PCM 120 system
34368	ITU-T G.751	PCM 480 system
139264	ITU-T G.751	PCM 1920 system

Table S-1 Frame generation

The multiplexer chain (BN 3035/90.30) allows generation of a completely structured signal from 64 kbit/s to 140 Mbit/s.

1.2 Frame alignment signals

Frame alignment signals (FAS) corresponding to ITU-T recommendations G.751, G.742 and G.704.

1.2.1 Frame bit modifications

The following bits can be statically programmed:

PCM 1920 (G.751) . . . . . FAS bit nos. 13, 14, 15, 16

PCM 480, 120 (G.751, G.742) . . . . . FAS bit nos. 11, 12

PCM 30/31 (G.704) . . . . . NFAS bit nos. 3 through 8

PCM 30/31 CRC (G.704) . . . . . NFAS bit nos. 3 through 8

The following bits can be dynamically programmed:

PCM 30/ PCM 30 CRC (G.704). . . . . NFAS bit nos. 4 through 8 (S_a4 through S_a8)

Bits S_a4 thruogh S_a8 can be selected and each loaded with a freely programmable pattern 8 bits in length. This permits transmission of S_a sequences.

For PCM 30 / PCM 30 CRC systems, frame 0 or 1 in timeslot 16 can be loaded with a freely programmable 8 bit word. Frames 2 through 15 can be loaded with a further freely programmable 8 bit word.

1.2.2 CRC checksum (PCM 30 CRC / PCM 31 CRC)

The ANT-20SE calculates the CRC checksum for the measured channel and the filler channels as per ITU-T recommendation G.704 and inserts the result bits at the appropriate position in the pulse frame.

1.3 Justification as per ITU-T G.742 and G.751

The bit rates in the upper and subordinate systems are in a fixed relationship to each other.

Justification is at a nominal rate (offset of upper and subordinate systems is identical). Exception: Insertion of external signals.

Upper system bit rate in kbit/s	ITU-T	Justification ratio	Nominal justification rate in kbit/s
8448	G.742	0.42424	4.226
34368	G.751	0.43575	9.750
139264	G.751	0.41912	9.934

Table S-2 Justification

1.3.1 PDH tributary offset

Static offset for the PDH tributary bit rates during insertion into the SDH container.

Offset . . . . . ±100 ppm
for all bit rates, relative to SDH container
Step width . . . . . 1 ppm

The offset is an average value. The actual offset at any given time may be above or below this value.

1.4 Error insertion (anomalies)

In addition to the error types described in the “Specifications” for the mainframe instrument, the following anomalies can be inserted:

Error type, anomaly[1]	Single	Rate[2]
CRC-4	yes	2E-3 to 1E-8
E bit	yes	2E-3 to 1E-8

1 For PCM 30 CRC and PCM 31 CRC only
2 A CRC word error rate is inserted

Table S-3 Available error types (anomalies) in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

1.5 Alarm generation (defects)

The alarm types are described in the “Specifications” for the mainframe instrument.

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.6 Test signals for bit error rate measurements

1.6.1 Internal test signals

Bit patterns as in the mainframe instrument:

- Transmitted in all timeslots (framed pattern to ITU-T O.150/O.151)
- Transmitted in a selected timeslot

1.6.2 External signal (with option 3035/90.20 only)

An external signal with bit rate 34 368 kbit/s (coaxial), 8 448 kbit/s (coaxial) or 2 048 kbit/s (coaxial or balanced) can be inserted into the selected timeslot instead of the bit pattern (see Sec. 1.6.1).

The interfaces for this signal are described in the “Specifications” for the STM-1 mapping options.

1.6.3 Filler signals

Complete structured signals using the pseudo-random bit sequence PRBS 6 are transmitted in all timeslots except the selected timeslot in all 64 kbit/s channels.

2 Receiver section

2.1 Frame systems

Frames which can be evaluated by the 64k/140M PDH MUX/DEMUX chain and 64k/140M PDH DEMUX chain (options BN 3035/90.30 and 3035/90.31)

Bit rate kbit/s	Frame conforming to	Notes
2048	ITU-T G.704	PCM 30, PCM 31 systems
2048	ITU-T G.704/G.706	PCM 30 CRC, PCM 31 CRC systems
8448	ITU-T G.742	PCM 120 system
34368	ITU-T G.751	PCM 480 system
139264	ITU-T G.751	PCM 1920 system

Table S-4 Frame systems for individual system bit rates

All timeslots can be selected for all PCM frame structures. These may be speech or data channels in a primary rate system or the tributary channels in a justified multiplex system.

2.2 Evaluation

2.2.1 Frame bit evaluation

The following bits are evaluated and displayed:

PCM 1920 (G.751) . . . . . FAS bit nos. 13, 14, 15, 16

PCM 480, 120 (G.751, G.742). . . . . FAS bit nos. 11, 12

PCM 30/31 (G.7049) . . . . . NFAS bit nos. 1 through 8

PCM 30/31 CRC (G.704). . . . . NFAS bit nos. 2 through 8 (A bit, S_a4 through S_a8)

For PCM30/31 CRC systems, one of the bits S_a4 through S_a8 can be selected in order to display pattern sequences of up to 8 bits in length.

The D alarm bits (RDI alarms) are also evaluated and indicated by means of LEDs.
Also see in the ”Specifications” of the mainframe instrument.

2.2.2 CRC evaluations (PCM 30 CRC / PCM 31 CRC)

Errored CRC words are evaluated in the selected channel (CRC word error count).

The equivalent CRC bit error ratio is calculated from the CRC word error ratio.

The number of E bit errors is also converted to the equivalent bit error ratio.

2.3 Offset measurements

All offsets in the hierarchy stages in the measurement path are measured simultaneously and displayed.

Display in ppm

2.4 Error measurements (anomalies)

The error measurements are described in the “Specifications” for the mainframe instrument. The frame alignment signals in all hierarchy stages of the selected path are checked simultaneously.

2.5 Alarm detection (defects)

The detected alarms are described in the “Specifications” for the mainframe instrument. The RDI alarms in all hierarchy stages of the selected path are checked simultaneously.

2.6 Evaluation of test signals for bit error measurements

2.6.1 Internal evaluation

Evaluation:

- in all timeslots (framed pattern to ITU-T O.150/O.151)
- in the selected timeslot

2.6.2 External signal (with option 3035/90.20 only)

Output of a signal with bit rate 34 368 kbit/s (coaxial), 8 448 kbit/s (coaxial) or 2 048 kbit/s (coaxial or balanced) for external evaluation is alternative or simultaneous with internal evaluation (see Sec. 2.6.1).

The interfaces for this are described in the “Specifications” for the “STM-1 mapping” options.

3 Drop&Insert / Through Mode / Block&Replace

Option: BN 3035/90.20

3.1 Functions

This Option provides the following functions for all PDH multiplex options fitted to the ANT-20SE.

Drop&Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

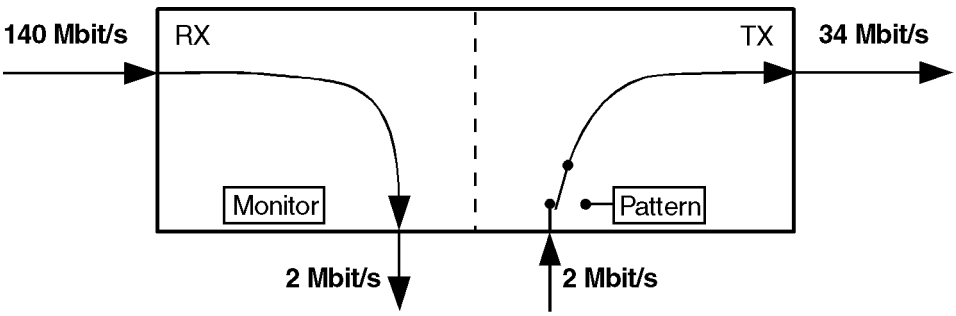


Fig. S-1 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 3.2.1, Page S-8 and Sec. 3.3.1, Page S-9).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator.

The ANT-20SE operates in Through Mode as a signal monitor without affecting the signal.

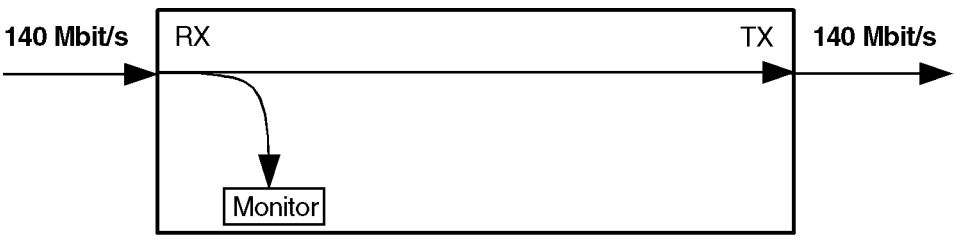


Fig. S-2 Through Mode: Generator and receiver coupled

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

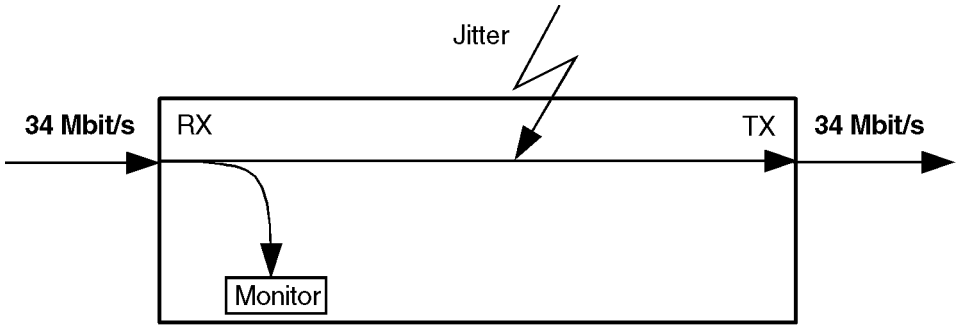


Fig. S-3 Through Mode: Adding jitter to the looped-through signal

Block&Replace

In PDH mode not possible.

3.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

3.1.2 Anomaly insertion

Drop&Insert

As specified in Sec. 1.4, Page S-3.

Through Mode

Anomaly insertion is not possible.

3.1.3 Defect generation

Drop&Insert

As specified in Sec. 1.5, Page S-3.

Through Mode

Defect generation is not possible.

3.1.4 Measurements

There are no restrictions on measurements (see Sec. 2, Page S-4).

3.2 Signal outputs

3.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-5 Specifications of the AUXILIARY signal output [11], electrical

3.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-6 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used as a LINE or as an AUXILIARY output.

3.3 Signal inputs

3.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

3.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used as a LINE or as an AUXILIARY input.

ANT-20SE
Advanced Network Tester

3

M13 MUX/DEMUX

BN 3060/90.12

Drop & Insert

BN 3060/90.10
in combination with
M13 MUX/DEMUX

Software Version 7.20

Specifications

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications M13 MUX/DEMUX

Notes:

Specifications M13 MUX DEMUX

Option BN 3035/90.32

1 Generator section

1.1 Frame generator, M13 MUX/DEMUX (option BN 3035/90.32)

The following frames are available:

Level	Bit rate in kbit/s	Frames conforming to	Notes
DS1	1544	T1.107	SF (D4)
	1544	T1.107	ESF (T1.107)
DS2	6312	T1.107	-
DS3	44736	T1.107	M13
	44736	T1.107a	C parity

Table S-1 Frame generation

The multiplexer chain (BN 3035/90.32) allows generation of a completely structured signal with 28 DS1 signals in a DS3 signal.
The DS2 level cannot be manipulated.

1.2 CRC checksum (DS1 ESF)

The ANT-20SE calculates the CRC-6 checksum for the measured channel and the filler channels as per standard T1.107 and inserts the result bits at the appropriate position in the Extended Super Frame.

1.3 Justification as per T1.107 or T1.107a

The bit rates in the upper and subordinate systems are in a fixed relationship to each other.

Justification is at a nominal rate (offset of upper and subordinate systems is identical). Exception: Insertion of external signals.

M13

Upper system	Justification ratio	Justification rate in kbit/s
DS2	0.335	1.8
DS3	0.39	3.544

Table S-2 M13 justification

C parity

Upper system	Justification ratio	Justification rate in kbit/s
DS2	0.073	0.393
DS3	1	9.398

Table S-3 C parity justification

1.3.1 PDH tributary offset

Static offset for the PDH tributary bit rates during insertion into the SONET-SPE container.

Offset . . . . . ±100 ppm
for all bit rates, relative to SONET-SPE container
Step width . . . . . 1 ppm

The offset is an average value. The actual offset at any given time may be above or below this value.

1.4 Error insertion (anomalies)

The error types are described in the “Specifications” for the mainframe instrument.

1.5 Alarm generation (defects)

The alarm types are described in the “Specifications” for the mainframe instrument.

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.6 Test signals for bit error rate measurements

1.6.1 Internal test signals

Bit patterns as in the mainframe instrument:

- Transmitted in all timeslots (framed pattern)
- Transmitted in a selected timeslot

1.6.2 External signal (with option 3035/90.20 only)

An external signal with bit rate 1544 kbit/s (coaxial or balanced) can be inserted into the selected timeslot instead of the bit pattern (see Sec. 1.6.1).

The interfaces for this signal are described in Sec. 3, Page S-6.

1.6.3 Filler signals

Complete structured signals using the pseudo-random bit sequence PRBS 6 are transmitted in all 64 kbit/s channels.

2 Receiver section

2.1 Frame systems

Frames which can be evaluated by the M13 MUX/DEMUX chain (Option BN 3035/90.32):

Level	Bit rate in kbit/s	Frames conforming to	Notes
DS1	1544	T1.107	SF (D4)
	1544	T1.107	ESF (T1.107)
DS2	6312	T1.107	-
DS3	44736	T1.107	M13
	44736	T1.107a	C parity

Table S-4 Frame systems for individual system bit rates

One channel is selected as test channel from the 28 DS1 signals.
The DS2 level cannot be evaluated.

2.2 Error measurements (anomalies)

The error measurements are described in the “Specifications” for the mainframe instrument. The frame alignment signals in all hierarchy stages of the selected path are checked simultaneously.

2.3 Alarm detection (defects)

The detected alarms are described in the “Specifications” for the mainframe instrument. The RDI alarms (yellow) in all hierarchy stages of the selected path are checked simultaneously.

2.4 Offset measurements

All offsets in the hierarchy stages of the selected path are measured and displayed simultaneously.

Display in ppm

2.5 Evaluation of test signals for bit error measurements

2.5.1 Internal evaluation

Evaluation:

- in all timeslots (framed pattern)
- in the selected timeslot

2.5.2 External signal (with option BN 3035/90.20 only)

Output of a signal with bit rate 1544 kbit/s (coaxial or balanced) for external evaluation is alternative to internal evaluation as described before (see Sec. 2.5.1).

The interfaces for this are described in Sec. 3, Page S-6.

3 Drop&Insert / Through Mode / Block&Replace

Option BN 3035/90.20

3.1 Functions

This option provides the following functions for all mapping options fitted to the ANT-20SE.

Drop&Insert

Generator and receiver operate independently as multiplexer and demultiplexer. The signal from a selected tributary is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

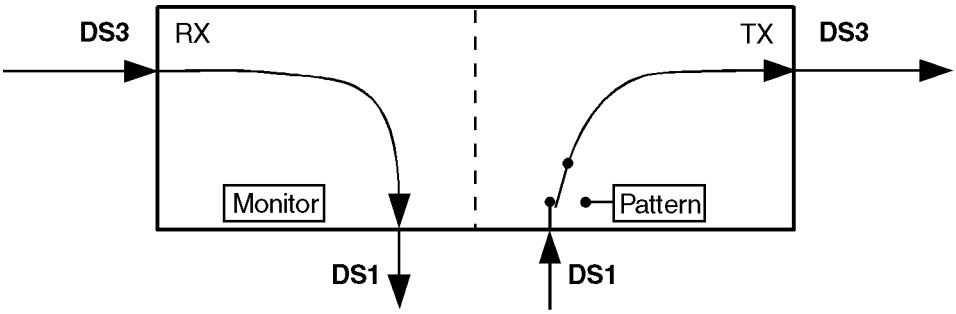


Fig. S-1 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 3.2.1, Page S-8 and Sec. 3.3.1, Page S-9).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator.

The ANT-20SE operates in Through Mode as a signal monitor without affecting the signal content.

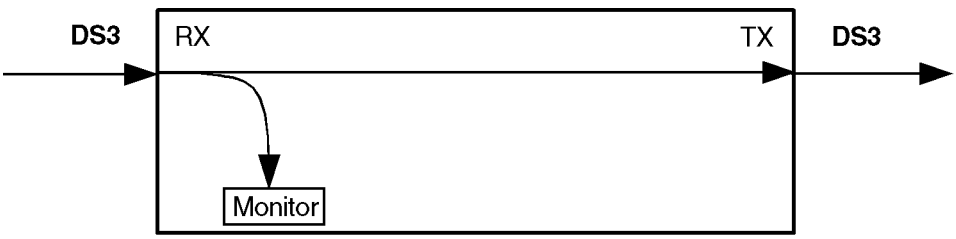


Fig. S-2 Through Mode: Generator and receiver coupled

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

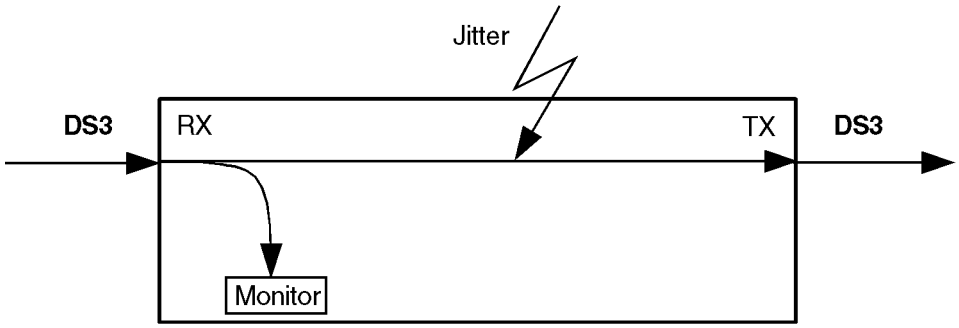


Fig. S-3 Through Mode: Adding jitter to the looped-through signal

Block&Replace

In PDH mode not possible.

3.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

3.1.2 Anomaly insertion

Drop&Insert

As specified in Sec. 1.4, Page S-2.

Through Mode

Anomaly insertion is not possible.

3.1.3 Defect generation

Drop&Insert

As specified in Sec. 1.5, Page S-2.

Through Mode

Defect generation is not possible.

3.1.4 Measurements

There are no restrictions on measurements (see Sec. 2, Page S-4).

3.2 Signal outputs

3.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-5 Specifications of the AUXILIARY signal output [11], electrical

3.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-6 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used as a LINE or as an AUXILIARY output.

3.3 Signal inputs

3.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

3.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used as a LINE or as an AUXILIARY input.

ANT-20SE
Advanced Network Tester

Optical Interfaces up to 155 Mbit/s
BN 3060/91.01 and BN 3060/91.02

Optical Interfaces up to 622 Mbit/s
BN 3060/91.11 and BN 3060/91.12

Optical Interfaces STM-16/OC-48
BN 3060/91.50 through BN 3060/91.53

Optical Interfaces STM-64/OC-192
BN 3060/91.40 through BN 3060/91.42

Drop&Insert
BN 3060/90.10
in combination with Optical Interfaces

Software Version 7.20

Specifications

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications STM-0/1/4/OC-1/3/12

Specifications STM-16/OC-48

Specifications STM-64/OC-192

Notes:

Specifications STM-0/1/4/OC-1/3/12

The numbers in square brackets […] correspond to the numbers printed on the instrument.

Calibrated specifications are indicated by ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [18], optical

Connector . . . . . 2.5 mm (PC)

"Fiber-to-fiber" adapter for direct connection to various 2.5 mm connector types . . . . . see list of accessories

Output level *** . . . . . 0 dBm +2/-3 dBm

Reduction in output level for 2 wavelength version . . . . . < 0.5 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . .1310 nm (1280 to 1330 nm)
1550 nm (1480 to 1580 nm)

Laser class to EN 60825-1:1994 1

The generator fulfills the requirements of ITU-T G.957, classes L1.1, L1.2, L1.3, L4.1, L4.2 and L4.3. The classes S1.1, S1.2 and S4.1 and S4.2 can be achieved by inserting an optical attenuator or the optical power splitter BN 3035/90.49.

LASER ON status display

LED is on when the laser source is active.

1.2 Clock generator and bit rates

1.2.1 Clock generation

See “Specifications” for the mainframe instrument.

1.2.2 Bit rates

The available bit rates depend on the options fitted.

STM-4, OC-12 . . . . . 622.08 Mbit/s

STM-1, OC-3 . . . . . 155.52 Mbit/s

STM-0, OC-1 . . . . . 51.84 Mbit/s

1.3 SDH and SONET TX signals

- Generates an STM-4 or STM-1 signal conforming to ITU-T-recommendation G.707.
- Generates an STM-0 signal conforming to ITU-RF.750-3.
- Generates an OC-12, OC-3 or OC-1 signal conforming to Bellcore recommendation GR-253.

1.3.1 STM-4 TX signal

STM-4 signal formation:

- STM-1 signal, generated internally x 4 (4 x AU-4 or 12 x AU-3)
- one STM-1 signal, generated internally (AU-4/AU-3), the other three tributaries loaded with HP-UNEQ
- one STM-1 signal, generated internally (AU-4/AU-3), the other three tributaries from the receiver
- complete STM-4 signal from receiver

1.3.2 STM-1 TX signal

STM-1 signal formation:

- STM-1 signal, generated internally
- complete STM-1 signal from receiver

1.3.3 STM-0 TX signal

STM-0 signal formation:

- STM-0 signal, generated internally
- complete STM-0 signal from receiver

1.3.4 OC-12 TX signal

OC-12 signal formation:

- STS-1 signal, generated internally x 12
- one STS-1 signal, generated internally, the other eleven tributaries loaded with UNEQ
- one STS-1 signal, generated internally, the other eleven tributaries from the receiver
- complete STS-12 from receiver
- STS-3c signal, generated internally x 4 (option BN 3035/90.70)
- one STS-3c signal, generated internally, the others loaded with UNEQ
- one STS-3c signal, generated internally, the others from the receiver

1.3.5 OC-3 TX signal

OC-3 signal formation:

- STS-3 signal, generated internally
- complete STS-3 signal from receiver

OC-3c signal formation: (option BN 3035/90.70)

- STS-3c signal, generated internally
- complete STS-3c signal from receiver

1.3.6 OC-1 TX signal

OC-1 signal formation:

- STS-1 signal, generated internally
- complete STS-1 signal from receiver

1.3.7 Scrambling

Scrambling is as per ITU-T recommendation G.707.
The scrambler can be switched on or off.

1.3.8 Overhead generator

1.3.8.1 Section overhead (SOH), Transport Overhead (TOH)

STM-4, OC-12 standard overhead (hex)

	S O H, TOH																																			
1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	J0 C1	Z0 C1	Z0 C1	Z0 C1	—	—	—	—	—	—	—	—
	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	28	28	28	28	28	28	28	28	28	28	28	28	01	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
2	B1	—	—	—	—	—	—	—	—	—	—	—	E1	—	—	—	—	—	—	—	—	—	—	—	F1	—	—	—	—	—	—	—	—	—	—	—
	XX	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
3	D1	—	—	—	—	—	—	—	—	—	—	—	D2	—	—	—	—	—	—	—	—	—	—	—	D3	—	—	—	—	—	—	—	—	—	—	—
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
4a	H1	H1	H1	H1	Y	Y	Y	Y	Y	Y	Y	Y	H2	H2	H2	H2	—	—	—	—	—	—	—	—	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
	68	68	68	68	9B	9B	9B	9B	9B	9B	9B	9B	00	00	00	00	FF	FF	FF	FF	FF	FF	FF	FF	00	00	00	00	00	00	00	00	00	00	00	00
4b	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
	68	68	68	68	68	68	68	68	68	68	68	68	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
4c	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
	60	60	60	60	60	60	60	60	60	60	60	60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
4d	H1	H1	H1	H1	Y	Y	Y	Y	Y	Y	Y	Y	H2	H2	H2	H2	—	—	—	—	—	—	—	—	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
	60	60	60	60	93	93	93	93	93	93	93	93	00	00	00	00	FF	FF	FF	FF	FF	FF	FF	FF	00	00	00	00	00	00	00	00	00	00	00	00
5	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	K1	—	—	—	—	—	—	—	—	—	—	—	K2	—	—	—	—	—	—	—	—	—	—	—
	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
6	D4	—	—	—	—	—	—	—	—	—	—	—	D5	—	—	—	—	—	—	—	—	—	—	—	D6	—	—	—	—	—	—	—	—	—	—	—
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
7	D7	—	—	—	—	—	—	—	—	—	—	—	D8	—	—	—	—	—	—	—	—	—	—	—	D9	—	—	—	—	—	—	—	—	—	—	—
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
8	D10	—	—	—	—	—	—	—	—	—	—	—	D11	—	—	—	—	—	—	—	—	—	—	—	D12	—	—	—	—	—	—	—	—	—	—	—
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
9	S1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z2	Z2	M1	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	E2	—	—	—	—	—	—	—	—	—	—	—
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Table S-1 SOH, TOH content; STM-4, OC-12

XX: Inserted by parity formation (B1, B2)

Line 4a: SDH pointers (AU-4)

Line 4b: SDH pointers (AU-3)

Line 4c: SONET pointers (STS-1 SPE)

Line 4d: SONET pointers (STS-3c)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

SOH byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11: E1, F1, E2 (single byte)
- Dynamic byte groups with pseudo random bit sequence PRBS11: D1 to D3, D4 to D12 (byte group)
- Dynamic bytes via DCC/ECC interface, Socket [21] (V.11): E1, F1, E2 (single byte)
- Dynamic byte groups via DCC/ECC interface, Socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

STM-1, STM-0, OC-3, OC-1 standard overhead

See separate operating manual “STM-1 mappings/STS-1 mappings”.

1.3.9 Error insertion (anomalies)

The following anomalies can be inserted in addition to those in the mainframe instrument:

Anomaly	Single	Rate	Burst m, n (frames)
B1 (STM-4, OC-12)	yes	2E-4 to 1E-10	m = 1 to 196000
B2 (STM-4, OC-12)	yes	2E-3 to 1E-10	m = 1 to 196000
MS-REI (STM-4) REI-L (OC-12)	yes	2E-3 to 1E-10	m = 1 to 196000

Table S-2 Available anomalies in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

1.3.10 Alarm generator (defects)

The following defects can be generated in addition to those in the mainframe instrument:

Defect	**Test sensor function**	**Test sensor thresholds**	
-	On/Off	M in N	|---t1---| |------t2------|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-622	yes	M = 1 to N - 1 N = 1 to 8000[1]	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RS-TIM (STM-4) TIM-L (OC-12)	yes	-	-
MS-AIS (STM-4) AIS-L (OC-12)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
MS-RDI (STM-4) RDI-L (OC-12)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

1 Included with options 3035/90.46, 3035/90.47 and 3035/90.48

Table S-3 Available defects in addition to the mainframe instrument

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.4 Output signals for the ADM Tester

1.4.1 Optical output signal

The available bit rates depend on the options fitted.

STM-4, OC-12 . . . . . 622.08 Mbit/s

STM-1, OC-3 . . . . . 155.52 Mbit/s

STM-0, OC-1 . . . . . 51.84 Mbit/s

Signal structure

Frame alignment signal . . . . . n x A1, n x A2

Parity formation B1, B2, B3

Section overhead, Transport Overhead . . . . . Standard overhead,
see Sec. 1.3.8, Page S-4
and “STM-1 Mappings/STS-1 Mappings”
operating manual

Pointer value . . . . . “0”

Matching of “ss” bits to STM-x/AU-4
STM-x/AU-3
OC-x

Path overhead and payload . . . . . HP-UNEQ (all zeros)

Possible modifications

Laser is switchable . . . . . ON/OFF

Wavelength is selectable . . . . . 1310 nm, 1550 nm

Scrambler is permanently . . . . . ON

- No frequency offset possible
- No overhead modifications possible
- No pointer actions

1.4.2 PDH output signal

The PDH output signal can be set as for normal operation. There are no restrictions.

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [17], optical

Connector . . . . . 2.5 mm (PC)

"Fiber-to-fiber" adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Input sensitivity
STM-1 / OC-3 ***, STM-0 / OC-1. . . . . -8 to -28 dBm
STM-4 / OC-12 *** . . . . . -8 to -28 dBm

Max. permitted input level . . . . . +2 dBm

Wavelength . . . . . 1100 to 1580nm

The receiver meets the requirements of ITU-T G.957 classes S1.1, S1.2, S4.1, S4.2 and S4.3.

Tolerance to jitter

measured using scrambled SDH or SONET signals:

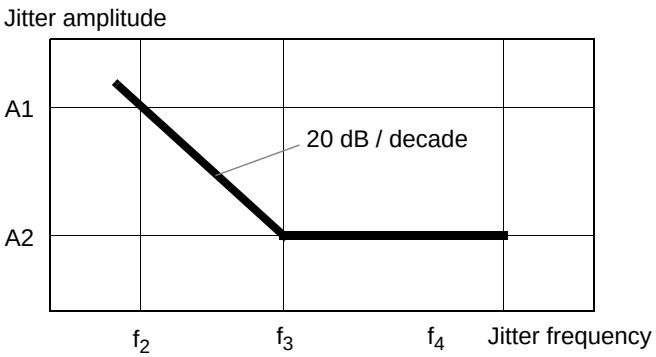


Fig. S-1 Relationship between jitter amplitude and jitter frequency

Bit rate Mbit/s	A1 UIpp	f_2 kHz	A2 UIpp	f_3 kHz	f_4 kHz
51.840	1.5	2	0.15	20	500
155.520	1.5	6.5	0.15	65	1300
622.080	1.5	25	0.15	250	5000

Table S-4 Tolerance to jitter at system bit rates for the ANT-20SE

Optical signal level display

Resolution . . . . . 1 dBm

Accuracy. . . . . ±1 dBm

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

Note: The high sensitivity of the optical input may cause LOF to be detected instead of LOS with some systems. This is due to incomplete blanking of the laser source (system or ANT-20SE).
One way of testing laser blanking despite this problem is to insert an additional optical attenuator in front of the input. This attenuates any residual light so that the level is below the LOS threshold.

LOS threshold . . . . . < -30 dBm

2.1.2 Signal input [16], electrical

Connector. . . . . unbalanced (coaxial)

Socket type. . . . . .SMA

Input impedance. . . . . .50 Ω
ab Serie AG . . . . . Eingangswiderstand für ECL-Signale vorhanden

Line code . . . . . .NRZ (scrambled)

Input voltage range. . . . . .200 mVpp to 1Vpp

Bit rate . . . . . 155.52 Mbit/s; 622.08 Mbit/s

Tolerance to jitter

As stated in Tab. S-4, Page S-8

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

2.1.3 Clock recovery

See “Specifications” for the mainframe instrument.

2.2 SDH and SONET RX signals

- Evaluation of STM-4 or STM-1 signal conforming to ITU-T recommendation G.707.
- Evaluation of STM-0 signal conforming to ITU-RF.750-3.
- Evaluation of OC-12, OC-3 or OC-1 signal conforming to the Bellcore GR-253 standard.

2.2.1 STM-4 RX signal

STM-4 signal evaluation:

- Analysis of section overhead (SOH) and demultiplexing of one channel, further analysis in mainframe
- Analysis of section overhead (SOH) and loop-through of STM-4 signal to transmitter

2.2.2 STM-1 RX signal

STM-1 signal evaluation:

- takes place in the mainframe.

2.2.3 STM-0 RX signal

STM-0 signal evaluation:

- takes place in the mainframe.

2.2.4 OC-12 RX signal

OC-12 signal evaluation:

- Analysis of transport overhead (TOH) and demultiplexing of one channel, further analysis in mainframe
- Analysis of transport overhead (TOH) and loop-through of OC-12 signal to transmitter

2.2.5 OC-3 RX signal

OC-3 signal evaluation:

- takes place in the mainframe.

OC-3c signal evaluation:

- takes place in the mainframe.

2.2.6 OC-1 RX signal

OC-1 signal evaluation:

- takes place in the mainframe.

2.2.7 Descrambling

Descrambling is as per ITU-T recommendation G.707.
The descrambler can be switched on or off.

Tip: In the case of unscrambled input signals make sure that there are no longer sequences with HIGH logical or LOW logical bits in the data stream.

2.3 Measurement modes

2.3.1 Alarm detection (defects)

The following alarms can be evaluated and displayed in addition to the alarm detection functions given in the mainframe instrument:

Defect	**LED**
LOS (optical)	LOS
LOF-622	LOF/OOF
RS-TIM (STM-4) TIM-L (OC-12)	-
MS-AIS (STM-4) AIS-L (OC-12)	MS-AIS/AIS-L
MS-RDI (STM-4) RDI-L (OC-12)	MS-RDI/RDI-L

Table S-5 LED displays for additional defects

2.3.2 Error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements given in the mainframe instrument:

Anomaly	**LED**
OOF-622	LOF/OOF
B1(STM-4, OC-12)	B1/B2
B2 (STM-4, OC-12)	B1/B2
MS-REI (STM-4) REI-L (OC-12)	-

Table S-6 LED displays for additional anomalies

Evaluation and display of B2 errors (STM-4, OC-12) refers to all test channels taken together.

2.3.3 Section overhead (SOH) and transport overhead (TOH) evaluation

Display

• complete SOH, TOH	hexadecimal (four channel-oriented partial SOHs/TOHs)
• Trace Identifier J0 (STM-4/OC-12)	ASCII, plain text

Evaluation

Bit error measurement

• bytes with pseudo random bit sequence PRBS11	E1, F1, E2 (single byte)
• byte groups with pseudo random bit sequence PRBS11	D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output

• in bytes via DCC/ECC interface, socket [21] (V.11)	E1, F1, E2 (single byte)
• in byte groups via DCC/ECC interface, socket [21] (V.11)	D1 to D3, D4 to D12, K1 to K2 (byte group)

3 Optical power splitter BN 3035/90.49

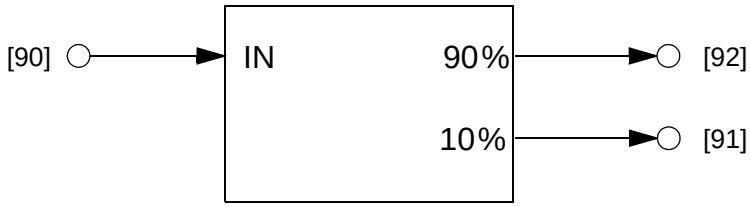


Fig. S-2 Optical Power Splitter

3.1 Wavelength ranges

"1310 nm" . . . . . 1260 to 1360 nm

"1550 nm" . . . . . 1500 to 1600 nm

3.2 Attenuation

Between "IN" [90] and "90%" [92]. . . . . 1.0 dB (typically), < 1.6 dB

Between "IN" [90] and "10%" [91]. . . . . 10.5 dB (typically), 8.8 to 12.0 dB

4 Drop&Insert / Through Mode / Block&Replace

Option: BN 3035/90.20

4.1 Functions

This option provides the following functions for all mapping options fitted to the ANT-20SE.

Drop&Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

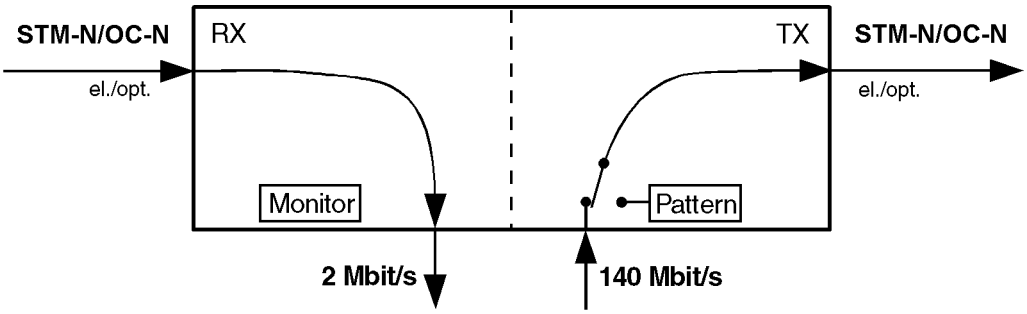


Fig. S-3 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 4.3.1, Page S-20 and Sec. 4.2.1, Page S-19).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator. One tributary signal can be output (dropped).

The ANT-20SE can also operate in Through Mode as a signal monitor without affecting the signal content.

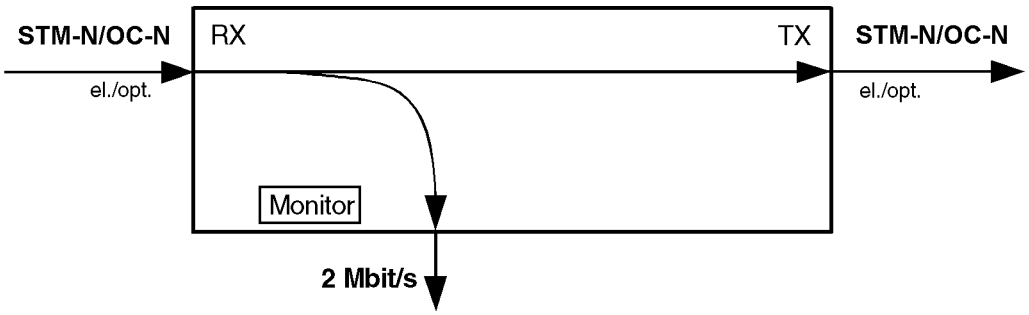


Fig. S-4 Through Mode: Generator and receiver coupled

In conjunction with the options “PDH MUX/DEMUX” and “M13 MUX/DEMUX”, BN 3035/90.30 to BN 3035/90.32, the ANT-20SE provides access to the tributary channels within the MUX/DEMUX chain. This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

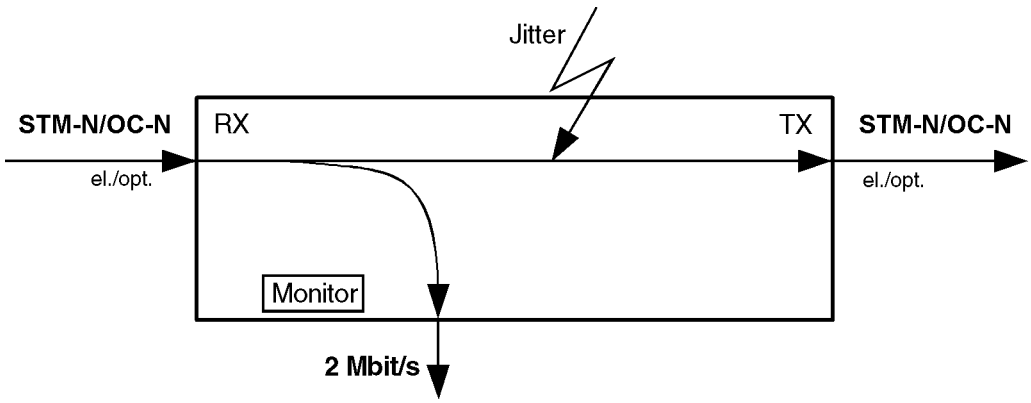


Fig. S-5 Through Mode: Adding jitter to the looped-through signal

In Through Mode, anomalies can be inserted in the SOH/TOH or the SOH/TOH bytes can be manipulated.

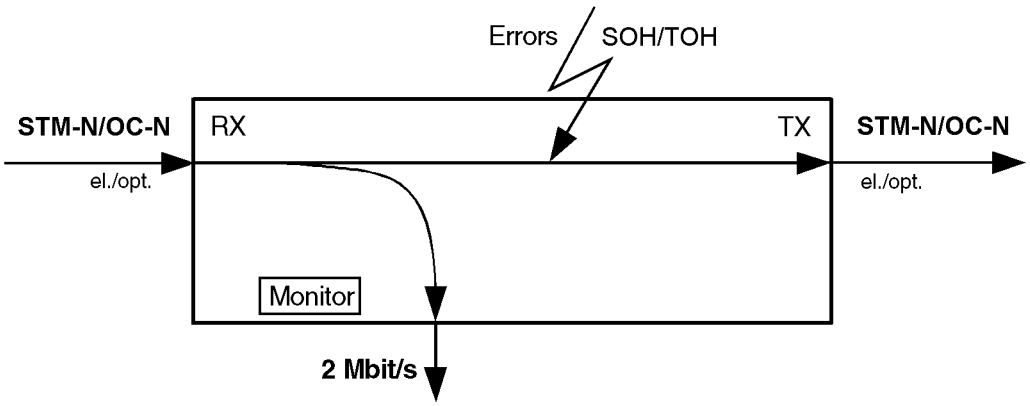


Fig. S-6 Through Mode: Inserting errors in the SOH/TOH

Block&Replace

Only possible with SDH C4 and C3 mapping and SONET STS3c and STS1 SPE mapping.

The transmitter and receiver are coupled. The received signal is looped through from the receiver to the transmitter. The ANT-20SE is used as a test channel monitor on the receive side. The test channel is reconstructed on the transmit side.

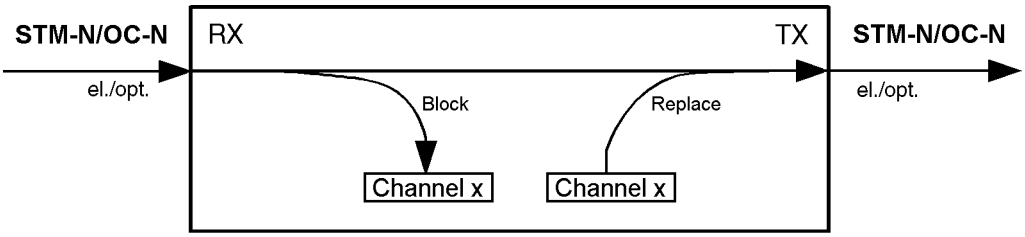


Fig. S-7 Block&Replace: Transmitter and receiver coupled

Jitter can be superimposed on the received signal in through mode when the “Jitter Generator up to 155 Mbit/s” or “Jitter generator up to 622 Mbit/s” options BN 3035/90.60 to 61 are used. This applies to all bit rates available in the instrument.

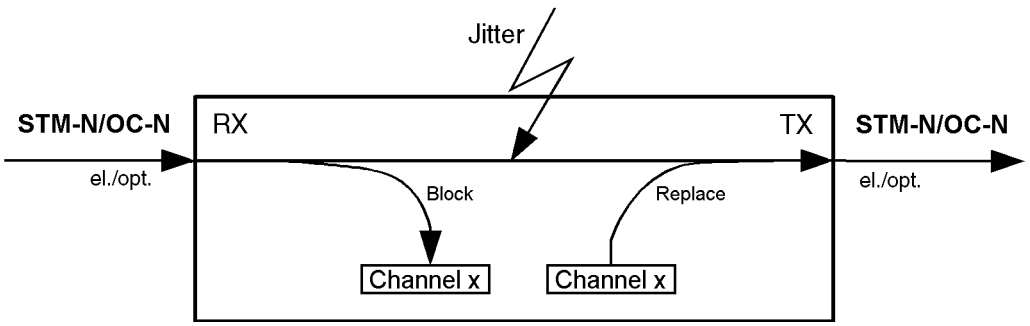


Fig. S-8 Block&Replace: Jittered through signal

Anomalies can be inserted in the SOH/TOH or the bytes manipulated in Block&Replace mode.

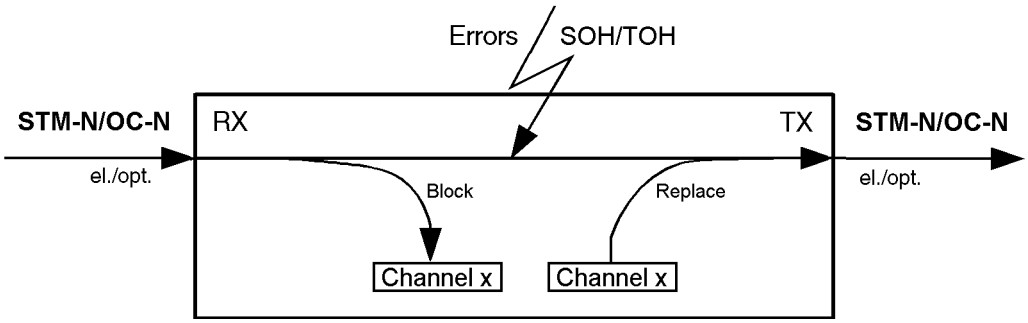


Fig. S-9 Block&Replace: Error insertion into the SOH/TOH

4.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock.
No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

4.1.2 Overhead generator

Drop&Insert

As specified in Sec. 1.3.8, Page S-4.

Through Mode

The “From Rx” function can be set in addition to the functions described in Sec. 1.3.8, Page S-4 for all bytes except bytes B1, B2 and M1.

4.1.3 Anomaly insertion

Drop&Insert

As specified in Sec. 1.3.9, Page S-5.

Through Mode

Anomaly insertion in bytes B1, B2 and MS-REI/REI-L.
Insertion limits are specified in Sec. 1.3.9, Page S-5.

4.1.4 Defect generation

Drop & Insert

As specified in Sec. 1.3.10, Page S-6.

Through Mode

No direct defect generation is possible.

Tip: Alarms (defects) in the SOH/TOH can be generated by manipulating the SOH bytes.

4.1.5 Measurements

There are no restrictions on measurements. See Sec. 2.3, Page S-11.

4.2 Signal outputs

4.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the AUXILIARY signal output [11], electrical

4.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used both as “LINE” and as “AUXILIARY” output.

4.3 Signal inputs

4.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-9 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

4.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . .balanced

Socket type . . . . . .Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-10 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used both as “LINE” and as “AUXILIARY” input.

Notes:

Specifications STM-16/OC-48

The numbers in square brackets […] correspond to the numbers printed on the instrument.

Calibrated specifications are indicated by ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [47], optical

Connector . . . . . 2.5 mm (PC)

"Fiber-to-fiber" adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Output level *** . . . . . 0 dBm +0/-2 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . 1310 nm (1285 to 1340 nm)
1550 nm (1520 to 1600 nm)

Laser class to EN 60825-1:1994,
Normal operation 1
Fault condition 3A

The generator fulfils the requirements of ITU-T G.957, classes S16.2, L16.2, L16.3 or S16.1, L16.1.

LASER ON status display

LED is on when the laser source is active.

1.1.2 Signal output [46], electrical

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Signal output impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Output voltage . . . . . ≥ 500 mVpp

Bit rate . . . . . 2488.32 Mbit/s

1.2 Clock generator and bit rates

1.2.1 Clock generation internal

See “Specifications” for the mainframe instrument.

Permissible clock offset . . . . . ±50 ppm

1.2.2 Clock generation external [45]

For feeding in a jitter-modulated clock signal that must be derived from the base module clock.

Clock frequency . . . . . 2488.32 Mbit/s

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Clock input impedance . . . . . 50 Ω

Input voltage range . . . . . .300 mVpp to 1 Vpp

1.2.3 Bit rate

STM-16, OC-48 . . . . . 2488.32 Mbit/s

1.2.4 Clock output [41]

For the Generator clock

Frequency . . . . . 2488.32 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 300 mVpp

1.3 SDH and SONET TX signals

- Generates an STM-16 signal conforming to ITU-T recommendation G.707.
- Generates an OC-48 signal conforming to the Bellcore-GR-253 and ANSI T1.105 standards.

1.3.1 STM-16 TX signal

STM-16 signal formation:

- STM-1 signal, generated internally x 16 (16 x AU-4 or 48 x AU-3)
- one STM-1 signal, generated internally (AU-4/AU-3), the other 15 tributaries loaded with HP-UNEQ
- one STM-1 signal, generated internally (AU-4/AU-3), the other 15 tributaries from the receiver

STM-16c signal formation:

- complete STM-16 signal from receiver

1.3.2 OC-48 TX signal

OC-48 signal formation:

- STS-1 signals, generated internally and STS-1 signals loaded with UNEQ
- STS-3c signal, generated internally x 16
- one STS-3c signal, generated internally, the other 15 tributaries loaded with UNEQ
- STS-1 signals generated internally, the other 47 tributaries loaded with UNEQ
- STS-48 signal from receiver
- one STS-3c signal, generated internally, the other 15 tributaries from the receiver

1.3.3 Scrambling

Scrambling is as per ITU-T recommendation G.707.
The scrambler cannot be switched off.

1.3.4 Overhead generator

1.3.4.1 Section overhead (SOH), Transport overhead (TOH)

STM-16, OC-48 standard overhead (hex)

See Tab. S-1, Page S-27.

Settings are only possible in SOH #1 or TOH #1.
This excludes the A1, A2, B1 and B2 bytes and the complete pointer line (H1, H2, H3).

XX: Inserted by parity formation (B1, B2)

Line 4a: SDH pointers (AU-4)

Line 4b: SDH pointers (AU-3)

Line 4c: SONET pointers (STS-1 SPE)

Line 4d: SONET pointers (STS-3c)

Line 9: Z1 and Z2 are used for SONET only

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

Overhead byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11 (only possible if channel #1of the STM-N-/OC signal is selected): D1 to D3, D4 to D12 (byte group)
- Dynamic via DCC/ECC interface socket [40] (V.11): E1, F1, E2 (single byte)
- Dynamic via DCC/ECC interface socket [40] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

STM-1, OC-3, OC-1 standard overhead

See Operating Manual “STM-1 mappings/STS-1 mappings”.

SOH, TOH																																
SOH	#1	#2	#3	...	#16	#1	...	#1	...	#1	...	#1	#2	#3	#4	...	#1	...	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	#1	...	#1	...	#16
1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	A2 28	J0 C1 01	Z0 C1 02	Z0 C1 03	Z0 C1 04	Z0 C1 05	Z0 C1 06	Z0 C1 07	Z0 C1 08	Z0 C1 09	Z0 C1 0A	Z0 C1 0B	Z0 C1 0C	Z0 C1 0D	Z0 C1 0E	Z0 C1 0F	Z0 C1 10	-- -- AA	-- -- AA	-- -- AA	-- -- AA
2	B1 XX	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	F1 00 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
3	D1 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	D3 00 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
4a	H1 68	H1 68	H1 68	H1 68	H1 68	Y 9B	H1 68	-- -- FF	-- -- FF	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4b	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4c	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4d	H1 60	H1 60	H1 60	H1 60	H1 60	Y 93	H1 60	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	-- -- 00	-- -- 00	-- -- 00	K2 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
6	D4 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	D5 00	-- -- 00	-- -- 00	-- -- 00	D6 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
7	D7 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	D8 00	-- -- 00	-- -- 00	-- -- 00	D9 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
8	D10 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	D11 00	-- -- 00	-- -- 00	-- -- 00	D12 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00
9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	Z2 00	E2 00	Z2 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00	-- -- 00

Table S-1 SOH, TOH contents; STM-16, OC-48

1.3.5 Error insertion (anomalies)

The following anomalies can be inserted in addition to those in the mainframe instrument:

Anomaly	Single	Rate	Burst m, n (frames)
B1 (STM-16, OC-48)	yes	1E-8 to 2E-5	m = 1 to 196000
B2 (STM-16, OC-48)	yes	1E-8 to 1E-3	m = 1 to 196000
MS-REI (STM-16) REI-L (OC-48)	yes	1E-8 to 1E-3	m = 1 to 196000

Table S-2 Available anomalies in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

1.3.6 Alarm generator (defects)

The following defects can be generated in addition to those in the mainframe instrument:

Defect	Test sensor function	Test sensor thresholds	
-	On/Off	M in N	|----t1----| |-----t2-----|
LOS (optical)	yes	M =800 to 7200 N= 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-2488	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RS-TIM (STM-16) TIM-L (OC-48)	yes	-	-
MS-AIS (STM-16) AIS-L (OC-48)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
MS-RDI (STM-16) RDI-L (OC-48)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-3 Available defects in addition to the mainframe instrument

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.4 Output signals for the ADM Tester

1.4.1 Optical output signal

STM-16, OC-48 . . . . . 2488.32 Mbit/s

Signal structure

Frame alignment signal . . . . . 48 x A1, 48 x A2

Parity formation B1, B2, B3

Section overhead, transport overhead . . . . . Standard overhead, see Sec. 1.3.4, Page S-26

Pointer value . . . . . “0”

Matching of “ss” bits to STM-x/AU-4
STM-x/AU-3
OC-x

Path overhead and payload . . . . . HP-UNEQ (all zeros)

Possible modifications

Laser is switchable . . . . . ON/OFF

Switchable wavelength (depending on option fitted) . . . . . 1310 nm or 1550 nm

Scrambler is permanently . . . . . ON

- No frequency offset possible
- No overhead modifications possible
- No pointer actions

1.4.2 PDH output signal

The PDH output signal can be set as for normal operation. There are no restrictions.

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [44], optical

Caution

Destruction of input [44]

The maximum input level of -8 dBm must not be exceeded. Otherwise, the optical input can be destroyed.

⇒ Insert an optical attenuator in any case:
- – for RX - TX loop operation
- – for higher input levels

Connector . . . . . 2.5 mm (PC)

“Fiber-to-fiber” adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Input sensitivity
STM-16 / OC-48 *** . . . . . -8 to -28 dBm

Max. permitted input level . . . . . -8 dBm

Wavelength . . . . . 1100 to 1600 nm

The receiver meets the requirements of ITU-T G.957 classes S16.2, L16.2, L16.3 or S16.1 and L16.1.

Optical signal level display

Resolution . . . . . 1 dBm

Accuracy . . . . . ±3 dB

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

LOS threshold . . . . . < -30 dBm

2.1.2 Signal input [43], electrical

Connector . . . . . unbalanced (coaxial)

Socket type . . . . . SMA

Input impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Input voltage range . . . . . 300 mVpp to 1Vpp

Bit rate . . . . . 2488.32 Mbit/s

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

2.1.3 Clock output [42]

For the recovered receive clock

Frequency . . . . . 2488.32 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 100 mVpp

2.2 SDH and SONET RX signals

- Evaluation of STM-16 signal conforming to ITU-T recommendation G.707.
- Evaluation of OC-48 signal conforming to Bellcore GR-253 and ANSI T1.105 standards.

2.2.1 STM-16 RX signal

STM-16 signal evaluation:

- Analysis of SOH and demultiplexing of one channel, further analysis in mainframe
- Analysis of SOH and loop-through of STM-16 signal to transmitter

2.2.2 OC-48 RX signal

OC-48 signal evaluation:

- Analysis of TOH and demultiplexing of one channel, further analysis in mainframe
- Analysis of TOH and loop-through of OC-48 signal to transmitter

2.2.3 Descrambling

Descrambling is as per ITU-T recommendation G.707.
The descrambler cannot be switched off.

2.3 Measurement modes

2.3.1 Alarm detection (defects)

The following alarms can be evaluated and displayed in addition to the alarm detection functions given in the mainframe instrument:

Defect	**LED**
LOS (optical)	LOS
LOF-2488	LOF/OOF
RS-TIM (STM-16) TIM-L (OC-48)	-
MS-AIS (STM-16) AIS-L (OC-48)	MS-AIS/AIS-L
MS-RDI (STM-16) RDI-L (OC-48)	MS-RDI/RDI-L

Table S-4 LED displays for additional defects

2.3.2 Error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements given in the mainframe instrument:

Anomaly	**LED**
OOF-2488	LOF/OOF
B1 (STM-16, OC-48)	B1/B2
B2 (STM-16, OC-48)	B1/B2
MS-REI (STM-16) REI-L (OC-48)	-

Table S-5 LED displays for additional anomalies

Evaluation and display of B2 errors (STM-16, OC-48) refers to all test channels taken together.

2.3.3 Section overhead (SOH) #1, Transport overhead (TOH) #1 evaluation

Display

- SOH #1, TOH #1 — hexadecimal
  Except: A1, A2, B1, B2, H1 to H3
- Trace Identifier J0 (STM-16, OC-48) — ASCII, plain text

Evaluation

Bit error measurement

- With PRBS11 pseudo-random sequence (only if channel #1 of the STM-N-/OC signal is selected): — D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output

- in bytes via DCC/ECC interface, socket [40] (V.11): — E1, F1, E2 (single byte)
- in byte groups via DCC/ECC interface, socket [40] (V.11): — D1 to D3, D4 to D12, K1 to K2 (byte group)

3 Optical power splitter BN 3035/90.49

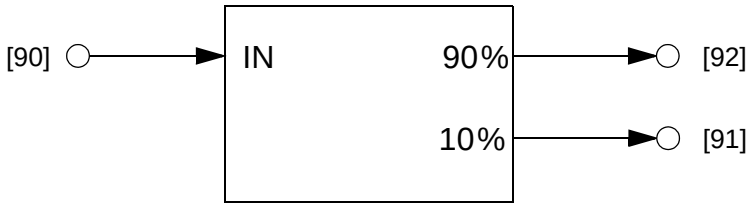


Fig. S-1 Optical Power Splitter

3.1 Wavelength ranges

"1310 nm" . . . . . 1260 to 1360 nm

"1550 nm" . . . . . 1500 to 1600 nm

3.2 Attenuation

Between "IN" [90] and "90%" [92]. . . . . 1.0 dB (typically), < 1.6 dB

Between "IN" [90] and "10%" [91]. . . . . 10.5 dB (typically), 8.8 to 12.0 dB

4 Drop&Insert / Through Mode

Option: BN 3035/90.20

4.1 Functions

This option provides the following functions for all mapping options fitted to the ANT-20SE.

Drop&Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

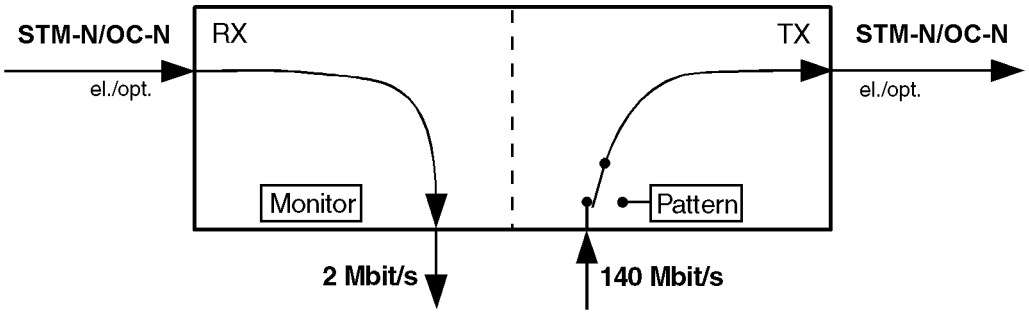


Fig. S-2 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 4.3.1, Page S-40 and Sec. 4.2.1, Page S-39).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20SE and re-transmitted by the generator. One tributary signal can be output (dropped).

The ANT-20SE can also operate in Through Mode as a signal monitor without affecting the signal content.

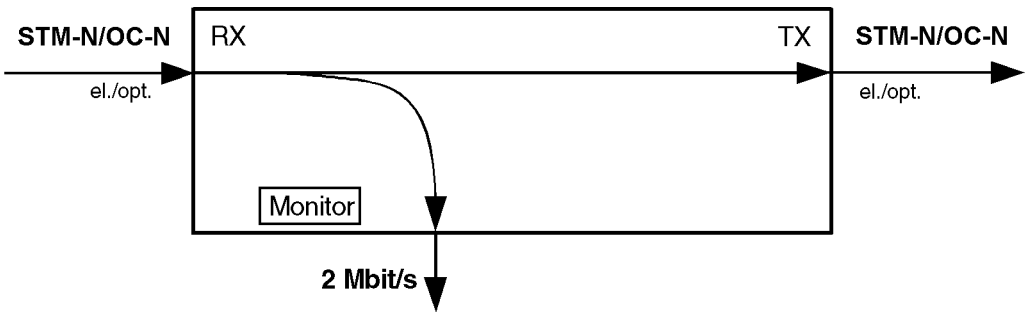


Fig. S-3 Through Mode: Generator and receiver coupled

In conjunction with the options “PDH MUX/DEMUX” and “M13 MUX/DEMUX”, BN 3035/90.30 to BN 3035/90.32, the ANT-20SE provides access to the tributary channels within the MUX/DEMUX chain. This also applies if the PDH signal is transmitted in a container.

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

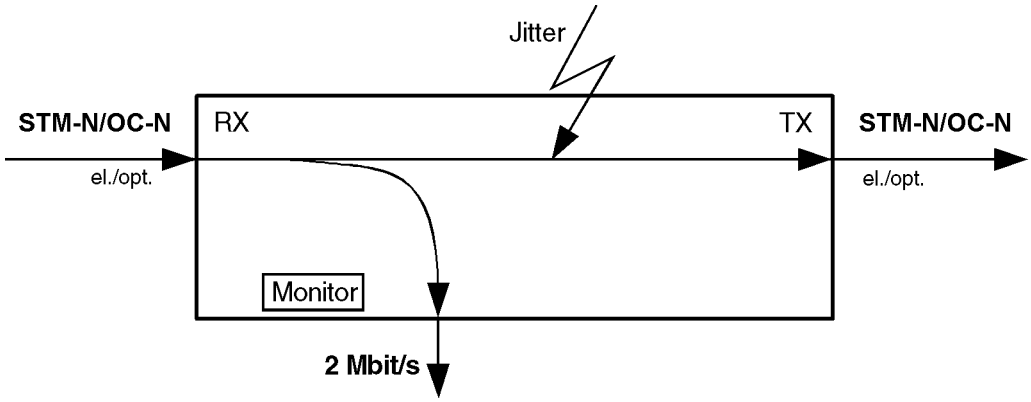


Fig. S-4 Through Mode: Adding jitter to the looped-through signal

In Through Mode, anomalies can be inserted in the SOH/TOH or the SOH/TOH bytes can be manipulated.

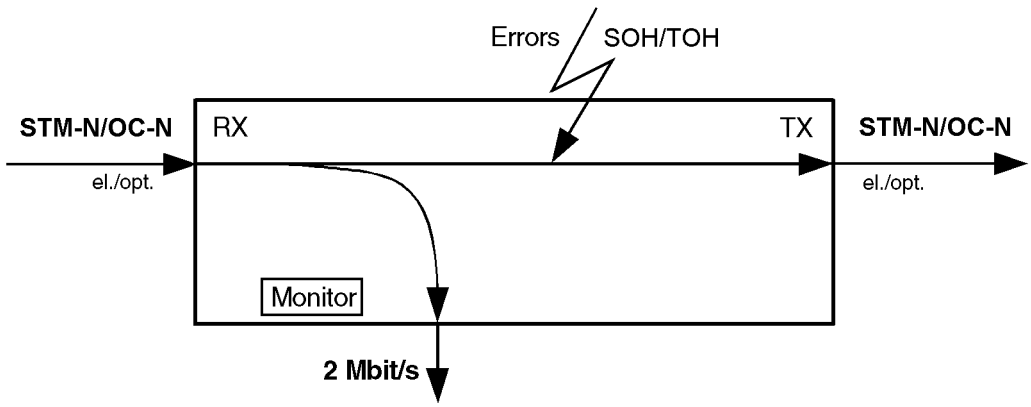


Fig. S-5 Through Mode: Inserting errors in the SOH/TOH

4.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock.
No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

4.1.2 Overhead generator

Drop&Insert

As specified in Sec. 1.3.4, Page S-26.

Through Mode

The “From Rx” function can be set in addition to the functions described in Sec. 1.3.4, Page S-26 for all bytes except bytes B1, B2 and M1.

4.1.3 Anomaly insertion

Drop&Insert

As specified in Sec. 1.3.5, Page S-28.

Through Mode

Anomaly insertion in bytes B1, B2 and MS-REI/REI-L.
Insertion limits are specified in Sec. 1.3.5, Page S-28.

4.1.4 Defect generation

Drop&Insert

As specified in Sec. 1.3.6, Page S-28.

Through Mode

No direct defect generation is possible.

Tip: Alarms (defects) in the SOH can be generated by manipulating the SOH bytes.

4.1.5 Measurements

There are no restrictions on measurements (see Sec. 2.3, Page S-33).

4.2 Signal outputs

4.2.1 Signal output [15], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-6 Specifications of the signal output [15], electrical

4.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used both as “LINE” and as “AUXILIARY” output.

4.3 Signal inputs

4.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

4.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-9 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used both as “LINE” and as “AUXILIARY” input.

5 Additions for SOH

These additions affect the following options:

- BN 3035/91.53
- BN 3035/91.54
- BN 3035/91.59

5.1 Generator section

5.1.1 Overhead generator

5.1.1.1 Section overhead (SOH), Transport overhead (TOH)

Section Overhead STM-16, OC-48

See Tab. S-11, Page S-44.

Settings can be made in the entire SOH, TOH excluding the B1 and B2 bytes and the complete pointer line (H1, H2, H3).

XX:	Inserted by parity formation (B1, B2)
Line 4a:	SDH pointers (AU-4)
Line 4b:	SDH pointers (AU-3)
Line 4c:	SONET pointers (STS-1 SPE)
Line 4d:	SONET pointers (STS-3c)
Line 4e:	SDH pointers (AU-4, VC-4-4c)
Line 4f:	SONET pointers (STS-12c SPE)
Line 4g:	SDH pointers (AU-4, VC-4-16c)
Line 4h:	SONET pointers (STS-48c SPE)
Line 9:	Z1 and Z2 are used for SONET only

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

Overhead byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11: E1, F1, E2
D1 to D3, D4 to D12 (byte group)
- Dynamic via DCC/ECC interface socket [21] (V.11): E1, F1, E2 (single byte)
- Dynamic via DCC/ECC interface socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

5.1.2 Error insertion (anomalies)

The following anomalies can be inserted in addition to those in the mainframe instrument:

Anomaly	Single	Rate	Burst m, n (frames)
B1 (STM-16, OC-48)	yes	1E-10 to 2E-5	m = 1 to 196000
B2 (STM-16, OC-48)	yes	1E-10 to 2E-3	m = 1 to 196000
MS-REI (STM-16) REI-L (OC-48)	yes	1E-10 to 2E-3	m = 1 to 196000

Table S-10 Available anomalies in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

SOH, TOH	SOH	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	...	#1	...	#16
	1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6
	2	B1 XX	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	3	D1 00	-- 00	-- 00	-- 00	D2 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	4a	H1 68	H1 68	H1 68	H1 68	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00
	4b	H1 68	H1 68	H1 68	H1 68	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00
	4c	H1 60	H1 60	H1 60	H1 60	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00
	4d	H1 60	H1 60	H1 60	H1 60	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00
	4e	H1 68	Y 9B	H1 68	Y 9B	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	H2 00	-- FF	-- FF	-- FF	H3 00	H3 00	H3 00	H3 00
	4f	H1 60	Y 93	H1 60	Y 93	H2 00	-- FF	-- FF	-- FF	H2 00	-- FF	-- FF	-- FF	H2 00	-- FF	-- FF	-- FF	H3 00	H3 00	H3 00	H3 00
	4g	H1 68	Y 9B	H1 68	Y 9B	H2 00	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	H3 00	H3 00	H3 00	H3 00
	4h	H1 60	Y 93	H1 60	Y 93	H2 00	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	-- FF	H3 00	H3 00	H3 00	H3 00
	5	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	6	D4 00	-- 00	-- 00	-- 00	D5 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	7	D7 00	-- 00	-- 00	-- 00	D8 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	8	D10 00	-- 00	-- 00	-- 00	D11 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00
	9	S1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00

Table S-11 SOH, TOH contents; STM-16, OC-48

5.2 Receiver section

5.2.1 Section overhead (SOH), Transport overhead (TOH) evaluation

Display

- SOH, TOH: hexadecimal
- Trace Identifier J0 (STM-16, OC-48): ASCII, plain text

Evaluation

Bit error measurement

- with PRBS11 pseudo-random sequence: E1, F1, E2
  D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output

- in bytes via DCC/ECC interface, socket [21] (V.11): E1, F1, E2 (single byte)
- in byte groups via DCC/ECC interface, socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

Notes:

Specifications STM-64/OC-192

The STM-64/OC-192 optical interface contains the following options:

- OC-12c/STM-4c Bit Error Testing BN 3035/90.90
- OC-48c/STM-16c Bit Error Testing BN 3035/90.93

The numbers in square brackets […] correspond to the numbers printed on the instrument.

Calibrated specifications are indicated by ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [103], optical

Connector . . . . . 2.5 mm (PC)

"Fiber-to-fiber" adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Output level *** . . . . . 0 dBm ±1 dBm

Wavelength (switchable, depending on option) . . . . . 1550 nm (1520 to 1580 nm)

Laser class to EN 60825-1:1994,
Normal operation 1
Fault condition 3A

LASER ON status display

LED is on when the laser source is active.

1.2 Clock generator and bit rates

1.2.1 Internal clock generation

See “Specifications” for the mainframe instrument.

Permissible clock offset . . . . . ±50 ppm

1.2.2 External clock generation [101]

For feeding in a jitter-modulated clock signal that must be derived from the base module clock.

Clock frequency . . . . . 9953.28 Mbit/s

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Clock input impedance . . . . . 50 Ω

Input voltage range . . . . . 100 mVpp to 600 mVpp

1.2.3 Bit rate

STM-64/OC-192 . . . . . 9953.28 Mbit/s

1.2.4 Clock output [102]

For the Generator clock

Frequency . . . . . 9953.28 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 50 mVpp

1.2.5 Frame trigger output [100]

No-load output voltage . . . . . CMOS levels

Socket . . . . . BNC

Output impedance . . . . . approx. 50 Ω

1.3 SDH and SONET TX signals

- Generates a STM-64 signal conforming to ITU-T recommendation G.707.
- Generates an OC-192 signal conforming to the Bellcore-GR-1377 standards.

1.3.1 STM-64 TX signal

STM-64 signal formation:

- one AUG1 signal (STM-1 level), generated internally x 64 (64 x AU-4 or 192 x AU-3)
- one AUG4 signal (STM-4c level)[1], generated internally x 16 (16 x AU-4-4c)
- one AUG16 signal (STM-16c level)[1], generated internally x 4 (4 x AU-4-16c)
- one AUG1 signal (STM-1 level), generated internally (AU-4 or AU-3), the other 63 AUG1 signals loaded with HP-UNEQ
- one AUG4 signal (STM-4c level)[1], generated internally, the other 60 AUG1 signals loaded with HP-UNEQ
- one AUG16 signal (STM-16c level)[1], generated internally, the other 48 AUG1 signals loaded with HP-UNEQ

1 Also see “Concatenated Mappings OC-12c/STM-4c OC-48c/STM-16c” operating manual

1.3.2 OC-192 TX signal

OC-192 signal formation:

- one STS-1 signal, generated internally x 192
- one STS-3c signal, generated internally x 64
- one STS-12c signal[1], generated internally x 16
- one STS-48c signal[1], generated internally x 4
- one STS-1 signal, generated internally, the other 191 STS-1 signals loaded with UNEQ
- one STS-3c signal, generated internally, the other 189 STS-1 signals loaded with UNEQ
- one STS-12c signal[1], generated internally, the other 180 STS-1 signals loaded with UNEQ
- one STS-48c signal[1], generated internally, the other 144 STS-1 signals loaded with UNEQ

1 See also Operating Manual “Concatenated Mappings OC-12c/STM-4c OC-48c/STM-16c”

1.3.3 Scrambling

Scrambling is as per ITU-T recommendation G.707, ANSI Standard T1.105 and Bellcore GR-253.
The scrambler cannot be switched off.

1.3.4 Overhead generator

STM-64/OC-192 overhead

See Tab. S-1, Page S-51.

Exceptions:
- The pointer row of the SOH (#1 through #64) or the TOH (#1 through #192) cannot be user defined.
- Settings are only possible in the ranges #1 through #16 (SOH) or #1 through #48 (TOH) for the “SQ” byte sequence.

Overhead byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11 (only possible if channel #1of the STM-N-/OC signal is selected): D1 to D3, D4 to D12 (byte group)
- Dynamic via DCC/ECC interface socket [21] (V.11): E1, F1, E2 (single byte)
- Dynamic via DCC/ECC interface socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

STM-1, OC-3, OC-1 standard overhead

See “STM-1 mappings / STS-1 mappings” operating manual.

Row 4 of the SOH / POH

Row 4 depends on the mapping set.
Corresponding information is found in Sec. 1.3.4.1, Page S-52 and Sec. 1.3.4.2, Page S-55.

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

SOH, TOH	SOH	#1	#2	#3	...	#64	#1	...	#64	#1	#2	#3	#4	...	#64	#1	#65	...	#128	#64	#1	...	#192	#64
	TOH	#1	#2	#3	...	#64	#1	...	#128	#64	#1	...	#192	#64	#1	#129	#1	...	#64	#1	#2	#3	#4	...
	1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A2 28	...	A2 28	A2 28	A2 28	A2 28	A2 28	...	A2 28	A2 28	A2 28	...	A2 28	A2 28	J0 C1 01	Z0 C1 02	Z0 C1 03	Z0 C1 04	Z0 C1 05	...
	2	B1 XX	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	E1 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	F1 00	-- 00	-- 00	-- 00	-- 00	-- 00
	3	D1 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D2 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D3 00	-- 00	-- 00	-- 00	-- 00	-- 00
	4	see Sec. 1.3.4.1, Page S-52 to Sec. 1.3.4.2, Page S-55																			H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	K2 00	-- 00	-- 00	-- 00	-- 00	-- 00
	6	D4 00	-- 00	-- 00	-- 00	-- 00	D5 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D6 00	-- 00	-- 00	-- 00	-- 00	-- 00
	7	D7 00	-- 00	-- 00	-- 00	-- 00	D8 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D9 00	-- 00	-- 00	-- 00	-- 00	-- 00
	8	D10 00	-- 00	-- 00	-- 00	-- 00	D11 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D12 00	-- 00	-- 00	-- 00	-- 00	-- 00
	9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	M1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	E2 00	-- 00	-- 00	-- 00	-- 00	-- 00

SOH, TOH	SOH	...	#64	#1	#2	#3	...	#64	#1	...	#64	#1	#2	#3	#4	...	#64	#1	#65	...	#128	#64	#1	...	#192
	TOH	...	#128	#64	#1	...	#192	#64	#1	#129	#1	...	#64	#1	#2	#3	#4	...	#64	#1	#65	...	#128	#64	#1	...	#192
	1	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	...	A2 28	A2 28	A2 28	A2 28	A2 28	...	A2 28	A2 28	A2 28	...	A2 28	A2 28	J0 C1 01	Z0 C1 02	Z0 C1 03	Z0 C1 04	Z0 C1 05	...
	2	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	F1 00	-- 00	-- 00	-- 00	-- 00	-- 00
	3	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D3 00	-- 00	-- 00	-- 00	-- 00	-- 00
	4	see Sec. 1.3.4.1, Page S-52 to Sec. 1.3.4.2, Page S-55																			H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	K2 00	-- 00	-- 00	-- 00	-- 00	-- 00
	6	D4 00	-- 00	-- 00	-- 00	-- 00	D5 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D6 00	-- 00	-- 00	-- 00	-- 00	-- 00
	7	D7 00	-- 00	-- 00	-- 00	-- 00	D8 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D9 00	-- 00	-- 00	-- 00	-- 00	-- 00
	8	D10 00	-- 00	-- 00	-- 00	-- 00	D11 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	-- 00	D12 00	-- 00	-- 00	-- 00	-- 00	-- 00
	9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	M1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	E2 00	-- 00	-- 00	-- 00	-- 00	-- 00

Table S-1 SOH, TOH contents; STM-64/OC-192

1.3.4.1 ITU-T Standard

STM-0 level

Containers = VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

STM-1 level

AU-3, containers = VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, containers = VC4, VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STM-4 level

AU-3, containers = VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1, #2, #3, #4								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, containers = VC4, VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1, #2, #3, #4								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC4c

Overhead #1								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

Overhead #2, #3, #4								
Y	Y	Y	-	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC4v

Overhead #1,#2 #3, #4								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STM-16 level

AU-3, containers = VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1 through #16								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, containers = VC4, VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1 through #16								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC4c

Overhead #1, #5, #9, #13								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

Overhead #2, #3, #4, #6, #7, #8, #10, #11, #12, #14, #15, #16								
Y	Y	Y	-	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC16c

Overhead #1								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

Overhead #2 through #16								
Y	Y	Y	-	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STM-64 level

AU-3, containers = VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1 through #64								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, containers = VC4, VC3, VC2, VC12, VC11/TU12, VC11/TU11

Overhead #1 through #64								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC4c

Overhead #1, #5, #9, #13, #17, #21, #25, #29, #33, #37, #41, #45, #49, #53, #57, #61								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

Overhead #2, #3, #4, #6, #7, #8, #10, #11, #12, #14, #15, #16, #18, #19, #20, #22, #23, #24, #26, #27, #28, #30, #31, #32, #34, #35, #36, #38, #39, #40, #42, #43, #44, #46, #47, #48, #50, #51, #52, #54, #55, #56, #58, #59, #60, #62, #63, #64								
Y	Y	Y	-	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

AU-4, container = VC16c

Overhead #1, #17, #33, #49								
H1	Y	Y	H2	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

Overhead #2 through #16, #18 through #32, #34 through #48, #50 through #64								
Y	Y	Y	-	-	-	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

1.3.4.2 ANSI Standard

STS-1 (OC-1)

Containers = STS1SPE, VT6SPE, VT2SPE, VT1.5SPE

Overhead #1								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

STS-3 (OC-3)

Containers = STS1SPE, VT6SPE, VT2SPE, VT1.5SPE

Overhead #1, #2, #3								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

Container = STS3cSPE

Overhead #1								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STS-12 (OC-12)

Containers = STS1SPE, VT6SPE, VT2SPE, VT1.5SPE

Overhead #1 through #12								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

Containers = STS3cSPE, STS12cSPE, STS12vSPE

Overhead #1 through #4								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STS-48 (OC-48)

Containers = STS1SPE, VT6SPE, VT2SPE, VT1.5SPE

Overhead #1 through #48								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

Containers = STS3cSPE, STS12cSPE, STS48cSPE

Overhead #1 through #16								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

STS-192 (OC-192)

Containers = STS1SPE, VT6SPE, VT2SPE, VT1.5SPE

Overhead #1 through #192								
H1	-	-	H2	-	-	H3	-	-
XX	-	-	XX	-	-	XX	-	-

Containers = STS3cSPE, STS12cSPE, STS48cSPE

Overhead #1 through #64								
H1	H1	H1	H2	H2	H2	H3	H3	H3
XX	XX	XX	XX	XX	XX	XX	XX	XX

1.3.5 Error insertion (anomalies)

The following anomalies can be inserted in addition to those in the mainframe instrument:

Anomaly	Single	Rate	Burst m, n (frames)
B1 (STM-64/OC-192)	yes	1E-10 to 2E-5	m = 1 to 196000
B2 (STM-64/OC-192)	yes	1E-10 to 1E-3	m = 1 to 196000
MS-REI (STM-64) REI-L (OC-192)	yes	1E-10 to 1E-3	m = 1 to 196000

Table S-2 Anomalies available in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

1.3.6 Alarm generator (defects)

The following defects can be generated in addition to those in the mainframe instrument:

Defect	Test sensor function	Test sensor thresholds	
-	On/Off	M in N	|----t1----| |-----t2-----|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-9953	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RS-TIM (STM-64) TIM-L (OC-192)	yes	-	-
MS-AIS (STM-64) AIS-L (OC-192)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
MS-RDI (STM-64) RDI-L (OC-192)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s

Table S-3 Defects available in addition to the mainframe instrument

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

2 Receiver section

2.1 Digital signal input

2.1.1 Signal input [113], optical

Caution

Destruction of input [113]

The maximum input level of 0 dBm must not be exceeded. Otherwise, the optical input may be destroyed.

⇒ Insert an optical attenuator if a higher input level is expected.

Connector . . . . . 2.5 mm (PC)

“Fiber-to-fiber” adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Input sensitivity
STM-64 / OC-192 *** . . . . . -4 to -15 dBm

Max. permitted input level . . . . . 0 dBm

Wavelength . . . . . 1500 to 1600 nm

Optical signal level display

Resolution . . . . . 1 dBm

Accuracy . . . . . ±3 dB

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

LOS threshold . . . . . < -15 dBm

2.2 Outputs for RX clock and frame trigger

2.2.1 Clock output [112]

For the recovered receive clock

Frequency . . . . . 9958.28 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 70 mVpp

2.2.2 Frame trigger output [110]

No-load output voltage . . . . . CMOS level

Socket . . . . . BNC

Impedance . . . . . approx. 50 Ω

2.3 SDH and SONET RX signals

- Evaluation of STM-64 signal conforming to ITU-T recommendation G.707
- Evaluation of OC-192 signal conforming to Bellcore GR-1377 standards

2.3.1 STM-64 RX signal

STM-64 signal evaluation:

- Analysis of SOH and demultiplexing of one channel, further analysis in mainframe

2.3.2 OC-192 RX signal

OC-192 signal evaluation:

- Analysis of TOH and demultiplexing of one STS-1 or STS-3c channel, further analysis in mainframe

2.3.3 Descrambling

Descrambling is as per ITU-T recommendation G.707, ANSI Standard T1.105 and Bellcore GR-253.
The descrambler cannot be switched off.

2.4 Measurement modes

2.4.1 Alarm detection (defects)

The following alarms can be evaluated and displayed in addition to the alarm detection functions given in the mainframe instrument:

Defect	**LED**
LOS (optical)	LOS
LOF-9953	LOF/OOF
RS-TIM (STM-64) TIM-L (OC-192)	-
MS-AIS (STM-64) AIS-L (OC-192)	MS-AIS/AIS-L
MS-RDI (STM-64) RDI-L (OC-192)	MS-RDI/RDI-L

Table S-4 LED displays for additional defects

2.4.2 Error measurements (anomalies)

The following anomalies can be evaluated and displayed in addition to the error measurements given in the mainframe instrument:

Anomaly	**LED**
OOF-9953	LOF/OOF
B1 (STM-64/OC-192)	B1/B2
B2 (STM-64/OC-192)	B1/B2
MS-REI (STM-64) REI-L (OC-192)	-

Table S-5 LED displays for additional anomalies

Evaluation and display of B2 errors (STM-64/OC-192) refers to all test channels taken together.

2.4.3 Section overhead (SOH) #1 to #64, Transport overhead (TOH) #1 to #192 evaluation

Display

• SOH #1, TOH #1	hexadecimal Except: B1, B2, H1 to H3
• Trace Identifier J0 (STM-64/OC-192)	ASCII, plain text

Evaluation

Bit error measurement

• with PRBS11 pseudo-random sequence:	E1, F1, E2 (single byte)
	D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output

• in bytes via DCC/ECC interface, socket [21] (V.11):	E1, F1, E2 (single byte)
• in byte groups via DCC/ECC interface, socket [21] (V.11):	D1 to D3, D4 to D12, K1 to K2 (byte group)

3 Optical power splitter BN 3035/90.49

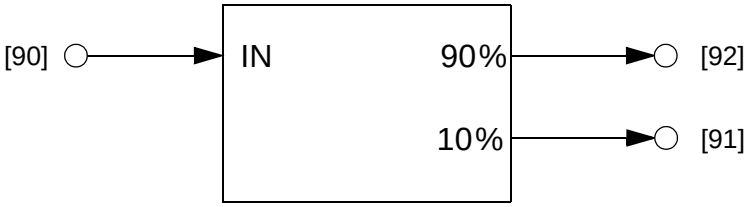


Fig. S-1 Optical power splitter

3.1 Wavelength ranges

“1310 nm” . . . . . 1260 to 1360 nm

“1550 nm” . . . . . 1500 to 1600 nm

3.2 Attenuation

Between “IN” [90] and “90%” [92] . . . . . 1.0 dB (typically), < 1.6 dB

Between “IN” [90] and “10%” [91] . . . . . 10.5 dB (typically), 8.8 to 12.0 dB

ANT-20SE
Advanced Network Tester

O.172 Jitter/Wander up to 155 Mbit/s

BN 3060/91.30

O.172 Jitter/Wander up to 622 Mbit/s

BN 3060/91.31

O.172 Jitter/Wander for 2488 Mbit/s Interfaces

BN 3060/91.32

Software Version 7.20

Specifications

5

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications O.172 Jitter / Wander up to 622 Mbit/s

Specifications O.172 Jitter / Wander (2488 Mbit/s Interface)

Notes:

Specifications O.172 Jitter / Wander up to 622 Mbit/s

These Specifications apply to the following Options:

- 3035/90.81 O.172 Jitter Generator
- 3035/90.82 O.172 Jitter Analyzer
- 3035/90.83 O.172 Jitter Generator Extension up to 622 Mbit/s
- 3035/90.84 O.172 Jitter Analyzer Extension up to 622 Mbit/s
- 3035/90.85 O.172 Wander Generator
- 3035/90.86 O.172 Wander Analyzer

Numbers enclosed in square brackets […] correspond to numbers printed on the instrument.

Calibrated specifications are indicated by ***.

Standards

Jitter and wander is generated and analyzed in accordance with the following standards:

- ITU-T G.823, G.824, G.825, O.172
- Bellcore GR-253, GR-499
- ANSI T1.101, T1.102, T1.105.03

1 Jitter Generator

Meets or exceeds the requirements of ITU-T O.172.

1.1 Bit rates

As fitted to the mainframe instrument.

Bit rates . . . . . 1544 kbit/s, 2048 kbit/s, 6312 kbit/s, 8448 kbit/s, 34368 kbit/s, 44736 kbit/s, 51840 kbit/s, 139264 kbit/s, 155520 kbit/s, 622080 kbit/s

Modulation source . . . . . internal or external

Jitter modulation signal . . . . . sine wave

1.2 Internal modulation source

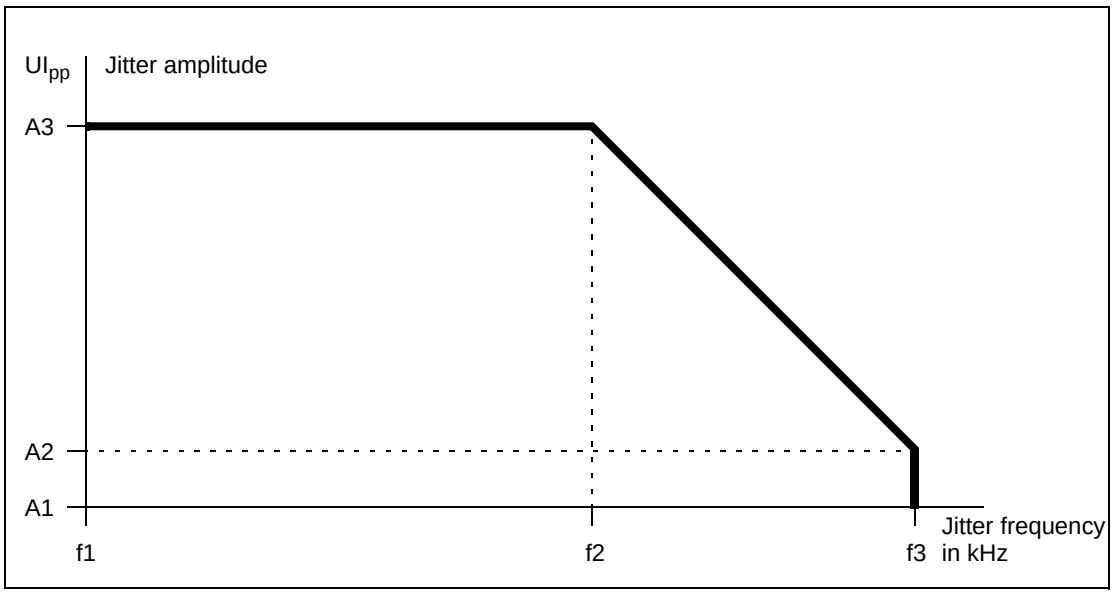


Fig. S-1 Jitter amplitude versus jitter frequency

Bit rate in kHz	A1 in UIpp	A2 in UIpp	A3 in UIpp	f1 in Hz	f2 in kHz	f3 in kHz
1544	0.002	0.5	64	0.1	0.625	80
2048	0.002	0.5	64	0.1	1.56	200
6312	0.002	0.5	64	0.1	0.94	120
8448	0.002	0.5	64	0.1	6.25	800
34368	0.002	0.5	64	0.1	27	3500
44736	0.002	0.5	64	0.1	35	4500
51840	0.002	0.5	64	0.1	27	3500
139264	0.002	0.5	64	0.1	39	5000
155520	0.002	0.5	64	0.1	39	5000
622080	0.008	1.0	256	0.1	20	5000

Table S-1 Jitter amplitude and jitter frequency at various system bit rates

Settling time for changes in amplitude . . . . . <2 seconds

Changes in modulation frequency or amplitude are without phase hits.

Jitter frequency setting step width
0.1 Hz to 1 MHz . . . . . 0.1 Hz
above 1 MHz . . . . . 1 Hz
Jitter amplitude setting step width . . . . . 0.001 UI

1.3 External modulation voltage input [30]

Socket . . . . . BNC

Input impedance . . . . . 75 Ω

Frequency range . . . . . 0 Hz to 5 MHz

Nominal input voltage range . . . . . 0 to 2.0 V_{pp} (8.2 dBm)
Corresponding jitter amplitude (at 2.0 V_{pp}) . . . . . variable

Maximum permitted input level . . . . . 4.0 V_{pp} (14.2 dBm)

If the external modulation voltage exceeds 2.0 V_{pp} this will be indicated by the message:
Warning: External [30] Modulation Exceeded!

Note: To achieve maximum accuracy, it is recommended that as high an input voltage as possible is used (maximum 2.0 V pp) and that the amplitude be set to the desired value. At very low input voltages and very large amplitude settings, accuracy will be reduced and intrinsic jitter increased.

1.4 Error limits

The error limits conform to or are better than the requirements of ITU-T O.172.

1.4.1 Amplitude error ***

Amplitude error describes the deviation from the set amplitude for sine wave modulation.

Maximum deviation . . . . . .±Q% of set value ± 0.02 UI_{pp}

Q (variable error) is taken from the following table:

Bit rate in k/bits	Q (variable error) in %	Frequency range in kHz
1544	8	0.002 to 40
2048	8	0.01 to 100
6312	8	0.002 to 60
8448	8	0.02 to 400
34368	8	0.1 to 500
	12	500 to 800
44736	8	0.002 to 400
51840	8	0.3 to 400
139264	8	0.1 to 500
	12	500 to 2000
	15	2000 to 3500
155520	8	0.5 to 500
	12	500 to 1300
622080	8	1 to 500
	12	500 to 2000
	15	2000 to 5000
Q = 12% below the stated ranges or Q = 15% above the stated ranges		

Table S-2 Q for various bit rates and modulation frequencies

1.4.2 Intrinsic jitter

The intrinsic jitter indicates the maximum output jitter of the ANT-20SE for a jitter amplitude setting of 0 UI. A bandwidth between the filters HP1 and LP (see Tab. S-7, Page S-8) is assumed.

Bit rate in kbit/s	Intrinsic jitter in UI
up to 155520	0.005
622080	0.04

Table S-3 Intrinsic jitter

1.4.3 Modulation frequency

Modulation frequency accuracy . . . . . ±0.1%

2 Jitter Analyzer

Meets or exceeds the requirements of ITU-T O.172

2.1 Bit rates

As fitted to the mainframe instrument.

Bit rates . . . . . 1544 kbit/s, 2048 kbit/s, 6312 kbit/s, 8448 kbit/s, 34368 kbit/s, 44736 kbit/s, 51840 kbit/s, 139264 kbit/s, 155520 kbit/s, 622080 kbit/s

permissible offset. . . . . ±100 ppm

Receive line codes . . . . . .as fitted to the mainframe instrument

Tip: It is recommended that cables not longer than 10 m are used for jitter and wander measurements. Longer cables can cause pattern jitter due to frequency-dependent loss characteristics, which would reduce measurement accuracy.

2.2 Jitter measurement range

Range 1
- up to 155 Mbit/s. . . . . 0 to 1.6 UI_{pp}
- at 622 Mbit/s . . . . . 0 to 6.4 UI_{pp}

Range 2
- up to 155 Mbit/s. . . . . .0 to 20 UI_{pp}
- at 622 Mbit/s . . . . . .0 to 80 UI_{pp}

Range 3
- up to 155 Mbit/s. . . . . .0 to 200 UI_{pp}
- at 622 Mbit/s . . . . . .0 to 800 UI_{pp}

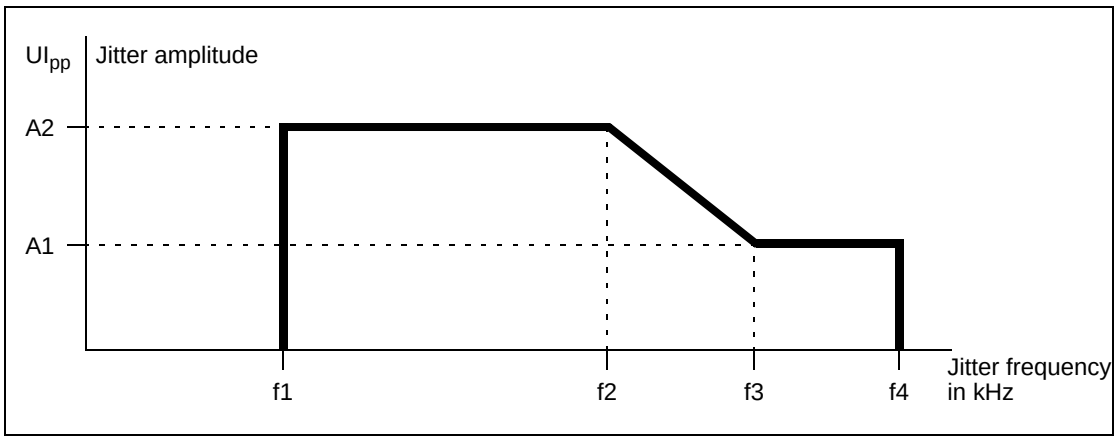


Fig. S-2 Jitter measurement range

Jitter measurement range 1.6 UI or 6.4 UI

Bit rate in kbit/s	A2 (UI)	A1 (UI)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)
1544	1.6	0.5	0.1	12.5 k	40 k	-
2048	1.6	0.5	0.1	31.25 k	100 k	-
6312	1.6	1	0.1	37.5 k	60 k	-
8448	1.6	0.5	0.1	62.5 k	200 k	400 k
34368	1.6	0.5	0.1	62.5 k	200 k	800 k
44736	1.6	0.5	0.1	62.5 k	200 k	400 k
51840	1.6	0.25	0.1	62.5 k	400 k	-
139264	1.6	0.5	0.1	62.5 k	200 k	3500 k
155520	1.6	0.2	0.1	62.5 k	500 k	1300 k
622080	6.4	0.2	0.1	62.5 k	2000 k	5000 k

Table S-4 Jitter measurement range 1.6 UI or 6.4 UI versus bit rate

Jitter measurement range 20 UI or 80 UI

Bit rate in kbit/s	A2 (UI)	A1 (UI)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)
1544	20	0.5	0.1	1 k	40 k	-
2048	20	0.5	0.1	2.5 k	100 k	-
6312	20	1	0.1	3 k	60 k	-
8448	20	0.5	0.1	5 k	200 k	400 k
34368	20	0.5	0.1	5 k	200 k	800 k
44736	20	0.5	0.1	5 k	200 k	400 k
51840	20	0.25	0.1	5 k	400 k	-
139264	20	0.5	0.1	5 k	200 k	3500 k
155520	20	0.2	0.1	5 k	500 k	1300 k
622080	80	0.2	0.1	5 k	2000 k	5000 k

Table S-5 Jitter measurement range 20 UI or 80 UI versus bit rate

Jitter measurement range 200 UI or 800 UI

Bit rate in kbit/s	A2 (UI)	A1 (UI)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)
up to 155520	200	20	0.1	100	1 k	-
622080	800	80	0.1	100	1 k	-

Table S-6 Jitter measurement range 200 UI or 800 UI versus bit rate

Note: The stated measurement ranges apply for electrical signals with nominal line code (CMI, HDB-3, B3ZS, B8ZS) or clock.

2.3 Weighting filters to ITU-T O.172

The following filter settings are possible, depending on the bit rate setting:

High-pass filter (in Hz)[1] 0.1; 2; 4; 10; 20; 40; 100; 200; 400; 500; 700
1 k; 3 k; 8 k; 10 k; 12 k; 18 k; 20 k; 30 k; 65 k; 80 k; 250 k

High-pass filter characteristic . . . . . 1st order (to ITU-T O.172)

Low-pass filter (in Hz) . . . . . .1 k[2]; 40 k; 60 k; 100 k; 400 k; 800 k; 1300 k; 3500 k; 5000 k

Low-pass filter characteristic . . . . . 3rd order Butterworth (to ITU-T O.172)

1 High pass filters between 0.1 Hz and 10 Hz only can be set for the 200 UI and 800 Ui measurement ranges.
2 The 1 kHz low-pass filter is only available for measurement ranges 200 UI and 800 UI (no other low-pass filter is available for these ranges). Filter characteristic: 4th order.

Filter properties
-3 dB cutoff frequency tolerance . . . . . .$f_C \pm 10\%$
Second high-pass filter pole . . . . . .≤0.1 Hz
Maximum attenuation . . . . . at least 60 dB

Preferred filter settings to ITU-T:

Bit rate in kbit/s	**HP1 + LP**		**HP2 + LP**	
	High-pass in kHz	**Low-pass in kHz**	**High-pass in kHz**	**Low-pass in kHz**
1544	0.01	40	8	40
2048	0.02	100	18	100
6312	0.01	60	3	60
8448	0.02	400	3	400
34368	0.1	800	10	800
44736	0.01	400	30	400
51840	0.1	400	20	400
139264	0.2	3500	10	3500
155520	0.5	1300	65	1300
622080	1	5000	250	5000

Table S-7 ITU-T filter settings

Note: If 0.1 Hz, 2 Hz or 4 Hz is set as the high-pass filter, up to three minutes may elapse after switching on the cold instrument before valid results are delivered by the jitter analyzer. This does not apply if an already warmed-up instrument is switched on again.

2.4 Demodulator output [31]

Socket . . . . . BNC

Output impedance . . . . . 75 Ω

Output voltage (terminated with 75 Ω):

Bit rate (in kbit/s)	Range		
	1.6 UI or 6.4 UI	**20 UI or 80 UI**	**200 UI or 800 UI**
up to 155520	1 V/UI	0.1 V/UI	0.01 V/UI
622080	0.25 V/UI	0.025 V/UI	0.0025 V/UI

Table S-8 Output voltages at output [31]

2.5 Result display

The positive and negative jitter amplitudes are measured.

Current Values

The current values are displayed continuously or shown as a graph.

Jitter peak-peak . . . . . peak to peak jitter value

Jitter +peak. . . . . positive peak jitter value

Jitter -peak . . . . . negative peak jitter value

Current Values display averaging (selectable). . . . . off, 1, 2, 3, 4, 5 seconds

Display resolution (current value)
in range 1 . . . . . 0.001 UI_{pp}
in range 2 . . . . . 0.01 UI_{pp}
in range 3 . . . . . 0.1 UI_{pp}

Display range 1 (graphic display)
Jitter peak-peak . . . . . 1.6 UI_{pp} or 6.4 UI_{pp} (622 Mbit/s)
Jitter +peak/-peak. . . . . ±0.8 UI_p or ±3.2 UI_p (622 Mbit/s)

Display range 2 (graphic display)
Jitter peak-peak . . . . . 20 UI_{pp} or 80 UI_{pp} (622 Mbit/s)
Jitter +peak/-peak. . . . . ±10 UI_p or ±40 UI_p (622 Mbit/s)

Display range 3 (graphic display)
Jitter peak-peak . . . . . 200 UI_{pp} or 800 UI_{pp} (622 Mbit/s)
Jitter +peak/-peak. . . . . ±100 UI_p or ±400 UI_p (622 Mbit/s)

Max. Values

The maximum value is only displayed if a measurement was started in the “Application Manager”.

Jitter peak-peak . . . . . peak to peak jitter value in measurement interval

Jitter +peak . . . . . positive peak jitter value in measurement interval

Jitter -peak . . . . . negative peak jitter value in measurement interval

Display resolution
in range 1. . . . . .0.001 UI_{pp}
in range 2. . . . . .0.01 UI_{pp}
in range 3. . . . . .0.1 UI_{pp}

2.6 Error limits for displayed jitter

The error limits for displayed jitter meet or are better than the requirements of ITU-T Recommendation O.172.

The stated error limits apply under the following conditions:

- Electrical signals: Nominal input level to ITU-T G.703 without line distortion nominal line code (CMI, HDB-3, B3ZS, B8ZS) or clock
- Optical signals: Optical level in the range -10 dBm to -12 dBm (scrambled NRZ)
- Structured signals (pseudo-random sequences or framed signals) or clock
- Sine wave modulation
- Standard filter HP1 + LP or HP2 + LP as per Sec. 2.3, Page S-8, Table S-5

The overall measurement error is made up from the following partial errors (additive):

- Measurement error at reference frequency (see Sec. 2.6.1, Page S-11)
- Frequency response error (see Sec. 2.6.2, Page S-12)
- Deviation of filter frequency response from nominal curve (see Sec. 2.3, Page S-8)

2.6.1 Measurement accuracy

The stated measurement accuracy applies under the following conditions:

- Reference frequency: 100 kHz (SDH) or 1 kHz (PDH)
- The stated measurement error applies without restriction to the smaller measurement range, for values >0.8 UI (or >3.2 UI at 622 Mbit/s) in the medium measurement range and for values >10 UI (or 40 UI at 622 Mbit/s) in the larger measurement range.

Maximum measurement error***
(excluding frequency response error). . . . . ±5% of measured value ± W

The value W (fixed error) is taken from the following tables:

Bit rate in kbit/s	**Structured signals or pseudo-random bit sequences (PRBS)**			
	Filter HP1 + LP	**Filter HP2 + LP**	**HP 2 Hz + LP**	**HP 0.1 Hz + LP**
	W in UI	**W in UI**	**W in UI**	**W in UI**
1544	0.03	0.02[1]	0.05	0.07[2]
2048	0.03	0.02[1]	0.05	0.07[2]
6312	0.03	0.02[1]	0.05	0.07[2]
8448	0.03	0.02[1]	0.05	0.07[2]
34368	0.035	0.025[1]	0.07	0.1[2]
44736	0.035	0.025[1]	0.07	0.1[2]
51840	0.035	0.025	0.07	0.1[2]
139264	0.035	0.025[1]	0.07	0.2[2]
155520	0.05	0.025[1]	0.07	0.2[2]
622080	0.07	0.05[1]	0.1	0.5[2]

1 Demonstrated without modulation
2 After warming up the instrument for ≥30 min, only demonstrated with signal sources having high clock stability

Table S-9 W (fixed error) for structured signals or pseudo-random bit sequences

Bit rate in kbit/s	**Clock signals**			
	Filter HP1 + LP	**Filter HP2 + LP**	**HP 2 Hz + LP**	**HP 0.1 Hz + LP**
	W in UI	**W in UI**	**W in UI**	**W in UI**
1544	0.015	0.01[1]	0.05	0.07[2]
2048	0.015	0.01[1]	0.05	0.07[2]
6312	0.015	0.01[1]	0.05	0.07[2]

1 Demonstrated without modulation
2 After warming up the instrument for ≥30 min, only demonstrated with signal sources having high clock stability
3 Clock signals cannot be measured at the optical interfaces

Table S-10 W (fixed error) for clock signals

Bit rate in kbit/s	Clock signals			
	Filter HP1 + LP	Filter HP2 + LP	HP 2 Hz + LP	HP 0.1 Hz + LP
	W in UI	W in UI	W in UI	W in UI
8448	0.015	0.01[1]	0.05	0.07[2]
34368	0.025	0.02[1]	0.07	0.1[2]
44736	0.025	0.02[1]	0.07	0.1[2]
51840[3]	0.025	0.02	0.07	0.1[2]
139264	0.025	0.02[1]	0.07	0.2[2]
155520[3]	0.025	0.02[1]	0.07	0.2[2]

1 Demonstrated without modulation
2 After warming up the instrument for ≥30 min, only demonstrated with signal sources having high clock stability
3 Clock signals cannot be measured at the optical interfaces

Table S-10 W (fixed error) for clock signals *(continued)*

Additional error for
attenuated electrical signals . . . . . typically ≤0.03 UI
line-distorted electrical signals. . . . . typically ≤0.05 UI
optical signals with levels >-10 dBm or <-12 dBm. . . . . typically ≤0.05 UI

2.6.2 Frequency response error***

The following frequency response error can occur in addition to the measurement error at frequencies that are not equal to the reference frequency:

Frequency response error for SDH-/SONET-signals . . . . . .as per ITU-T O.172, Table 10

Reference frequency . . . . . 100 kHz

Bit rate in kbit/s	Additional error	Frequency range[1] in kHz
51840	±2%	0.1 to 400
155520	±2%	0.5 to 300
	±3%	300 to 1000
	±5%	1000 to 1300
622080	±2%	1 to 300
	±3%	300 to 1000
	±5%	1000 to 3000
	±10%	3000 to 5000

1 Below the stated frequency range, the error which applies there is continued

Table S-11 Frequency response error for SDH-/SONET-signals

Frequency response error for PDH / tributary signals . . . . . as per ITU-T O.171, Table 6

Reference frequency . . . . . 1 kHz

Bit rate in kbit/s	Additional error	Frequency range[1] in kHz
1544	±4%	0.01 to 1
	±2%	1 to 40
2048	±2%	0.02 to 100
6312	±4%	0.01 to 1
	±2%	1 to 60
8448	±2%	0.02 to 300
	±3%	300 to 400
34368	±2%	0.1 to 300
	±3%	300 to 800
44736	±4%	0.01 to 0.2
	±2%	0.2 to 300
	±3%	300 to 400
139264	±2%	0.2 to 300
	±3%	300 to 1000
	±5%	1000 to 3000
	±10%	3000 to 3500

1 Below the stated frequency range, the error which applies there is continued

Table S-12 Frequency response error for PDH / tributary signals

2.7 Input phase tolerance when measuring pointer jitter

The following table shows jitter amplitude and frequency combinations that can be measured without degradation in the 1.6 UI range using the specified high-pass filter (or above). It is assumed that the jitter is sine wave modulation conforming to ITU-T O.172, Section 9.2.4, Table 6 (representing worst-case pointer jitter).

Bit rate in kbit/s	HP filter (Hz)	Amplitude in UI	Frequency in Hz
1544	≥10	20	0.5
2048	≥20	40	0.5
6312	≥10	20	0.5
8448	≥20	40	0.5
34368	≥100	25	5
44736	≥10	20	0.5
139264	≥200	80	1.5

Table S-13 Input phase tolerance when measuring pointer jitter

2.8 RMS jitter

Range and resolution up to 155 Mbit/s

	1.6 UI range (peak - peak)	**20 UI range (peak - peak)**	**200 UI range (peak - peak)**
RMS jitter range	0 to 0.8 UI	0 to 10 UI	0 to 100 UI
Resolution	0.001 UI	0.01 UI	0.1 UI

Table S-14 Range and resolution up to 155 Mbit/s

Range and resolution at 622 Mbit/s

	6.4 UI range (peak - peak)	**80 UI range (peak - peak)**	**800 UI range (peak - peak)**
RMS jitter range	0 to 3.2 UI	0 to 40 UI	0 to 400 UI
Resolution	0.001 UI	0.01 UI	0.1 UI

Table S-15 Range and resolution at 622 Mbit/s

Measurement accuracy

Valid for all bit rates if the 12 kHz RMS filter is used with nominal signals.

1.6 UI or 6.4 UI range . . . . . ±5% of measured value ± 0.01 UI
20 UI / 200 UI or 80 UI / 800 UI range . . . . . ±5% of measured value ± 0.1 UI

Integration time . . . . . 1, 2, 5, 10, 20, 40, 80 seconds (selectable)

Default setting . . . . . 1 second

3 Tolerance to jitter measurement

3.1 Fast Maximum Tolerable Jitter (F-MTJ)

Only possible if option BN 3035/90.81 is fitted.

Once the measurement is started, selectable jitter amplitude and jitter frequency combinations are set. The result for each combination (test point) is then indicated either as “OK” (no alarms or bit errors) or “Failed” (alarms or bit errors).

Error source selectable from:
SDH . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI

SONET . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Delay (recovery time) . . . . . .0.1 to 999 s

Selectable jitter frequencies (scan frequencies) and jitter amplitudes . . . . . see Tab. S-1, Page S-3

Display . . . . . table of values

Default settings

Bit rate in kbit/s	f1 / A1 in kHz/UI	f2 / A2 in kHz/UI	f3 / A3 in kHz/UI	f4 / A4 in kHz/UI	f5 / A5 in kHz/UI	f6 / A6 in kHz/UI
1544	0.01/5	0.1/5	0.5/5	2/0.7	8/0.1	40/0.1
2048	-	0.002/15	0.02/1.5	2.4/1.5	18/0.2	100/0.2
6312	0.01/5	0.1/5	0.9/5	2/0.61	4/0.1	20/0.1
8448	-	0.002/15	0.02/1.5	0.4/1.5	3/0.2	400/0.2
34368	-	0.01/15	0.1/1.5	1/1.5	10/0.15	800/0.15
44736	0.01/5	0.1/5	2.3/5	15/0.52	60/0.1	300/0.1
51840	0.01/15	0.03/15	0.3/1.5	2/1.5	20/0.15	400/0.15
139264	-	0.02/15	0.2/1.5	0.5/1.5	10/0.075	3500/0.075
155520	-	0.05/15	0.5/1.5	6.5/1.5	65/0.15	1300/0.15
622080	-	0.1/15	1/1.5	25/1.5	250/0.15	5000/0.15

Table S-16 Jitter frequency and jitter amplitude settings for Fast-MTJ measurement

The default values in the table represent the corner values for the limit curves specified in ITU-T Recommendations G.823 and G.825 or Bellcore GR-499.

3.2 Maximum Tolerable Jitter (MTJ)

Only possible if option BN 3035/90.81 is fitted.

Once the measurement is started, the jitter amplitude of the digital signal is altered until the bit error meter detects that a pre-set threshold has been exceeded. The maximum tolerable jitter value that will be shown is one search step less than the value causing the threshold violation.

Error source, selectable from:
SDH . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI

SONET . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Delay (recovery time) . . . . . 0.1 to 999 s

Gate time . . . . . .1 to 60 s

The jitter frequencies (scan frequencies) can be user defined as a group of up to 20 freely programmable frequencies in the range from 0.1 Hz to 5 MHz (depending on bit rate).

Display . . . . . table of values or log vs. log graph

Tolerance masks can also be displayed.

Default scan frequencies

Bit rate in kbit/s	f1 in kHz	f2 in kHz	f3 in kHz	f4 in kHz	f5 in kHz	f6 in kHz	f7 in kHz	f8 in kHz	f9 in kHz
1544	0.002	0.01	0.04	0.1	0.4	1	4	10	40
2048	0.002	0.02	0.2	0.8	2.4	8	18	50	100
6312	0.002	0.01	0.04	0.1	0.4	1	4	20	60
8448	0.002	0.02	0.4	1	3	10	40	100	400
34368	0.002	0.1	1	4	10	40	100	300	800
44736	0.002	0.01	0.1	0.6	3	10	30	100	400
51840	0.002	0.01	0.03	0.3	2	8	20	100	400
139264	0.002	0.1	1	10	40	100	400	1000	3500
155520	0.002	0.1	1	6.5	20	65	200	600	1300
622080	0.002	0.1	1	10	100	400	1000	2000	5000

Table S-17 Default scan frequencies

Default tolerance masks

Bit rate in kbit/s	f1 / A1 in kHz/UI	f2/A2 in kHz/UI	f3 / A3 in kHz/UI	f4 / A4 in kHz/UI	f5 / A5 in kHz/UI	f6 / A6 in kHz/UI
1544	-	-	0.01/5	0.5/5	8/0.1	40/0.1
2048	-	0.002/15	0.02/1.5	2.4 /1.5	18/0.2	100/0.2
6312	-	-	0.01/5	0.9/5	4/0.1	20/0.1
8448	-	0.002/15	0.02/1.5	0.4/1.5	3/0.2	400/0.2
34368	-	0.003/50	0.1/1.5	1/1.5	10/0.15	800/0.15
44736	-	-	0.01/5	2.3/5	60/0.1	300/0.1
51840	0.01/15	0.03/15	0.3/1.5	2/1.5	20/0.15	400/0.15
139264	-	0.005/60	0.2/1.5	0.5/1.5	10/0.075	3500/0.075
155520	-	0.0193/39	0.5/1.5	6.5/1.5	65/0.15	1300/0.15
622080	-	0.0096/156	1/1.5	25/1.5	250/0.15	5000/0.15

Table S-18 Default tolerance masks

4 Jitter Transfer Function

4.1 Jitter Transfer Function measurement

Only possible if options BN 3035/90.81 **and** BN 3035/90.82 are fitted.

Once the measurement is started, a user-defined amplitude is set at each of the pre-selected jitter frequencies in turn. The Jitter Analyzer determines the jitter transferred by the device under test. The jitter is measured selectively, i.e. using a band-pass filter that is tuned to the modulation frequency. This ensures that interference frequencies outside the pass band of the filter do not affect the result.

The jitter transfer function is calculated from the logarithmic ratio of output jitter to input jitter on a point by point basis:

Jitter transfer function: $H(f_j) = 20 \log \frac{\text{output jitter}}{\text{input jitter}}$

Maximum measurement accuracy is achieved by means of a calibration measurement which can either be performed before every measurement (recommended) or stored for future use. The intrinsic error of the analyzer is determined at every selected scan frequency during a loop measurement (TX linked to RX). This intrinsic error correction is then applied to the results for the device under test as they are measured.

TX jitter settings . . . . . see Sec. 1, Page S-2

Measurement range . . . . . 1.6 UI_{pp} or 20 UI_{pp} (switchable)
or 6.4 UI_{pp} or 80 UI_{pp} at 622 Mbit/s

Delay (recovery time) . . . . . 0.1 to 999 s

Filter bandwidth (-3 dB) . . . . . 10 Hz

The jitter frequencies (scan frequencies) can be user defined as a group of up to 20 freely programmable frequencies in the range from 10 Hz to 5 MHz (depending on bit rate).

Display . . . . . table of values or graph with logarithmic frequency axis

Tolerance masks can also be displayed.

Default scan frequencies and amplitudes

Bit rate in kbit/s	f1/Ampl. (kHz/UI)	f2/Ampl. (kHz/UI)	f3/Ampl. (kHz/UI)	f4/Ampl. (kHz/UI)	f5/Ampl. (kHz/UI)	f6/Ampl. (kHz/UI)	f7/Ampl. (kHz/UI)	f8/Ampl. (kHz/UI)	relevante Normen
1544	0.01/1	0.035/1	0.1/1	0.35/1	1/1	2.5/0.51	15/0.1	-	Bellcore GR-499
2048	0.01/1	0.1/1	1/1	10/0.36	36/0.2	100/0.2	-	-	ITU-T G.823
6312	0.01/1	0.035/1	0.1/1	0.5/1	1/1	2.5/0.34	15/0.1	-	Bellcore GR-499
8448	0.01/1	0.1/1	0.4/1	1/0.6	10/0.2	100/0.2	400/0.2	-	ITU-T G.823
34368	0.01/1	0.1/1	0.3/1	1/1	3/0.5	10/0.15	100/0.15	800/0.15	ITU-T G.823
44736	0.01/1	0.1/1	1/1	4/1	15/0.52	-	-	-	Bellcore GR-499
51840	0.01/1	0.1/1	1/1	10/0.3	40/0.15	100/0.15	400/0.15	-	Bellcore GR-253
139264	0.01/1	0.1/1	0.5/1	1/0.75	5/0.15	-	-	-	ITU-T G.823
155520	0.1/1	1/1	10/0.975	130/0.15	500/0.15	1300/0.15	-	-	ITU-T G.825, Bellcore GR-253
622080	0.1/1	1/1	10/1	100/0.375	500/0.15	1000/0.15	5000/0.15	-	ITU-T G.825, Bellcore GR-253

Table S-19 Default scan frequencies and amplitudes

The default scan frequencies and amplitudes correspond to or are below the maximum tolerable jitter limit curves specified in the relevant standards. This ensures that the JTF measurement is not performed using unacceptably high levels of jitter.

Default tolerance masks

Bit rate in kbit/s	f1/max. dB in kHz/in dB	f2/max. dB in kHz/in dB	f3/max. dB in kHz/in dB	f4/max. dB in kHz/in dB	Applicable standards
1544	0.01/0.1	0.35/0.1	2.5/-34	15/-49.5	Bellcore GR-499
2048	0.01/0.5	36/0.5	100/-8.4	-	ITU-T G.735, G.736, G.737, G.738, G.739
6312	0.01/0.1	0.5/0.1	2.5/-28	15/-43.5	Bellcore GR-499
8448	0.01/0.5	0.1/0.5	1/-19.5	400/-19.5	ITU-T G.751
34368	0.01/0.5	0.3/0.5	3/-19.5	800/-19.5	ITU-T G.751
44736	0.01/0.1	1/0.1	15/-23.4	-	Bellcore GR-499
51840	0.01/0.1	40/0.1	400/-19.9	-	ANSI T1.105.03, Bellcore GR-253
139264	0.01/0.5	0.5/0.5	5/-19.5	-	-
155520	0.01/0.1	130/0.1	1300/-19.9	-	ITU-T G.958, ANSI T1.105.03, Bellcore GR-253
622080	0.01/0.1	500/0.1	5000/-19.9	-	ITU-T G.958, ANSI T1.105.03, Bellcore GR-253

Table S-20 Default tolerance masks

The default lower tolerance mask limit (min. dB) is always -99.9 dB and is not visible in the graph display.

4.2 Measurement error (typical)

The total error F_{total} is made up from the partial errors F1 + F2 + F3.

F1 and F2 depend on the transmitted jitter amplitude (F1) and on the measured jitter amplitude (F2). They can be read off from the diagrams below.
F3 depends on the measured jitter loss D (in dB) and on a bit rate-dependent constant k up to a maximum value,

where: **F3 = D · k**

Note: The value of F3 can never exceed $F3_{MAX}$.

Bit rate	**k**	**$F3_{MAX}$**
≤ 140 Mbit/s	0.035	0.5 dB
155 Mbit/s	0.05	1 dB
622 Mbit/s	0.1	3 dB

Table S-21 Factor k and the maximum value $F3_{MAX}$ as a function of bit rate

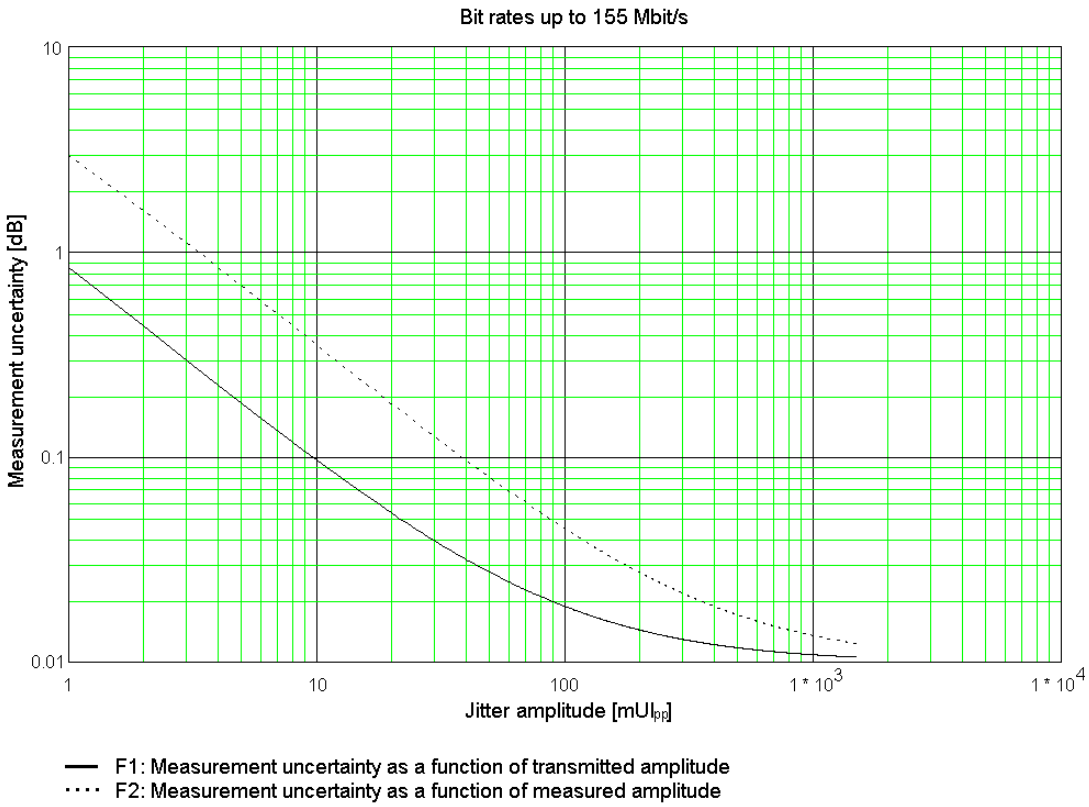


Fig. S-3 Measurement uncertainty for bit rates up to 155 Mbit/s

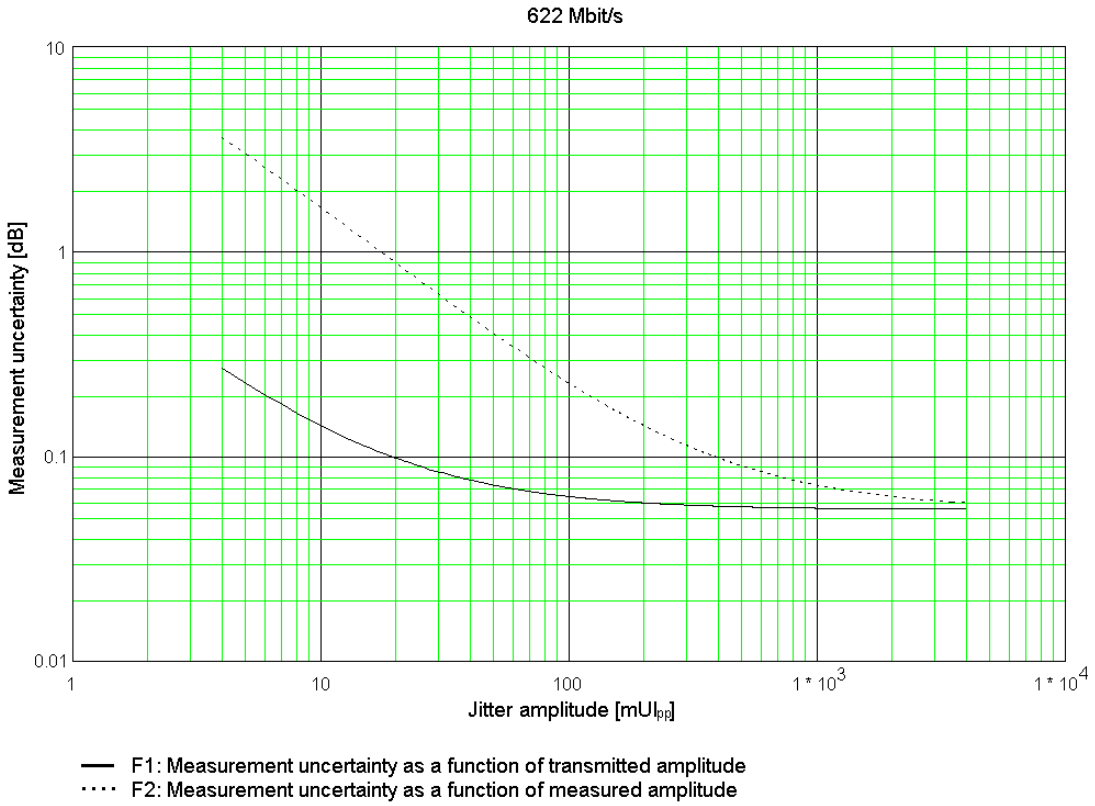


Fig. S-4 Measurement uncertainty for 622 Mbit/s

All data applies under the following conditions:

- Nominal level and standard line code
- Temperature: 20 °C to 26 °C
- Integration time: 5 s
- Settling time: 1 s
- Complete instrument warm-up time: 30 minutes
  The relevant optical bit rate (155 Mbit/s and 622 Mbit/s) must also have been activated for at least five minutes.
- Calibration immediately before the measurement
- Jitter amplitude on the jitter meter and measurement range:

up to 155 Mbit/s:	1 mUI to 1.5 UI	1.6 UI range
at 622 Mbit/s:	4 mUI to 4 UI	6.4 UI range

Example

A jitter transfer of -21 dB is measured at a bit rate of 34 Mbit/s and a transmitted amplitude of 1000 mUI_{pp}.

To calculate the total error, errors F1 and F2 are taken from Fig. S-3. Error F3 is calculated using the relationship given above (k is taken from Table S-21).

F1 = 0.011 dB (from Fig. S-3)

The jitter transfer function

$$H(f_j) = 20 \log \frac{\text{measured jitter}}{\text{transmitted jitter}} = 20 \log \frac{x}{1000\ mUI} = -21\ dB$$

gives a measured jitter of approximately 90 mUI.

This value can be used to read the value of F2 from Fig. S-3.

F2 = 0.05 dB (from Fig. S-3)

F3 = 21 dB · 0.035 = 0.735 dB

F3 is greater than $F3_{MAX}$ in Table S-21 (0.5 dB). The value $F3_{MAX}$ = 0.5 dB is therefore substituted for F3.

$$\mathbf{F_{total}} = 0.011\ dB + 0.05\ dB + 0.5\ dB \mathbf{= 0.561\ dB}$$

F1 F2 F3

5 Phase hits

An event is counted if the demodulated jitter signal violates a pre-set positive or negative threshold value. Positive and negative events are counted by separate counters. The counter value indicates the number of times the positive and negative thresholds were violated during the measurement.

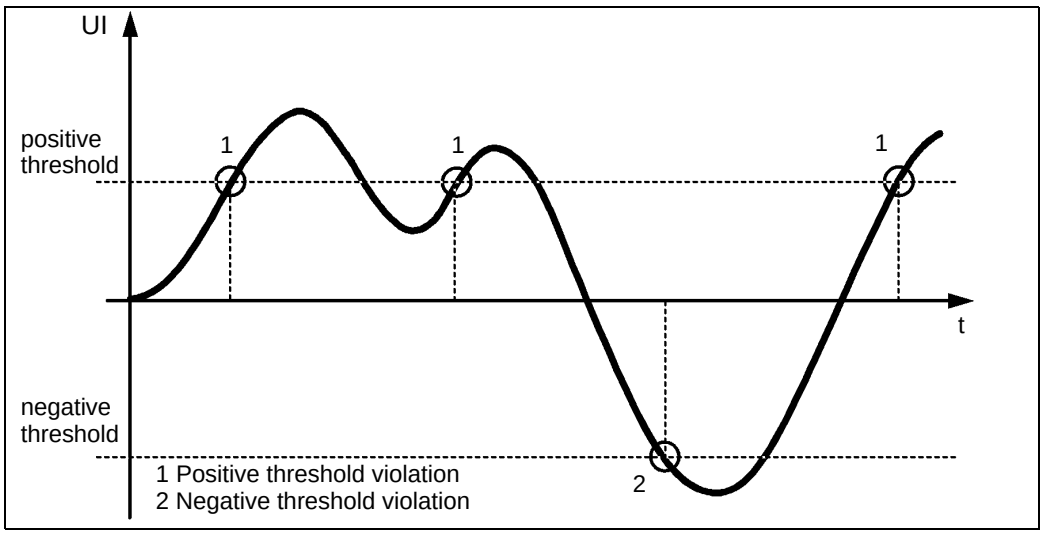


Table S-22 Example: Demodulated jitter signal (jitter vs. time function)

Display

- Number of times positive threshold was violated
- Number of times negative threshold was violated

Threshold settings (positive and negative)

Bit rates up to 155 Mbit/s	**1.6 UI range**	**20 UI range**	**200 UI range**
Range of values	0.1 UI to 0.8 UI	0.1 UI to 10 UI	1 to 100 UI
Step width	0.1 UI	0.1 UI	1 UI

Table S-23 Range of values and step width up to 155 Mbit/s

Bit rate 622 Mbit/s	**6.4 UI range**	**80 UI range**	**800 UI range**
Range of values	0.1 to 3.2 UI	0.1 to 40 UI	1 to 400 UI
Step width	0.1 UI	0.1 UI	1 UI

Table S-24 Range of values and step width for 622 Mbit/s

Alarms

Alarms . . . . . LOS (Loss of Signal), LTI (Loss of Timing Information) and AC line power failure

The counters are stopped during an alarm. The count resumes when the alarm is cleared and the gate time has not yet elapsed completely. The occurrence of an alarm is indicated by a yellow warming sign in front of the result. The warning sign is cleared when a new measurement is started.

Maximum count frequency . . . . . approx. 10 kHz (sine wave), approx. 25 kHz (square wave)

Threshold setting error limits . . . . . ±5% of threshold value, plus jitter meter error

6 Wander Generator

Only possible if options BN 3035/90.81 **and** BN 3035/90.85 are fitted.

6.1 Bit rates

As fitted to the mainframe instrument.

Bit rates . . . . . 1544 kbit/s, 2048 kbit/s, 6312 kbit/s, 8448 kbit/s, 34368 kbit/s, 44736 kbit/s, 51840 kbit/s, 139264 kbit/s, 155520 kbit/s, 622080 kbit/s

Wander modulation shape. . . . . sine wave

Frequency range . . . . . 10 µHz to 10 Hz

Wander frequency setting step width . . . . . 1 µHz

Amplitude range . . . . . 0.1 UI to 200000 UI

Wander amplitude setting step width. . . . . 0.1 UI

6.2 Wander amplitude and wander frequency

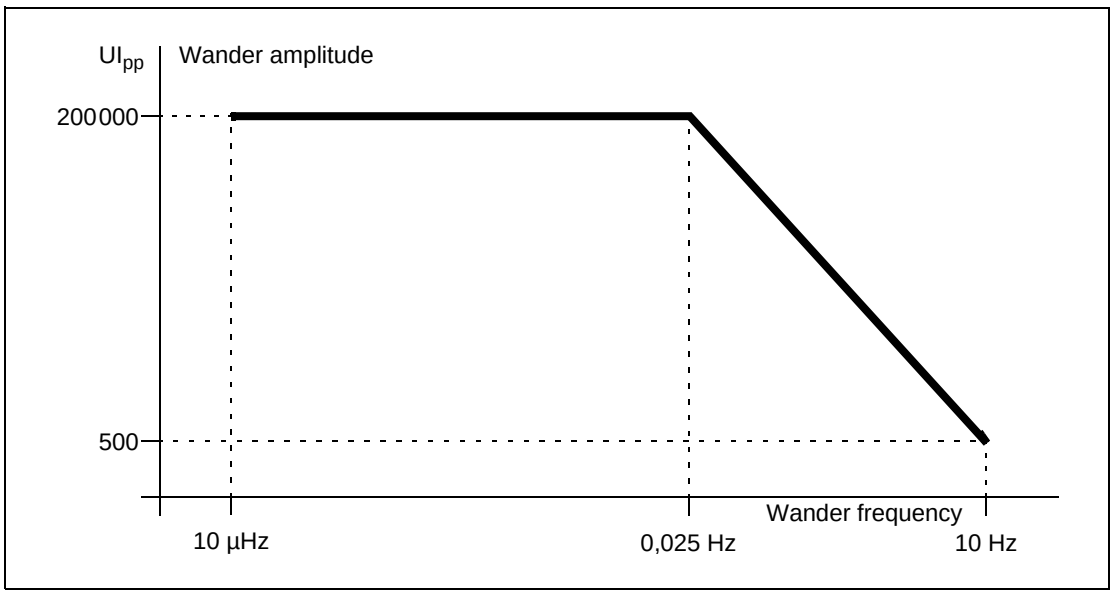


Fig. S-5 Maximum wander amplitude as a function of wander frequency

6.3 Error limits

6.3.1 Amplitude error

Amplitude error describes the deviation from the set amplitude for sine wave modulation.

Maximum deviation . . . . . ±8% of set value ± 0.02 UI_{pp}

6.3.2 Intrinsic jitter / wander

The intrinsic jitter / wander indicates the maximum output jitter / wander of the ANT-20SE for a jitter / wander amplitude setting of 0 UI. A bandwidth between the filters HP1 and LP (see Tab. S-7, Page S-8) is assumed.

Bit rate in kbit/s	**Intrinsic jitter / wander in UI**
up to 155520	0.005
622080	0.04

Table S-25 Intrinsic jitter / wander

6.3.3 Modulation frequency

Modulation frequency accuracy . . . . . ±0.1%

6.4 Synchronization

In Wander Generator mode, the generator of the ANT-20SE is normally synchronized to an external source. The appropriate reference signal should be fed into socket [25]. Refer to the “Specifications” for the mainframe instrument.

7 Wander Measurement

Only possible if options BN 3035/90.82 **and** BN 3035/90.86 are fitted.

7.1 Bit rates

As fitted to the mainframe instrument.

Bit rates . . . . . 1544 kbit/s, 2048 kbit/s, 6312 kbit/s, 8448 kbit/s, 34368 kbit/s, 44736 kbit/s, 51840 kbit/s, 139264 kbit/s, 155520 kbit/s, 622080 kbit/s

7.2 Reference input [34]/[35]

Tip: Wander measurements can only be performed using an external reference signal! This signal must conform with the clock frequencies or bit rates and input levels specified below.

Permissible offset . . . . . ±100 ppm

Wander transmission bandwidth . . . . . 0 to 100 Hz

Sockets . . . . . Bantam [34] and BNC [35]

Monitoring . . . . . LTI (Loss of Timing Information)

Socket [34]

Input impedance . . . . . 110 Ω, balanced

Permitted input level
Clock signal . . . . . 0.65 V_{pp} to 6.5 V_{pp}
Data signal (HDB-3, B8ZS) . . . . . ±3 V ± 10%

Reference frequencies
Clock signal . . . . . 1.544 MHz; 2.048 MHz
Data signal (HDB-3, B8ZS) . . . . . 1.544 Mbit/s; 2.048 Mbit/s

Socket [35]

Input impedance . . . . . 75 Ω, unbalanced

Permitted input level
Clock signal . . . . . 0.5 V_{pp} to 5 V_{pp}
Data signal (HDB-3, B8ZS) . . . . . ±2.37 V ± 10%

Reference frequencies
Clock signal . . . . . 1.544 MHz; 2.048 MHz; 5 MHz; 10 MHz
Data signal (HDB-3, B8ZS) . . . . . 1.544 Mbit/s; 2.048 Mbit/s

7.3 Measurement range

Wander amplitude range . . . . . ±1 x 10^6 s

Maximum permitted phase change rate
Sample rate 1/s . . . . . 1000 UI/s for all bitrates
Sample rate ≥ 30/s . . . . . 5000 UI/s for bitrates <45 Mbit/s
20000 UI/s for bitrates ≥45 Mbit/s

The upper limit of the wander frequency range is set by a first-order low-pass filter. The low-pass filter is selected automatically to correspond with the selected sample rate.

Sample rate	Low-pass filter/f_C
1/s	0.1 Hz
30/s	10 Hz
60/s	20 Hz
300/s	100 Hz

Table S-26 Low-pass filters for various sample rates

Low-pass filter

Filter characteristic . . . . . first order low-pass

Measurement bandwidth . . . . . 0 Hz to f_C

-3 dB cutoff frequency deviation . . . . . f_C ± 10%

Maximum attenuation . . . . . at least 30 dB

Pass-band ripple in the range 1 Hz to 10 Hz
(referred to the attenuation at 0.1 Hz) . . . . . <±0.2 dB

7.4 Result display

Result displayed in seconds
TIE (instantaneous value) . . . . . numerically and graphically
MTIE (maximum difference) . . . . . numerically

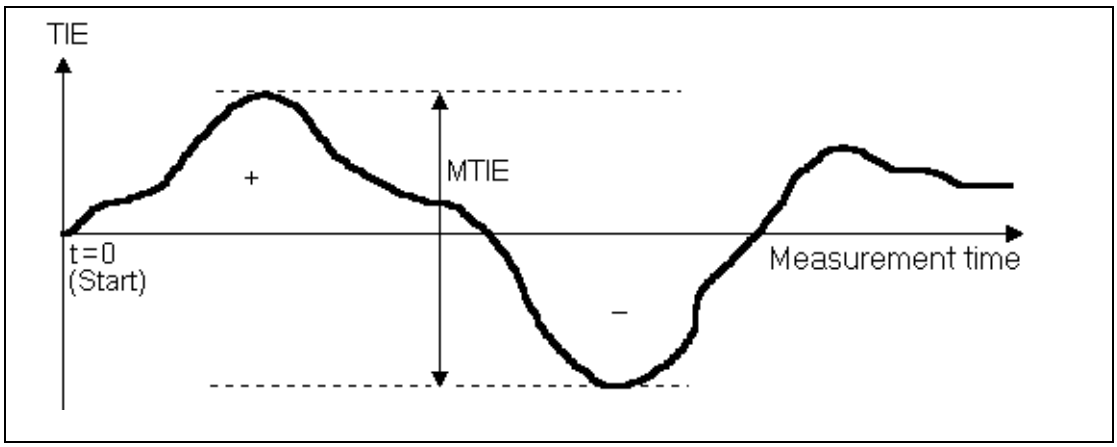


Fig. S-6 Example: Wander measurement versus measurement time

7.5 Accuracy***

The specified measurement error applies after a warm-up period of at least 30 minutes for the ANT-20SE and a maximum change in ambient temperature of 5 K.

Overall TIE error for each TIE measurement
for an observation interval τ . . . . . $<\pm 5\%$ of TIE value $\pm Z_0$

Z_0 is taken from the following table:

Z_0 (τ)/ns	**Observation interval τ/s**
$2.5 + 0.0275\ \tau$	$0.05 \leq \tau \leq 1000$
$29 + 0.001\ \tau$	$\tau > 1000$

Table S-27 Error Z_0

7.6 Memory requirements

Before starting a long-term wander measurement, check the available hard disk space. The ANT-20SE software calculates the expected hard disk space requirements from the selected gate time and sample rate. A warning message is displayed if there is insufficient space.

Sample rate	Memory requirements
1/s	approx. 58 kB/h
30/s	approx. 1.65 MB/h
60/s	approx. 3.3 MB/h
300/s	approx. 16.5 MB/h

Table S-28 Memory requirements versus sample rate

8 Measurement of Maximum Tolerable Wander

only possible with options BN 3035/90.81 **and** BN 3035/90.85

8.1 Maximum Tolerable Wander (MTW)

Note: The ANT-20SE's generator is normally synchronized externally in MTW mode. This is done by connecting an appropriate reference signal to socket [25]. Refer to the "Specifications" of the mainframe for details.
An appropriate message will be displayed when the MTW measurement is started if the internal clock source is used for a MTW measurement.

Variable combinations of wander amplitudes and wander frequencies are set once the measurement is started. The output signal is modulated for one period of the wander frequency for each combination of values. The measurement point is then marked as "OK" (no alarms or bit errors detected) or "Failed" (alarms or bit errors detected).

Error source, selectable
SDH . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI
SONET . . . . . TSE (Test Sequence Error, bit error), Code, B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Settling time (wait between measurements) . . . . . .0.1 to 999 s

Settable values of wander frequency
(scan frequency) and wander amplitude . . . . . see Fig. S-5, Page S-26

Display . . . . . table of values

Default settings

Bit rate in kbit/s	f1 / A1 in Hz/UI	f2 / A2 in Hz/UI	f3 / A3 in Hz/UI	f4 / A4 in Hz/UI	f5 / A5 in Hz/UI	f6 / A6 in Hz/UI	Relevant standards
1544	0.014/17	0.16/15	0.16/15	0.19/13	3.9/13	10/5	ITU-T G.824
2048	0.00488/36.9	0.01/18	1.67/18	10/3	-	-	ITU-T G.823
6312	0.01/24.4	0.03/18.9	0.1/14.4	03/11.2	1/8.5	10/5	ITU-T G.824
8448	-	-	-	-	-	-	-
34368	0.01/137.5	0.032/137.5	0.13/34.4	4.4/34.4	10/15.1	-	ITU-T G.823
44736	0.01/120.7	0.03/96.1	0.1/81	0.3/73.2	1.675/65.7	10/11	ITU-T G.824
51840	0.016/103.7	0.05/33.2	0.13/13	10/13	-	-	ITU-T G.813 (Option 1)
139264	0.01/557	0.032/557	0.13/139.3	2.2/139.3	10/30.6	-	ITU-T G.823
155520	0.016/311	0.05/99.5	0.13/38.9	10/38.9	-	-	ITU-T G.813 (Option 1)
622080	0.016/1244	0.5/398	0.13/155.5	10/155.5	-	-	ITU-T G.813 (Option 1)

Table S-29 Settings for wander frequency and wander amplitude for MTW measurements

Note: The masks specified in the standards quoted generally start at lower frequencies (e.g. 12 µHz). These lower wander frequencies result in very long measurement times. They have therefore been omitted in order to reduce measurement times. You can alter the appropriate default settings if you want to make measurements at these lower frequencies.

Notes:

Specifications O.172 Jitter / Wander (2488 Mbit/s Interface)

These Specifications apply to the following options:

- BN 3035/90.88 Jitter Generator / Jitter Analyzer
- BN 3035/90.87 Wander Generator
- BN 3035/90.89 Wander Analyzer

Numbers enclosed in square brackets […] correspond to numbers printed on the instrument.

Calibrated specifications are indicated by ***.

Standards

Jitter is generated and jitter and wander are analyzed in accordance with the following standards:

- ITU-T G.825, O.172
- Bellcore GR-253
- ANSI T1.101, T1.105.03

1 Jitter Generator

Meets or exceeds the requirements of ITU-T O.172

1.1 Bit rate

Bit rate . . . . . 2488320 kbit/s

Maximum offset (Jitter Generator/Analyzer active) . . . . . ±50 ppm

Modulation source . . . . . internal or external

Jitter modulation signal . . . . . sine wave

1.2 Internal modulation source

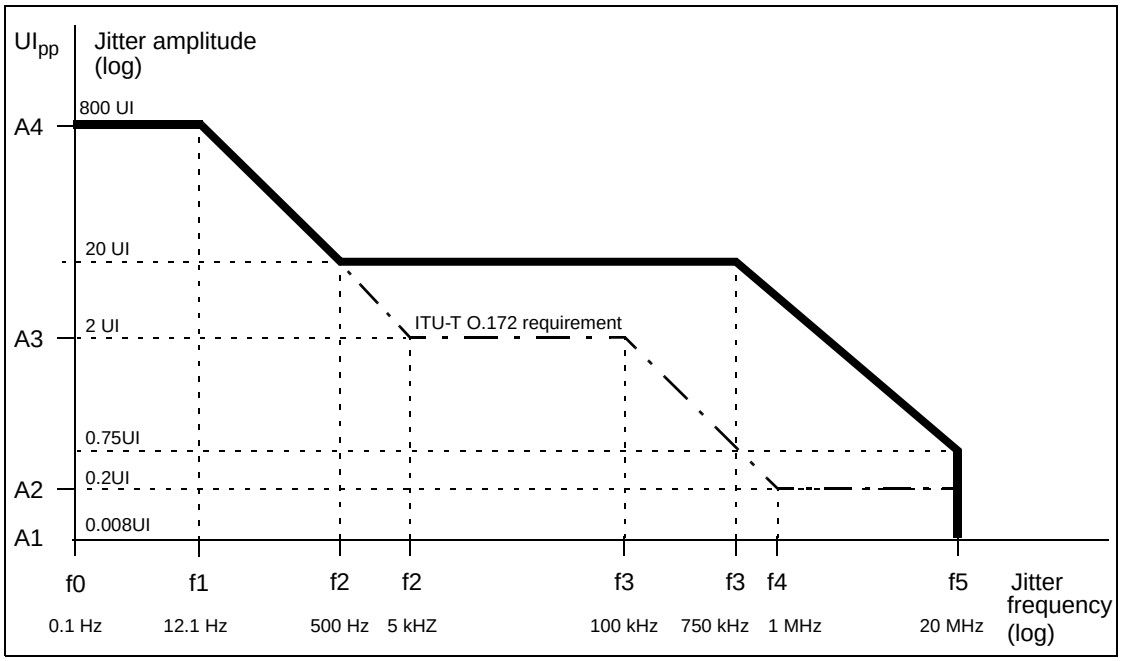


Fig. S-7 Jitter amplitude versus jitter frequency

	Amplitude in UIpp				Frequency in kHz					
Bit rate in kHz	**A1**	**A2**	**A3**	**A4**	**f0**	**f1**	**f2/f2**	**f3/f3**	**f4**	**f5**
ANT-20SE	0.008	0.75	20	800	0.0001	0.0121	0.5	750	-	20000
ITU-T O.172	-	0.2	2	800	0.000125	0.0121	5	100	1000	20000

Table S-30 Jitter amplitude and jitter frequency

Settling time for changes in amplitude . . . . . <2 seconds

Changes in modulation frequency or amplitude are without phase hits.

Jitter frequency setting step width
0.1 Hz to 1 MHz . . . . . 0.1 Hz
above 1 MHz . . . . . 1 Hz

Jitter amplitude setting step width . . . . . 0.001 UI

1.3 External modulation voltage input [50]

Socket . . . . . BNC

Input impedance . . . . . 75 Ω

Frequency range . . . . . 0.1 Hz to 20 MHz

Nominal input voltage range . . . . . 0 to 2.0 V_{pp} (8.2 dBm)

Corresponding jitter amplitude (at 2.0 V_{pp}) . . . . . variable

Maximum permitted input level . . . . . 4.0 V_{pp} (14.2 dBm)

1.4 Error limits

The error limits conform to or are better than the requirements of ITU-T O.172.

1.4.1 Amplitude error***

Amplitude error describes the deviation from the set amplitude for sine wave modulation.

Maximum deviation . . . . . ±Q% of set value ± 0.02 UI_{pp}

Q (variable error) is taken from the following table:

Q (variable error) in %	Frequency range in kHz
8	5 to 500
12	500 to 2000
15	2000 to 20000
Q = 12% below the stated ranges	

Table S-31 Q for various modulation frequencies

1.4.2 Intrinsic jitter

The intrinsic jitter indicates the maximum output jitter of the ANT-20SE for a jitter amplitude setting of 0 UI. A bandwidth between the filters HP1 and LP (see Tab. S-33, Page S-40) is assumed.

Intrinsic jitter . . . . . 0.04 UI

1.4.3 Modulation frequency

Modulation frequency accuracy . . . . . ±0.1%

2 Jitter Analyzer

Meets or exceeds the requirements of ITU-T O.172

2.1 Bit rate

Same as bit rate of STM-16 / OC-48 Module

Bit rate . . . . . 2488320 kbit/s

Permitted offset . . . . . ±20 ppm

RX line code . . . . . NRZ (optical)

2.2 Jitter measurement range

Range 1 . . . . . 0 to 2 UI_{pp}

Range 2 . . . . . 0 to 32 UI_{pp}

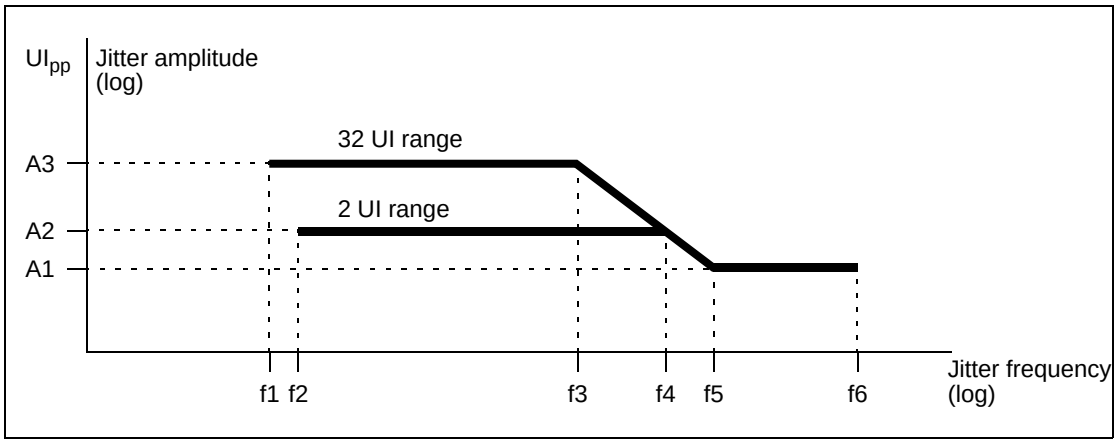


Fig. S-8 Jitter measurement range

Amplitude in UI_{pp}			**Frequency in kHz**					
A1	**A2**	**A3**	**f1**	**f2**	**f3**	**f4**	**f5**	**f6**
0.2	2	32	5 (0.01)	5 (0.08)	6.25	100	1000	20000
f1 = 10 Hz with 5 or 12 kHz high-pass filter deactivated f2 = approx. 80 Hz with 5 or 12 kHz high-pass filter deactivated								

Table S-32 Jitter measurement range

2.3 Weighting filters to ITU-T O.172

High-pass filters . . . . . 5 kHz, 12 kHz and 1000 kHz

High-pass filter characteristic . . . . . 1st order (to ITU-T O.172)

Low-pass filter . . . . . 20000 kHz
Low-pass filter characteristic . . . . . 3rd order Butterworth (to ITU-T O.172)

Filter properties
-3 dB cutoff frequency tolerance . . . . . $f_C \pm 10\%$
Maximum attenuation . . . . . at least 60 dB

Default filter settings to ITU-T O.172 (standard filters):

HP1 + LP		**HP2 + LP**	
High-pass in kHz	**Low-pass in kHz**	**High-pass in kHz**	**Low-pass in kHz**
5	20000	1000	20000

Table S-33 ITU-T filter settings

Frequency range without high-pass filter (lower -3 dB cutoff point):

Range 1 (2 UI_{pp}) . . . . . 80 Hz

Range 2 (32 UI_{pp}) . . . . . 10 Hz

2.4 Demodulator output [51]

Socket . . . . . BNC

Output impedance . . . . . 75 Ω

Output voltage (terminated with 75 Ω)
Range 1 (2 UI_{pp}) 1V/UI
Range 2 (32 UI_{pp}) . . . . . 62.5 mV/UI

2.5 Result display

The positive and negative jitter amplitudes are measured.

Current Values

The current values are displayed continuously or shown as a graph.

Jitter peak-peak . . . . . .peak to peak jitter value

Jitter +peak. . . . . positive peak jitter value

Jitter -peak . . . . . .negative peak jitter value

Current Values display averaging (selectable). . . . . off, 1, 2, 3, 4, 5 seconds

Display resolution (current value)
in range 1 (2 UI_{pp}) . . . . . 0.001 UI_{pp}
in range 2 (32 UI_{pp}) . . . . . 0.01 UI_{pp}

Display range 1 (graphical display)
Jitter peak-peak . . . . . .2 UI_{pp}
Jitter +peak/-peak. . . . . ±1 UI_p

Display range 2 (graphical display)
Jitter peak-peak . . . . . .32 UI_{pp}
Jitter +peak/-peak. . . . . ±16 UI_p

Max. Values

The maximum value is only displayed if a measurement was started in the “Application Manager”.

Jitter peak-peak . . . . . .peak to peak jitter value in measurement interval

Jitter +peak. . . . . .positive peak jitter value in measurement interval

Jitter -peak . . . . . .negative peak jitter value in measurement interval

Display resolution
in range 1 (2 UI_{pp}) . . . . . 0.001 UI_{pp}
in range 2 (32 UI_{pp}) . . . . . 0.01 UI_{pp}

2.6 Error limits for displayed jitter

The error limits for displayed jitter meet the requirements of ITU-T Recommendation O.172.

The stated error limits apply under the following conditions:

- Optical level in the range -10 dBm to -12 dBm (scrambled NRZ)
- Structured signals (framed signals to ITU-T O.172)
- Sine wave modulation
- Standard filters HP1 + LP or HP2 + LP as per Sec. 2.3, Page S-40, Table S-33

The overall measurement error is made up from the following partial errors (additive):

- Measurement error at reference frequency (see Sec. 2.6.1, Page S-42)
- Frequency response error (see Sec. 2.6.2, Page S-43)
- Deviation of filter frequency response from nominal curve (see Sec. 2.3, Page S-40)

2.6.1 Measurement accuracy

The stated measurement accuracy applies under the following conditions:

- Reference frequency: 100 kHz
- The stated measurement error applies without restriction to the smaller measurement range and for values >1 UI in the larger measurement range.

Maximum measurement error***
(excluding frequency response error) . . . . . ±5% of measured value ± W

The value W (fixed error) is taken from the following table:

Filter HP1 + LP	**Filter HP2 + LP**	**HP 80 Hz + LP**	**HP 10 Hz + LP**
W in UI	**W in UI**	**W in UI**	**W in UI**
0.1	0.05[1]	0.2	0.3
1 demonstrated without modulation			

Table S-34 W (fixed error)

Additional error for
optical signals with levels >-10 dBm or <-12 dBm. . . . . typically ≤0.05 UI

2.6.2 Frequency response error***

The following frequency response error can occur in addition to the measurement error at frequencies that are not equal to the reference frequency:

Frequency response error . . . . . .to ITU-T O.172, Table 10

Reference frequency . . . . . 100 kHz

Additional error	Frequency range[1] in kHz
±2%	1 to 300
±3%	300 to 1000
±5%	1000 to 3000
±10%	3000 to 10000
±15%	10000 to 20000

1 Below the stated frequency range, the error which applies there is continued

Table S-35 Frequency response error

The specified frequency response error applies for a jitter amplitude of 0.15 UI_{pp} and an ambient temperature range of +23 ±10 °C.

2.7 RMS jitter

Range and resolution

	2 UI range (peak - peak)	32 UI range (peak - peak)
RMS range	0 to 1 UI	0 to 16 UI
Resolution	0.001 UI	0.01 UI

Table S-36 Range and resolution

Measurement accuracy

Valid if the 12 kHz RMS filter is used with nominal signals.

2 UI range. . . . . .±5% of measured value ± 0.01 UI
32 UI range. . . . . .±5% of measured value ± 0.1 UI

Integration time. . . . . .1, 2, 5, 10, 20, 40, 80 seconds (selectable)

Default setting. . . . . 1 second

2.8 Phase hits

An event is counted if the demodulated jitter signal violates a pre-set positive or negative threshold value. Positive and negative events are counted by separate counters. The counter value indicates the number of times the positive and negative thresholds were violated during the measurement.

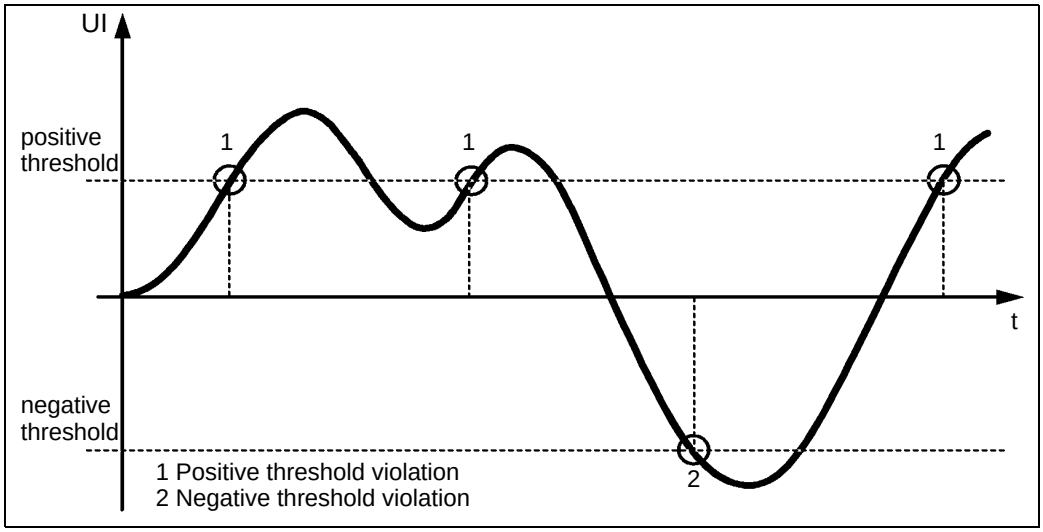


Fig. S-9 Example: Demodulated jitter signal (jitter vs. time function)

Display

- Number of times positive threshold was violated
- Number of times negative threshold was violated

Threshold settings (positive and negative)

Range of values in range 1 (2 UI_{pp}) . . . . . 0.1 UI_p to 1 UI_p
Step width . . . . . 0.1 UI_p
Range of values in range 2 (32 UI_{pp}) . . . . . 0.1UI_p to 16 UI_p
Step width . . . . . 0.1 UI_p

Alarms

Alarms . . . . . LTI (Loss of Timing Information) and AC line power failure

The counters are stopped during an alarm. The count resumes when the alarm is cleared and the gate time has not yet elapsed completely. The occurrence of an alarm is indicated by a yellow warming sign in front of the result. The warning sign is cleared when a new measurement is started.

Maximum count frequency . . . . . approx. 20 kHz (sine wave)

Threshold setting error limits . . . . . ±5% of threshold value, plus jitter meter error

3 Tolerance to jitter measurement

3.1 Fast Maximum Tolerable Jitter (F-MTJ)

Once the measurement is started, selectable jitter amplitude and jitter frequency combinations are set. The result for each combination (test point) is then indicated either as “OK” (no alarms or bit errors) or “Failed” (alarms or bit errors).

Error source selectable from:
SDH . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI
SONET . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Delay (recovery time) . . . . . 0.1 to 999 s

Selectable jitter frequencies (scan frequencies)
and jitter amplitudes . . . . . see Tab. S-30, Page S-36

Display . . . . . table of values

Default settings

f1 / A1 in kHz/UI$_{pp}$	**f2 / A2 in kHz/UI$_{pp}$**	**f3 / A3 in kHz/UI$_{pp}$**	**f4 / A4 in kHz/UI$_{pp}$**	**f5 / A5 in kHz/UI$_{pp}$**
0.012/622	5/1.5	100/1.5	1000/0.15	20000/0.15

Table S-37 Jitter frequency and jitter amplitude settings for Fast-MTJ measurement

The default values in the table represent the corner values of the limit curve specified in ITU-T Recommendation G.825.

3.2 Maximum Tolerable Jitter (MTJ)

Once the measurement is started, the jitter amplitude of the digital signal is altered until the bit error meter detects that a pre-set threshold has been exceeded. The maximum tolerable jitter value that will be shown is one search step less than the value causing the threshold violation.

Error source selectable from:
SDH . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI
SONET . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Delay (recovery time) . . . . . .0.1 to 999 s

Gate time . . . . . 1 to 60 s

The jitter frequencies (scan frequencies) can be user defined as a group of up to 20 freely programmable frequencies in the range from 0.1 Hz to 20 MHz.

Display . . . . . .table of values or log vs. log graph

Tolerance masks can also be displayed.

Default scan frequencies

f1 in kHz	**f2 in kHz**	**f3 in kHz**	**f4 in kHz**	**f5 in kHz**	**f6 in kHz**	**f7 in kHz**	**f8 in kHz**	**f9 in kHz**	**f10 in kHz**
0.012	0.1	1	5	20	100	500	1000	5000	20000

Table S-38 Default scan frequencies

Default tolerance mask

f1 / A1 in kHz/UI_{pp}	**f2/A2 in kHz/UI_{pp}**	**f3 / A3 in kHz/UI_{pp}**	**f4 / A4 in kHz/UI_{pp}**	**f5 / A5 in kHz/UI_{pp}**
0.0121/622	5/1.5	100/1.5	1000/0.15	20000/0.15

Table S-39 Default tolerance mask

4 Jitter Transfer Function

4.1 Jitter Transfer Function measurement

Once the measurement is started, a user-defined amplitude is set at each of the pre-selected jitter frequencies in turn. The Jitter Analyzer determines the jitter transferred by the device under test. The jitter is measured selectively, i.e. using a band-pass filter that is tuned to the modulation frequency. This ensures that interference frequencies outside the pass band of the filter do not affect the result.

The jitter transfer function is calculated from the logarithmic ratio of output jitter to input jitter on a point by point basis:

Jitter transfer function: $H(f_j) = 20 \log \frac{\text{output jitter}}{\text{input jitter}}$

Maximum measurement accuracy is achieved by means of a calibration measurement which can either be performed before every measurement (recommended) or stored for future use. The intrinsic error of the analyzer is determined at every selected scan frequency during a loop measurement (TX linked to RX). This intrinsic error correction is then applied to the results for the device under test as they are measured.

TX jitter settings . . . . . .see Sec. 1, Page S-36

Measurement range, fixed . . . . . 32 UI for f <1 kHz,
4 UI for f ≥1 kHz

Delay (recovery time) . . . . . 0.1 to 999 s

Filter bandwidth (-3 dB) . . . . . 10 Hz

The jitter frequencies (scan frequencies) can be user defined as a group of up to 20 freely programmable frequencies in the range from 10 Hz to 20 MHz.

Display . . . . . table of values or log vs. log graph

Tolerance masks can also be displayed.

Default scan frequencies and amplitudes as per ITU-T G.825 and Bellcore GR-253

f1/Ampl. (kHz/UI)	f2/Ampl. (kHz/UI)	f3/Ampl. (kHz/UI)	f4/Ampl. (kHz/UI)	f5/Ampl. (kHz/UI)	f6/Ampl. (kHz/UI)	f7/Ampl. (kHz/UI)	f8/Ampl. (kHz/UI)
0.1/15	1/3.0	10/1.5	100/1.5	500/0.3	2000/0.15	5000/0.15	20000/0.15

Table S-40 Default scan frequencies and amplitudes

The default scan frequencies and amplitudes correspond to or are below the maximum tolerable jitter limit curves specified in the relevant standards. This ensures that the JTF measurement is not performed using unacceptably high levels of jitter.

Default tolerance mask as per ITU-T G.958, Bellcore GR-253 and ANSI T1.105.03

Frequency in kHz	f1 = 0.01	f2 = 2000	f3 = 20000
Maximum level in dB	0.1	0.1	-19.9
Minimum level in dB	-99.9	-99.9	-99.9

The default lower tolerance mask limit (min. dB) is always -99.9 dB and is not visible in the graph display.

4.2 Measurement error (typical)

The total error F_{total} is made up from the partial errors F1 + F2 + F3.

F1 and F2 depend on the transmitted jitter amplitude (F1) and on the measured jitter amplitude (F2). They can be read off from the diagrams below.
F3 depends on the measured jitter loss D (in dB) and on a bit rate-dependent constant k up to a maximum value,

where: **F3 = D · k**

Note: The value of F3 can never exceed $F3_{MAX}$.

k	**$F3_{MAX}$**
0.1	2 dB

Table S-41 Factor k and the maximum value $F3_{MAX}$

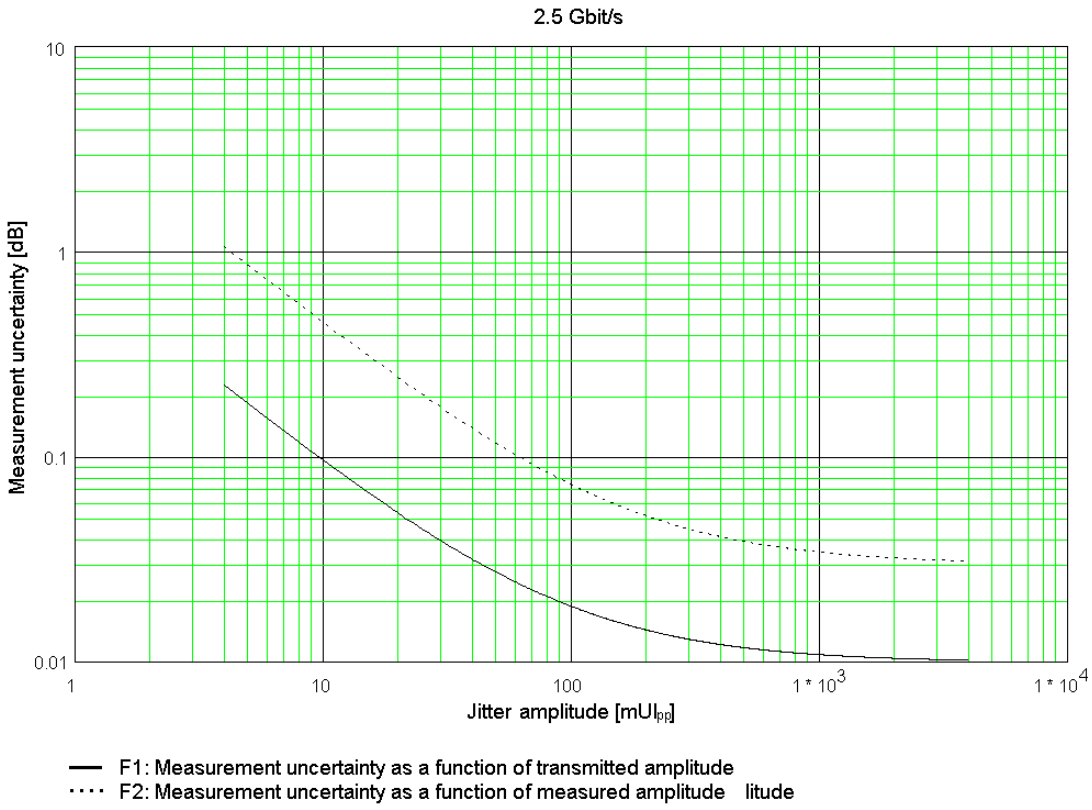


Fig. S-10 Measurement uncertainty at 2.5 Gbit/s

All data applies under the following conditions:

- Nominal optical level
- Temperature: 20 °C to 26 °C
- Integration time: 5 s
- Settling time: 1 s
- Complete instrument warm-up time: 30 minutes
  The relevant optical bit rate (STM-16) must also have been activated for at least five minutes.
- Calibration immediately before the measurement
- Jitter amplitude on jitter meter: 4 mUI to 4 UI
- Frequency range: 1 kHz to 20 MHz

Example

A jitter transfer of -21 dB is measured at a transmitted amplitude of 1000 mUI_{pp}.

To calculate the total error, errors F1 and F2 are taken from Fig. S-10. Error F3 is calculated using the relationship given above (k is taken from Table S-41).

F1 = 0.011 dB (from Fig. S-10)

The jitter transfer function

$$H(f_j) = 20 \log \frac{\text{measured jitter}}{\text{transmitted jitter}} = 20 \log \frac{x}{1000\ mUI} = -21\ dB$$

gives a measured jitter of approximately 90 mUI.

This value can be used to read the value of F2 from Fig. S-10.

F2 = 0.08 dB (from Fig. S-10)

F3 = 21 dB · 0.1 = 2.1 dB

F3 is greater than $F3_{MAX}$ in Table S-41 (2.0 dB). The value $F3_{MAX}$ = 2.0 dB is therefore substituted for F3.

$$\mathbf{F_{total}} = 0.011\ dB + 0.08\ dB + 2.0\ dB \mathbf{= 2.091\ dB}$$

F1 F2 F3

5 Wander Generator

Only possible if options BN 3035/90.88 **and** BN 3035/90.87 **and** BN 3035/90.81 are fitted.

5.1 Bit rate

Bit rate . . . . . 2488320 kbit/s

Wander modulation shape. . . . . sine wave

Frequency range . . . . . 10 µHz to 10 Hz

Wander frequency setting step width . . . . . 1 µHz

Amplitude range . . . . . 0.1 UI to 200000 UI

Wander amplitude setting step width. . . . . 0.1 UI

5.2 Wander amplitude, wander frequency and clock offset

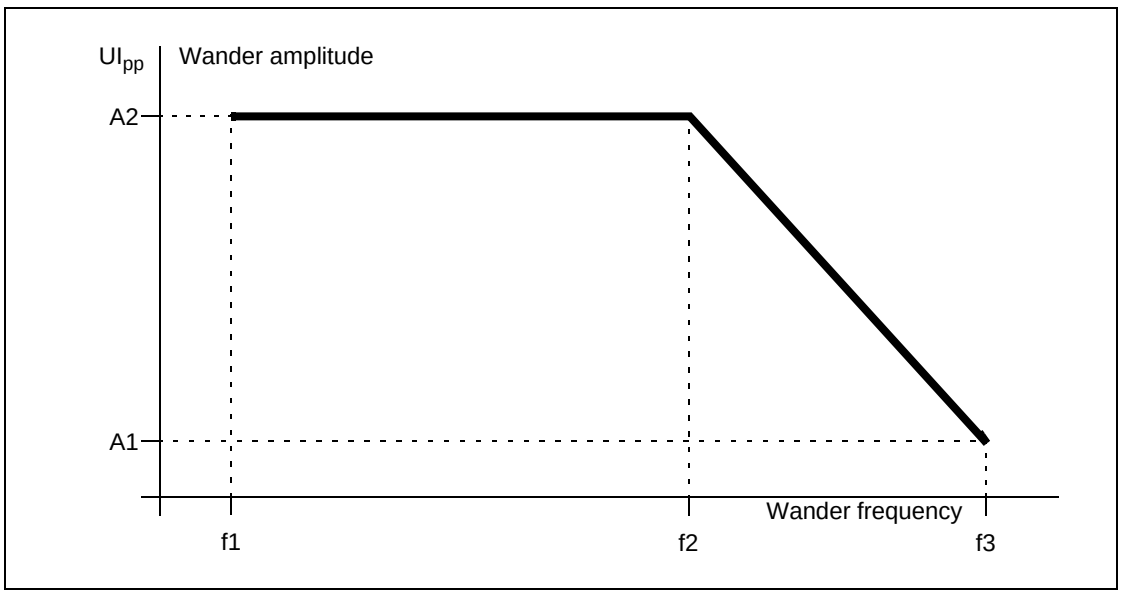


Fig. S-11 Maximum wander amplitude as a function of the wander frequency with the parameter of clock offset

Clock offset	A1 in UI	A2 in UI	f1 in µHz	f2 in Hz	f3 in Hz
0 ppm	2340	200000	10	0.117	10
50 ppm	390	200000	10	0.0195	10

Table S-42 Maximum wander amplitude as a function of the wander frequency with the parameter of clock offset

The maximum values for the amplitude / frequency combinations that can be set depend on the clock offset.

At a given modulation frequency, the maximum settable amplitude is the value 200000 UI or the value calculated from the following equation, whichever is the smaller:

$$A_{max} = \frac{23400 - 390 \times \Delta f}{f_{mod}}$$

A_{max} = maximum settable amplitude in UI

Δf = magnitude of clock offset in ppm

f_{mod} = modulation frequency in Hz

5.3 Error limits

5.3.1 Amplitude error

Amplitude error describes the deviation from the set amplitude for sine wave modulation.

Maximum deviation . . . . . ±8% of set value ± 0.02 UI_{pp}

5.3.2 Intrinsic jitter / wander

The intrinsic jitter / wander indicates the maximum output jitter / wander of the ANT-20SE for a jitter / wander amplitude setting of 0 UI. A bandwidth between the filters HP1 and LP (see Tab. S-33, Page S-40) is assumed.

Intrinsic jitter / wander . . . . . 0.04 UI

5.3.3 Modulation frequency

Modulation frequency accuracy . . . . . ±0.1%

5.4 Synchronization

In Wander Generator mode, the generator of the ANT-20SE is normally synchronized to an external source. The appropriate reference signal should be fed into socket [25]. Refer to the “Specifications” for the mainframe instrument.

6 Wander Measurement

Only possible if options BN 3035/90.88 **and** BN 3035/90.89 are fitted.

6.1 Reference clock [54]

Tip: Wander measurements can only be performed using an external reference signal. This signal must conform with the clock frequencies and input levels specified below.

Socket . . . . . BNC

Input impedance . . . . . 75 Ω

Clock frequencies . . . . . 1.544; 2.048; 5; 10 MHz

Permitted input level . . . . . 0.5 to 5 V_{pp}

Monitoring . . . . . LTI (Loss of Timing Information)

6.2 Measurement range

Wander amplitude range . . . . . $\pm 1 \times 10^6$ s

Maximum permitted phase change rate
Sample rate 1/s . . . . . 1000 UI/s
Sample rate ≥ 30/s . . . . . 10000 UI/s

The upper limit of the wander frequency range is set by a first-order low-pass filter. The low-pass filter is selected automatically to correspond with the selected sample rate.

Sample rate	**Low-pass filter/f_C**
1/s	0.1 Hz
30/s	10 Hz
60/s	20 Hz
300/s	100 Hz

Table S-43 Low-pass filters for various sample rates

Low-pass filter

Filter characteristic . . . . . 1st order low-pass filter

Measurement bandwidth . . . . . 0 Hz to f_{LIM}

Deviation in -3 dB cutoff frequency. . . . . f_{LIM} ± 10%

Maximum attenuation . . . . . .at least 30 dB

1 Hz to 10 Hz passband ripple
(referred to attenuation at 0.1 Hz) . . . . . <±0.2 dB

6.3 Result display

Result displayed in seconds
TIE (instantaneous value) . . . . . numerically and graphically
MTIE (maximum difference) . . . . . numerically

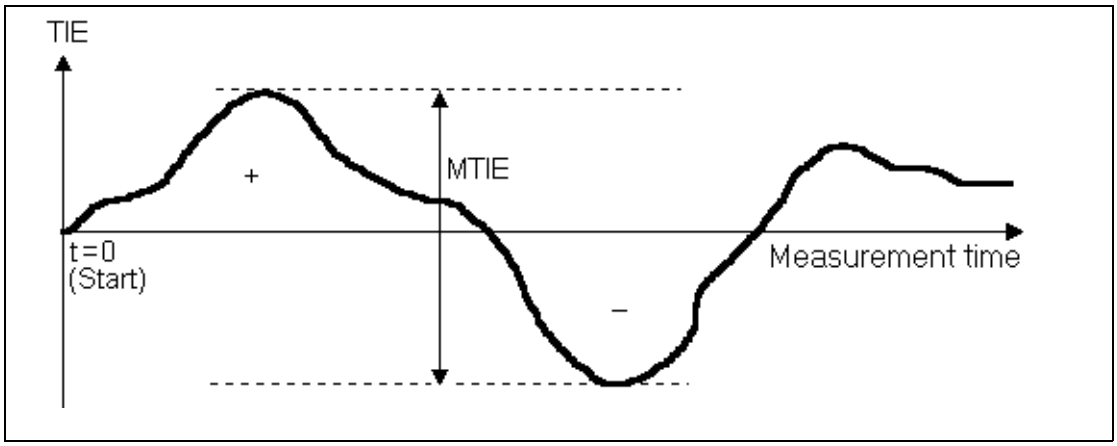


Fig. S-12 Example: Wander measurement versus measurement time

6.4 Accuracy

The specified measurement error applies after a warm-up period of at least 30 minutes for the ANT-20SE and a maximum change in ambient temperature of 5 K.

Overall TIE error for each TIE measurement
for an observation interval τ. . . . . <±5% of measured TIE value ± Z_0

Z_0 is taken from the following table:

Z_0 (τ)/ns	**Observation interval τ/s**
2.5 + 0.0275 τ	0.05 ≤ τ ≤ 1000
29 + 0.001 τ	τ > 1000

Table S-44 Error Z_0

6.5 Memory requirements

Before starting a long-term wander measurement, check the available hard disk space. The ANT-20SE software calculates the expected hard disk space requirements from the selected gate time and sample rate. A warning message is displayed if there is insufficient space.

Sample rate	Memory requirements
1/s	approx. 58 kB/h
30/s	approx. 1.65 MB/h
60/s	approx. 3.3 MB/h
300/s	approx. 16.5 MB/h

Table S-45 Memory requirements versus sample rate

7 Measurement of Maximum Tolerable Wander

only possible with options BN 3035/90.88 **and** BN 3035/90.87 **and** BN 3035/90.81

7.1 Maximum Tolerable Wander (MTW)

Note: The ANT-20SE's generator is normally synchronized externally in MTW mode. This is done by connecting an appropriate reference signal to socket [25]. Refer to the "Specifications" of the mainframe for details.
An appropriate message will be displayed when the MTW measurement is started if the internal clock source is used for a MTW measurement.

Variable combinations of wander amplitudes and wander frequencies are set once the measurement is started. The output signal is modulated for one period of the wander frequency for each combination of values. The measurement point is then marked as "OK" (no alarms or bit errors detected) or "Failed" (alarms or bit errors detected).

Error source, selectable
SDH . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, MS-REI, MS-RDI, HP-REI, HP-RDI, LP-REI, LP-RDI
SONET . . . . . TSE (Test Sequence Error, bit error), B1, B2, B3, REI-L, REI-P, REI-V, RDI-L, RDI-P, RDI-V

Error threshold . . . . . 0 to 999999

Settling time (wait between measurements). . . . . 0.1 to 999 s

Settable values of wander frequency
(scan frequency) and wander amplitude . . . . . see Tab. S-42, Page S-50

Display . . . . . table of values

Default settings

Bit rate in kbit/s	f1 / A1 in Hz/UI	f2 / A2 in Hz/UI	f3 / A3 in Hz/UI	f4 / A4 in Hz/UI	f5 / A5 in Hz/UI	f6 / A6 in Hz/UI	Relevant standards
2488320	0.016/4977	0.05/1593	0.13/622	10/622	-	-	ITU-T G.813 (Option 1)

Table S-46 Settings for wander frequency and wander amplitude for MTW measurements

Note: The masks specified in the standards quoted generally start at lower frequencies (e.g. 12 µHz). These lower wander frequencies result in very long measurement times. They have therefore been omitted in order to reduce measurement times. You can alter the appropriate default settings if you want to make measurements at these lower frequencies.

Notes:

ANT-20SE
Advanced Network Tester

ATM Module

BN 3060/90.50

Software Version 7.20

Specifications

6

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications ATM Module

Notes:

Specifications ATM Module

These specifications include the option BN 3035/90.70 (ATM Functions).

The ATM Mappings specifications are include in the operating manual BN 3035/98.15.

1 ATM generator

1.1 Scrambling

Scrambling is as per ITU-T recommendation I.432 ($X^{43}+1$).
The function can be disabled.

1.2 Error insertion (anomalies)

The following anomalies can be inserted in addition to the error types described in the Mainframe “Specifications”.

Error type: Anomaly	**Single**	**Rate[1]**	**Sensor thresholds**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
AAL-1 Cell loss	yes	1E-3 to 1E-6	-
AAL-1 CRC	yes	1E-3 to 1E-6	-
AAL-1 PE	yes	1E-3 to 1E-6	-

1 Mantissa: 1 only, exponent: -1 to -6 (integer values)
2 Non-correctable header errors
3 Correctable header errors

Table S-1 Error types (anomalies) available in addition to the Mainframe

AAL-1 Cell loss, AAL-1 CRC and AAL-1 PE errors refer to the test channel (foreground channel). Test sequence errors (TSE) are inserted in the ATM payload or in the AAL-1 payload of the test channel.
Correctable and non-correctable header errors will be inserted in the overall cell stream.

1.3 Alarm generation (defects)

The following defects can be generated in addition to the alarm types described in the Mainframe “Specifications”.

Defect	Sensor function test	Single
	On/Off	
LCD[1]	yes	yes
VC-AIS[2]	yes	yes
VC-RDI[3]	yes	yes
VP-AIS	yes	yes
VP-RDI	yes	yes
Vx-AIS[4]	yes	yes
Vx-RDI[4]	yes	yes

1 LCD (Loss of Cell Delineation) is generated by a non-correctable header error in ≥ 7 consecutive cells.
2 AIS: Alarm Indication Signal; VC: Virtual Channel; VP: Virtual Path
3 RDI: Remote Defect Indication
4 For Vx-AIS and Vx-RDI the alarms are inserted simultaneously in VP and VC.

Table S-2 Alarm types (defects) available in addition to the Mainframe

1.4 Test channel

Cells

Header

UNI/NNI, VCI, VPI, PT and CLP . . . . . user-settable
HEC . . . . . formed automatically

Payload

Pseudo random sequences . . . . . PRBS 11, PRBS 15, PRBS 20, PRBS 23
Digital word . . . . . 16 bits

Load profile

Constant, Equidistant, Burst

Constant

Load setting . . . . . 0.01% to 100%

Resolution for load range settings
from 0.01% to 0.99% 0.01%
from 0.1% to 9.9% 0.1%
from 1% to 100% 1%

Equidistant

Setting range
Cell spacing . . . . . 1 to 10000 cell periods

Resolution for cell spacing range settings
from 1 to 100 . . . . . 1 cell period
from 10 to 1000 . . . . . 10 cell periods
from 100 to 10000 . . . . . 100 cell periods

Burst

Setting range
Maximum burst length . . . . . 1023 cells / 2.79 ms
Burst load . . . . . 0 to 100%
Resolution . . . . . depends on burst length

Maximum burst period . . . . . 32767 cells / 89 ms

Load units . . . . . Mbit/s, Cells/s, %
Time units . . . . . µs, cell periods

1.5 Background load

The background load is generated from memory-based sequences. Foreground traffic (test channel) has priority.

Header . . . . . freely settable
Payload . . . . . bytewise constant, byte freely settable
Maximum load cell repeat factor (n1) 255
Maximum number of empty cell following a load cell (n2) 1023
Maximum sequence repeat factor (n1 load cells, n2 empty cells) 255
Maximum number of sequences 200

1.6 Fill cells

The cell stream is filled using IDLE or UNASSIGNED cells.
The type of cell used can be switched.

1.7 AAL-1 segmentation

Unframed signals with system bandwidths of 1.5 Mbit/s, 2 Mbit/s, etc., can be transmitted in the AAL-1 PDU in the test channel.

Possible payload patterns at 2 Mbit/s . . . . . PRBS unframed, PRBS in PCM30, PRBS in PCM30CRC

2 ATM receiver

2.1 Descrambling

Descrambling is as per ITU-T recommendation I.432 ($X^{43}+1$).
The function can be disabled.

2.2 Measurement modes

2.2.1 Error measurement (anomalies)

The following anomalies can be evaluated and displayed in addition to those described in the Mainframe “Specifications”, section 2.3.3.

Anomaly	**LED**	**Explanation**	
HCOR	-	Correctable Header Error	
HUNC	-	Uncorrectable Header Error	
CER	-	Cell Error Ratio	Test cell measurements
CLR	-	Cell Loss Ratio	
CMR	-	Cell Misinsertion Rate	
AAL-1-CRC	-	AAL1 CRC Error	AAL-1 measurements
AAL-1-PE	-	AAL1 Parity Error	
AAL-1-CLR	-	AAL1 Cell Loss Ratio	
AAL-1-CMR	-	AAL1 Cell Misinsertion Rate	

Table S-3 Display and evaluation of anomalies

HUNC, HCOR errors refer to the overall cell stream, all other errors refer to the test channel.

2.2.2 Alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm types described in the Mainframe “Specifications”, section 2.3.1.

Defect	LED	Explanation	
LCD	LOF / LCD	Loss of Frame/Loss of Cell Delineation	
OCLR	-	Cell Loss Overflow[1]	Test cell measurements
OCMR	-	Cell Misinserted Overflow[2]	
VC-AIS	-	Virtual Channel Alarm Indication Signal	
VC-RDI	-	Virtual Channel Remote Defect Indication	
VP-AIS	-	Virtual Path Alarm Indication Signal	
VP-RDI	-	Virtual Path Remote Defect Indication	
AAL-1-OOS	-	AAL1 Out of Sync	

1 more than 255 lost cells within 100 ms or relative to last test cell
2 more than 255 misinserted cells within 100 ms or relative to last test cell

Table S-4 LED displays indicating additional alarms

2.2.3 ATM performance measurements

Error Related Performance Parameters

The measurement is made using the test cells.

Results

Lost Cell Count, Cell Loss Ratio . . . . . CLR
Misinserted Cell Count, Cell Misinserted Rate . . . . . CMR
Error Cell Count, Cell Error Ratio . . . . . CER

Cell Transfer Delay

The measurement “Cell Transfer Delay” is made using the test cells.

Display . . . . . rate distribution
Resolution . . . . . 160 µs to 0.355 s
Range . . . . . 20 µs to 42.9 s
Range offset . . . . . 0 to 0.167 s
Units . . . . . µs

Cells with delay times outside the measurement range will be assigned to class 0 (underflow) or class 127 (overflow).

Cell Delay Variation

The measurement “Cell Delay Variation” is made using the test cells.

Display . . . . . rate distribution,
minimum cell delay,
maximum cell delay,
mean cell delay,
2-Point-CDV, (Peak-to-peak-CDV)

Results are valid only if no delay times outside the measurement range are detected.

2.2.4 Payload channel analysis and load measurement

Cell filters (VCI, VPI) for extracting the test channel.

The VCI filter can be disabled.

Average cell rate

The measurement is made over all connections and in the test channel simultaneously.

Measurement interval . . . . . 1 s
Resolution 0.01%

Load indicator

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Peak cell rate

The measurement is made in the test channel.

Measurement interval . . . . . 1 s
Resolution 0.1%

Load indicator

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Channel loading histogram

Measurement interval . . . . . 100 ms
Number of classes 101
Class “0” contains the number of 100 ms intervalls in which a load of 0 % is measured.
Class width 1
Load indicator . . . . . Mbit/s, Cells/s, %

Payload channel cell distribution

Display of payload channel cells classified into payload cells, OAM cells and payload cells with CLP marked

Measurement interval . . . . . 1 s
Display . . . . . cell count

Test cell format

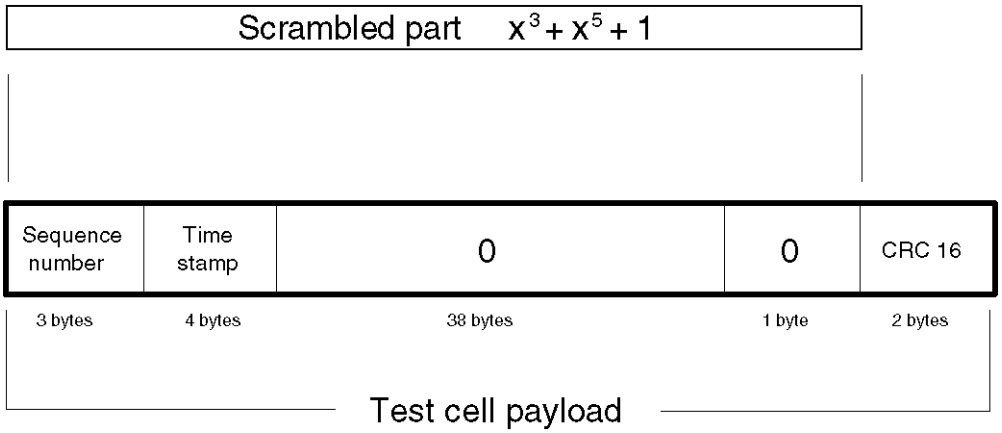


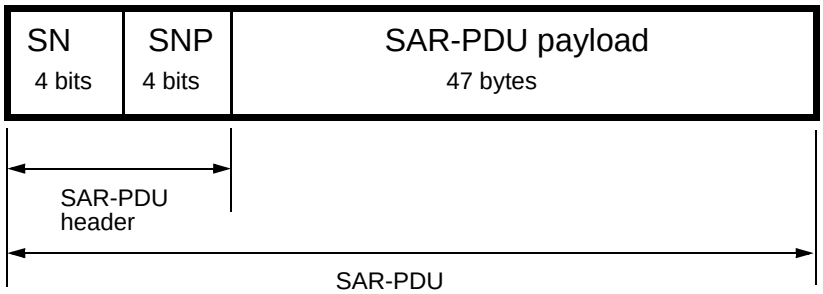
Fig. S-1 Test cell format as per ITU-T O.191 (Draft 4/95)

2.2.5 AAL-1 Reassembly

Reassembly of AAL-1 structured cells is from the SAR-PDU. The format is shown in Fig. S-2, Page I-9. The “TSE” error measurement is made using framed or unframed PRBS mapped into the SAR-PDU payload.

The following payload patterns are available for error measurements:

- PRBS unframed
- PRBS in PCM30 frame
- PRBS in PCM30 frame (with CRC)



SN: Sequence Number
SNP: Sequence Number Protection
PDU: Protocol Data Unit
SAR: Segmentation and Reassembly

Fig. S-2 SAR-PDU format for AAL-1 cells

Notes:

ANT-20SE
Advanced Network Tester

ATM Mappings

BN 3060/90.52 and BN 3060/90.53

for ATM modul BN 3060/90.50
and Broadband Analyzer/Generator BN 3060/90.51

Software Version 7.20

Specifications

6

WAVETEK
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Communications Test Solutions

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Specifications ATM Mappings

Specifications ATM Mappings

1 STM-1 C4, ATM in 155.52 Mbit/s mapping

This mapping structure is included in the following instrument versions and options:

- ATM Module, BN 3035/90.70
- Broadband Analyzer/Generator, BN 3035/90.80

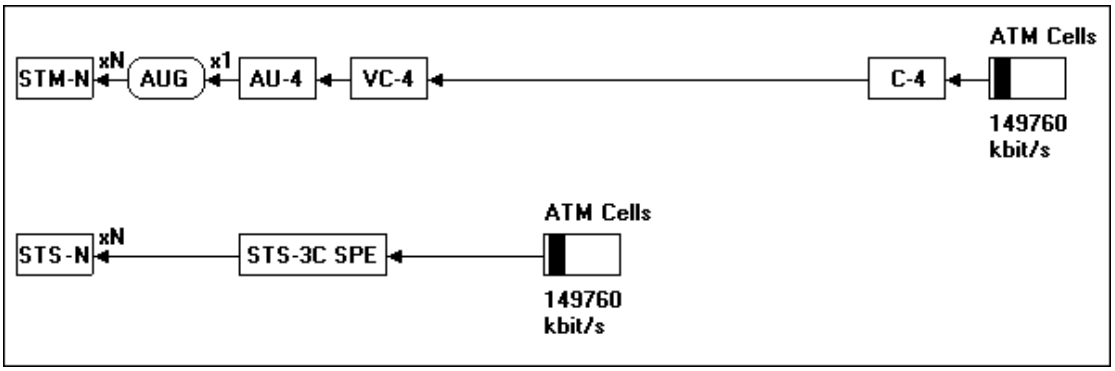


Fig. S-1 150 Mbit/s in STM-1/STS-3c ATM cell stream mapping structure

For the following topics please refer to the specifications of the “STM-1 Mappings” file:

- Overhead
- Alarm generation (defects)
- Error insertion (anomalies)
- Overhead evaluation
- Error measurement (anomalies)
- Alarm detection (defects)

2 STS-3c, ATM in 155.52 Mbit/s mapping

This mapping structure is included in the following instrument versions and options:

- ATM Module, BN 3035/90.70
- Broadband Analyzer/Generator, BN 3035/90.80

For the following topics please refer to the specifications of the “STS-1 Mapping” file (section “STS-3c Mapping”:

- Overhead
- Alarm generation (defects)
- Error insertion (anomalies)
- Overhead evaluation
- Error measurement (anomalies)
- Alarm detection (defects)

3 STS-1, ATM in 51.840 Mbit/s mapping

Option 3035/90.71

- Includes the ATM mapping for STS-1 in accordance with ITU-T G.707 and ANSI Draft T1.105.02-199X.

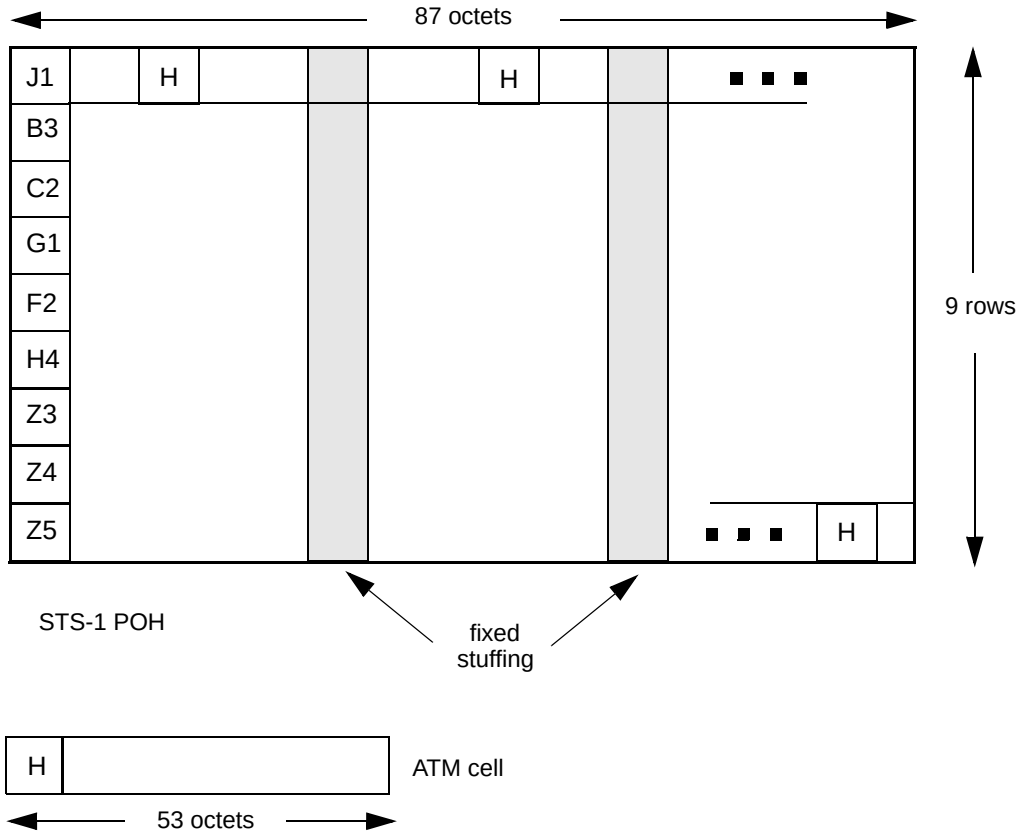


Fig. S-2 ATM mapping for STS-1 (51.840 Mbit/s)

For the following topics please refer to the specifications of the “STS-1 Mapping” file:

- Overhead
- Alarm generation (defects)
- Error insertion (anomalies)
- Overhead evaluation
- Error measurement (anomalies)
- Alarm detection (defects)

4 E4, ATM in 139.264 Mbit/s mapping

Option 3035/90.72

- Frames to G.832.
- ATM mapping to G.804.

4.1 Overhead

Overhead byte	Option 3035/90.72
FA1(hex)	“F6”
FA2 (hex)	“28”
EM (hex)	Inserted via parity formation
TR (ASCII)	“WG E4-TRACE”
MA (hex)	“10”
NR (hex)	“00”
GC (hex)	“00”
P1 (hex)	“00”
P2 (hex)	“00”

Table S-1 Overhead contents

4.2 Alarm generation (defects)

The following alarm types (defects) can be generated:

Defect	Sensor function test	Sensor thresholds
	On/Off	M in N
AIS	Yes	-
LOF	Yes	M = 1 to N-1; N = 1 to 8001
RDI	Yes	M = 1 to N-1; N = 1 to 8001
UNEQ	Yes	M = 1 to N-1; N = 1 to 8001
PLM	Yes	M = 1 to N-1; N = 1 to 8001
TIM	ja	-

Table S-2 Available alarm types (defects)

4.3 Error insertion (anomalies)

Trigger modes . . . . . Single or Rate

Error type, anomaly	Single	Rate
FAS	Yes	2E-3 to 1E-8
EM (BIP-8)	Yes	2E-3 to 1E-10
REI	Yes	5E-5 to 1E-10

Table S-3 Available error types (anomalies) and trigger modes

4.4 Error measurement (anomalies)

The following anomalies can be evaluated and displayed in addition to those described in the Mainframe “Specifications”.

Anomaly	LED
FAS	FAS
EM (BIP-8)	B1/B2
REI	-

Table S-4 LED indication of possible anomalies

4.5 Alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm types described in the Mainframe “Specifications”.

Defect	LED
AIS	AIS
LOF	LOF/OOF
RDI	RDI
UNEQ	HP-UNEQ
PLM	HP-PLM
TIM	-

Table S-5 LED indication of possible defects

5 E3, ATM in 34.368 Mbit/s mapping

Option 3035/90.74

- Frames to G.832.
- ATM mapping to G.804

5.1 Overhead

Overhead byte	Option 3035/90.74
FA1(hex)	“F6”
FA2 (hex)	“28”
EM (hex)	Inserted via parity formation
TR (ASCII)	“WG E3-TRACE
MA (hex)	“10”
NR (hex)	“00”
GC (hex)	“00”

Table S-6 Overhead contents

5.2 Alarm generation (defects)

The following alarm types (defects) can be generated:

Defect	Sensor function test	Sensor thresholds
	On / Off	M in N
AIS	Yes	-
LOF	Yes	M = 1 to N-1; N = 1 to 8001
RDI	Yes	M = 1 to N-1; N = 1 to 8001
UNEQ	Yes	M = 1 to N-1; N = 1 to 8001
PLM	Yes	M = 1 to N-1; N = 1 to 8001
TIM	Yes	-

Table S-7 Available alarm types (defects)

5.3 Error insertion (anomalies)

Trigger modes . . . . . Single or Rate

Error type, anomaly	Single	Rate
FAS	Yes	2E-3 to 1E-8
EM (BIP-8)	Yes	2E-3 to 1E-10
REI	Yes	2E-4 to 1E-10

Table S-8 Available error types (anomalies) and trigger modes

5.4 Error measurement (anomalies)

The following anomalies can be evaluated and displayed in addition to the error types available in the Mainframe.

Anomaly	LED
FAS	FAS
EM (BIP-8)	B1/B2
REI	-

Table S-9 LED indication of possible anomalies

5.5 Alarm detection (defects)

The following defects can be evaluated and displayed in addition to the alarm types available in the Mainframe.

Defect	LED
AIS	AIS
LOF	LOF/OOF
RDI	RDI
UNEQ	HP-UNEQ
PLM	HP-PLM
TIM	-

Table S-10 LED indication of possible defects

6 E1, ATM in 2.048 Mbit/s mapping

Option 3035/90.75

- ATM mapping according to ITU-T G.804.

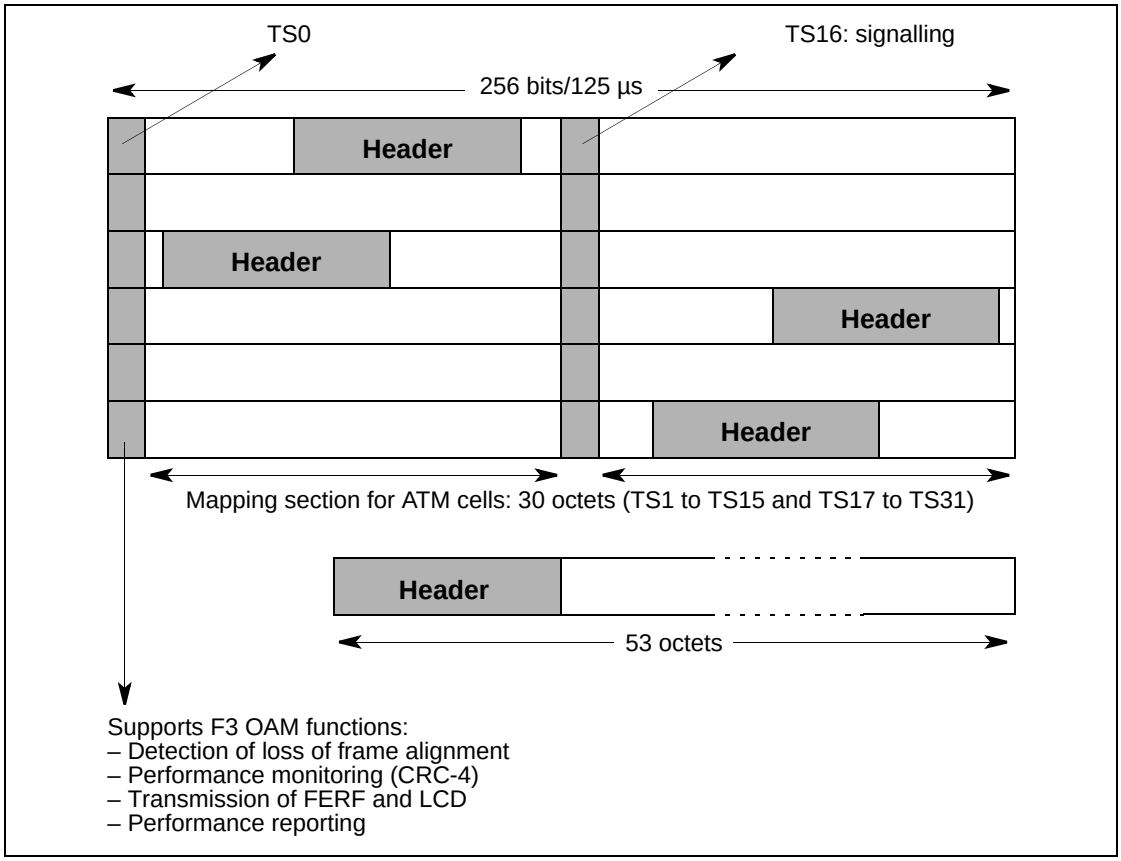


Fig. S-3 ATM mapping for E1 (2048 kbit/s)

For the following topics please refer to the specifications of the “STM-1-Mapping” file:

- Alarm generation (defects)
- Error insertion (anomalies)
- Error measurement (anomalies)
- Alarm detection (defects)

7 DS3, ATM in 44.736 Mbit/s mapping (PLCP, HEC based)

Option 3035/90.73

7.1 PLCP-based Mapping

The ATM cells are firs mapped into PLCP frames (Physical Layer Convergence Protocol) as per G.804. The PLCP frame slips bit-synchronously (Nibble-aligned floating-4 bit) into DS3 C Parity frames as per G.804 (G.704). For more information refer to the specifications of the “STS-1 Mapping” file (section “DS3 Mapping”):

7.1.1 Overhead

DS3: PLCP based ATM mapping

O H						
	1	**2**	**3 (POI)**	**4 (POH)**	**5**	**6**
1	A1 F6	A2 28	P11 2C	Z6 00	ATM Cell	
2	A1 F6	A2 28	P10 29	Z5 00	ATM Cell	
3	A1 F6	A2 28	P09 25	Z4 00	ATM Cell	
4	A1 F6	A2 28	P08 20	Z3 00	ATM Cell	
5	A1 F6	A2 28	P0 1C	Z2 00	ATM Cell	
6	A1 F6	A2 28	P06 19	Z1 00	ATM Cell	
7	A1 F6	A2 28	P05 15	X 00	ATM Cell	
8	A1 F6	A2 28	P04 10	B1	ATM Cell	
9	A1 F6	A2 28	P03 0D	G1 00	ATM Cell	
10	A1 F6	A2 28	P02 08	X 00	ATM Cell	
11	A1 F6	A2 28	P01 04	X 00	ATM Cell	
12	A1 F6	A2 28	P00 01	C1	ATM Cell	Trailer C

All values are hexadecimal.

B1 is formed from the POH and ATM cells of the 12 rows of the previous frame.

7.1.2 Alarm generation (defects)

The following alarm types (defects) can be generated:

Defect	Sensor function test	Sensor thresholds
	on/off	M in N
AIS_DS3	yes	-
IDLE_DS3	yes	-
LOF_DS3	yes	-
YELLOW_DS3 (RDI)	yes	-
PLCP_LOF	yes	M = 1 to N-1; N = 1 to 8000
PLCP_RAI	yes	

Table S-11 Available alarm types (defects)

7.1.3 Error insertion (anomalies)

Trigger types . . . . . Single error, error rate

Error type, anomaly	Single	Rate
FE_DS3	yes	-
Parity_DS3	yes	-
FEBE_DS3	yes	-
PLCP_FAS	yes	1E-3 to 1E-7
PLCP_B1	yes	1E-3 to 1E-8
PLCP_REI(FEBE)	yes	1E-3 to 1E-8

Table S-12 Available error types (anomalies) and trigger types

7.1.4 Error measurement (anomalies)

The following error types can be displayed and evaluated in addition to the error types provided by the Mainframe.

Anomaly	**LED**
FE_DS3, MFE_DS3	FAS/CRC
P_DS3, CP_DS3	-
FEBE_DS3	-
PLCP_FAS	FAS/CRC
PLCP_B1	B1/B2
PLCP_REI (FEBE)	-

Table S-13 LED display of possible anomalies

7.1.5 Alarm detection (defects)

The following alarms can be displayed and evaluated in addition to the defects provided by the Mainframe.

Defect	**LED**
AIS_DS3	AIS
LOF_DS3, OOF_DS3	LOF/LCD
YELLOW_DS3	RDI
IDLE_DS3	-
PLCP_LOF	LOF/LCD
PLCP_RAI	-

Table S-14 LED display of possible defects

7.2 HEC-based Mapping

The G.704 multiframe is used for HEC-based mapping of ATM cells into 44.736 Mbit/s as per G.804.

7.2.1 Alarm generation (defects)

Defect	**Sensor function test**
	on/off
AIS_DS3	yes
IDLE_DS3	yes
LOF_DS3	yes
YELLOW_DS3 (RDI)	yes

Table S-15 Alarm generation (defects): Available alarm types

7.2.2 Error insertion (anomalies)

Error type, anomaly	**Single**
FE_DS3	yes
Parity_DS3	yes
FEBE_DS3	yes

Table S-16 Error insertion (anomalies): Available error types and trigger types

7.2.3 Error measurement (anomalies)

Anomaly	**LED**
FE_DS3, MFE_DS3	FAS/CRC
P_DS3, CP_DS3	-
FEBE_DS3	-

Table S-17 Error measurement (anomalies): LED display of possible anomalies

7.2.4 Alarm detection (defects)

Defect	LED
AIS	AIS
LOF_DS3, OOF_DS3	LOF/LCD
YELLOW_DS3	RDI
IDLE_DS3	-

Table S-18 Alarm detection (defects): LED display of possible defects

8 DS1, ATM in 1.544 Mbit/s mapping

Option 3035/90.76

8.1 Alarm generation (defects)

Defect	Sensor function test
	on/off
AIS_DS1	yes
LOF_DS1	yes
YELLOW_DS1	yes

Table S-19 Alarm generation (defects): Available defects

8.2 Error insertion (anomalies)

Trigger types . . . . . .Single error

Anomaly	Single
FE_DS1	yes
CRC6	yes

Table S-20 Error insertion (anomalies): Available anomalies and trigger mode

8.3 Error measurement (anomalies)

The following error types can be displayed and evaluated in addition to the error types provided by the Mainframe.

Anomaly	LED
FE_DS1	FAS/CRC
CRC6	FAS/CRC

Table S-21 Error measurement (anomalies): LED display of available anomalies

8.4 Alarm detection (defects)

The following alarms can be displayed and evaluated in addition to the defects provided by the Mainframe.

Defect	**LED**
AIS_DS1	AIS
LOF_DS1, OOF_DS1	LOF/LCD
YELLOW_DS1	RDI

Table S-22 Alarm detection (defects): LED display of available defects

9 STM-1 C3, ATM in 155.52 Mbit/s mapping

Option 3035/90.77

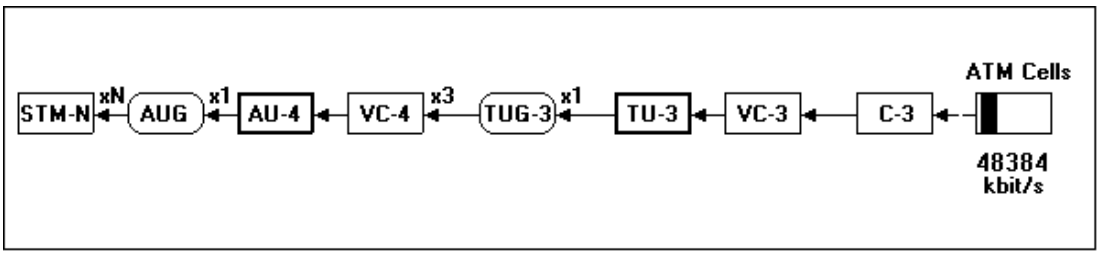


Fig. S-4 Mapping structure AU-4: ATM → C-3 → AU-4 → STM-1

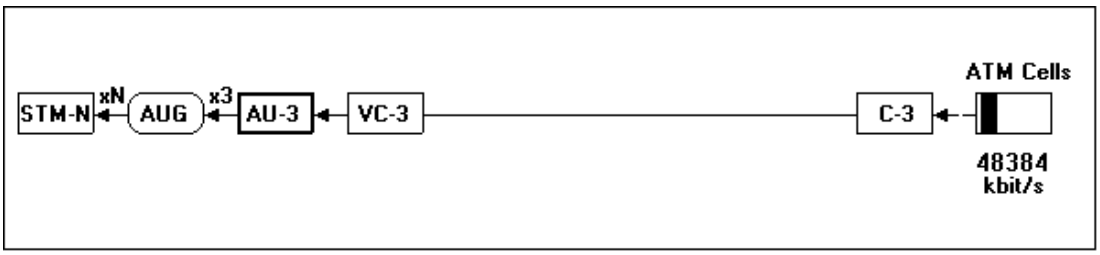


Fig. S-5 Mapping structure AU-3: ATM → C-3 → AU-3 → STM-1

For the following topics please refer to the specifications of the “STM-1Mapping” file:

- Overhead
- Alarm generation (defects)
- Error insertion (anomalies)
- Overhead evaluation
- Error measurement (anomalies)
- Alarm detection (defects)

10 STS-1 SPE, ATM in 44.736 Mbit/s mapping

see Sec. 3, Page S-3 and Sec. 7, Page S-9

11 VC3, ATM in 44.736 Mbit/s mapping

see Sec. 7, Page S-9 and Sec. 9, Page S-16

ANT-20SE
Advanced Network Tester

Broadband Analyzer/Generator

BN 3060/90.51

Software Version 7.20

Specifications

Contents

Specifications Broadband Analyzer/Generator

Specifications Broadband Analyzer/Generator

1 Generator

1.1 Scrambling

The cell payload is scrambled as per ITU-T recommendation I.432 ($X^{43} + 1$).
The scrambler can be disabled.

1.2 Fill Cells

The fill cell type is selectable. IDLE or UNASSIGNED cells can be used.

1.3 Cell Header

UNI/NNI Modus	selectable[1]
GFC	selectable[2]
VPI, VCI	selectable[3]
CI (congestion indicator)	selectable[2]
CLP (cell loss priority)	selectable[2]
HEC	formed automatically

1 Set to UNI automatically for SVC.
2 Selectable for PVC. Set automatically for SVC (0 set).
3 Selectable for PVC. Set automatically for SVC.

1.4 General Functions

1.4.1 Error Insertion (Anomalies)

The following anomalies can be inserted in addition to the errors inserted in the physical layer. These anomalies are not dependent on the active measurement type, they are referred to the entire cell stream including fill cells.

Error type, anomaly	**Single**	**Rate[1]**	**Sensor threshold**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M=1 to 31 N = M+1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M =1 to 31 N = M +1 to M + 31

1 Mantissa = 1 (fixed), exponent = -2 to -6 (integer values)
2 Uncorrectable header error
3 Correctable header error

Table S-1 Settable anomalies

1.4.2 Alarm Generation (Defects)

The following defects can be generated in addition to the physical layer alarms. These defects can be generated independently of the active measurement type. They are referred to the entire cell stream.

Defect	**Test sensor functions**	**Single**
	On/Off	
LCD[1]	yes	yes

1 LCD (Loss of Cell Delineation) is generated if uncorrectable header errors are found in seven or more consecutive cells.

Table S-2 Settable defects

1.5 Functions for ATM Layer Quality of Service Measurements

1.5.1 General

Number of test channels 4
Source models . . . . . "Constant Bit Rate", "On-Off"

Traffic Shaper[1] . . . . . "Single Leaky Bucket", "Dual Leaky Bucket"

Maximum total bandwidth of all test channel . . . . . 366792 cells/s[2]

1 Can be disabled
2 In practice, the upper limit is given by the physical mapping

1.5.2 Error Insertion (Anomalies)

The following anomalies can be inserted selectively into each of the 4 test channels. All anomalies are inserted as a single event.

Uncorrectable header error . . . . . HUNC
Correctable header error . . . . . HCOR
Cell loss . . . . . Cell Loss
Cell error. . . . . Cell Error
Cell misinsertion . . . . . Cell Misins.
Severely errored cell block . . . . . SECB

1.5.3 Alarm Generation

The following defects can be generated selectively on each of the 4 test channels. All defects are generated as "on/off" functions.

F5 layer (VC) Alarm Indication Signal . . . . . VC-AIS
F4 layer (VP) Alarm Indication Signal . . . . . VP-AIS
F5 layer (VC) Remote Defect Indication. . . . . VC-RDI
F4 layer (VP) Remote Defect Indication . . . . . VP-RDI

1.5.4 Test Cell Format

Test cell format conforms with ITU-T recommendation O.191, issue of 9th January 1997.

Transmission timestamp resolution . . . . . 640 ns[1]

1 The lowest value bits of the timestamp are always set to 0

1.6 Source Models

1.6.1 Constant Bit Rate Model

A cell stream with nominally constant cell spacing is generated.

Parameters . . . . . peak cell rate and cell jitter”
Peak cell rate . . . . . 0 bis 366792 cells/s[1]
Peak cell rate units . . . . . cells/s, Mbit/s, kbit/s

Peak cell rate resolution . . . . . 1 cell/s

Maximum possible cell jitter[2] . . . . . depends on the peak cell rate and the mapping setting

Jitter profile . . . . . periodic ramp[3]
Jitter units . . . . . µs, ms
Jitter resolution . . . . . 1 µs

1 In practice, the upper limit is given by the physical mapping.
2 This is the source model jitter. The jitter in the actual data stream is the sum of the source model jitter, the multiplex jitter and the intrinsic jitter of the generator. The intrinsic jitter of the generator is largely determined by the mapping and is hence strongly dependent on the physical cell rate.
3 Cell arrival times are reduced over a certain time interval until the set jitter amplitude is reached. A gap then occurs in the cell stream to ensure that the correct mean cell rate is achieved.

1.6.2 “On-Off” Model

A burst-type cell stream with on/off character is generated.

Parameters . . . . . peak cell rate, mean cell rate, burst size and cell jitter

Peak cell rate . . . . . 0 to 366792 cells/s[1]
Peak cell rate units . . . . . cells/s, Mbit/s, kbit/s

Peak cell rate resolution . . . . . 1 cell/s

Mean cell rate . . . . . 0 to 366792 cells/s[1]
Mean cell rate units . . . . . cells/s, Mbit/s, kbit/s

1 In practice, the upper limit is given by the physical mapping.

Mean cell rate resolution . . . . . 1 cell/s

Maximum burst size . . . . . depends on the settings for mean cell rate and peak cell rate

Burst size units . . . . . µs, ms
Burst size resolution . . . . . 1 µs

Maximum possible cell jitter . . . . . depends on the peak cell rate and the mapping setting

Jitter profile . . . . . periodic ramp, standardized on burst size[1]
Jitter units . . . . . µs, ms
Jitter resolution . . . . . 1 µs

1 Cell arrival times are reduced within the burst so that the set jitter amplitude is achieved.

1.7 Traffic Shaper

1.7.1 Traffic Shaper for CBR, UBR and DBR Traffic Contracts

Algorithm . . . . . compatible with single leaky bucket
Parameters . . . . . peak cell rate and $CDVT_{PCR}$[1]
Peak cell rate range . . . . . 0 to 366792 cells/s
Peak cell rate units . . . . . cells/s, Mbit/s, kbit/s
$CDVT_{PCR}$ range . . . . . 0 to 16,383 ms
$CDVT_{PCR}$ units . . . . . µs, ms

1 “Cell Delay Variation Tolerance” referred to the peak cell rate.

1.7.2 Traffic Shaper for VBR and SBR Traffic Contracts

Algorithm . . . . . compatible with dual leaky bucket

Parameters . . . . . peak cell rate, sustainable cell rate, burst tolerance, $CDVT_{SCR}$ and $CDVT_{PCR}$

Peak cell rate range. . . . . 0 to 366792 cells/s
Peak cell rate units . . . . . cells/s, Mbit/s, kbit/s
Sustainable cell rate range . . . . . 0 bis 366792 Cells/s
Sustainable cell rate units . . . . . cells/s, Mbit/s, kbit/s
Burst tolerance range . . . . . 0 to 999.99 ms
Burst tolerance units . . . . . µs, ms
$CDVT_{PCR}$ range. . . . . 0 to 16.383 ms
$CDVT_{PCR}$ units . . . . . µs, ms
$CDVT_{SCR}$ range. . . . . 0 to 16.383 ms
$CDVT_{SCR}$ units . . . . . µs, ms

1 “Cell Delay Variation Tolerance” referred to the sustainable cell rate.

2 Receiver

2.1 Descrambling

Descrambling as per ITU-T recommendation I.432 ($X^{43} + 1$).
The Descrambler can be disabled.

2.2 General Functions

2.2.1 Error Measurements (Anomalies)

The following anomalies are evaluated and displayed in addition to the errors on the physical layer. These errors are detected for the entire cell stream.

Anomaly	Count	Explanation
HEC Error Count correctable	yes	Correctable cell header errors
HEC Error Count uncorrectable	yes	Uncorrectable cell header errors

Table S-3 Display of possible anomalies

2.2.2 Alarm Detection (Defects)

Defect	LED	Defect Seconds Count [1]	Explanation
Loss of Cell Delineation	Software LEDs for history and actual status	yes	Loss of cell synchronization
Physical Layer Defect	Software LEDs for history and actual status	yes	Sum alarm for physical layer errors. Activated when an analyzable cell stream is no longer present.

1 A “Defect Second” is counted if the event occurs at least once within a one-second interval.

Table S-4 Display of possible defects

2.2.3 Receiver Bandwidth

Display of momentary bandwidth of all virtual channels in the physical connection in Mbit/s and as a percentage. The percentage is referred to the theoretical maximum bandwidth for the selected mapping setting.

2.3 ATM Layer Quality of Service Measurements

2.3.1 General Features

Number of measurement channels 4
Maximum measurement channel bandwidth . . . . . 366792 cells/s[1]
Maximum total bandwidth of all test channels . . . . . 366792 cells/s[1]

1 In practice, the upper limit is given by the physical mapping.

2.3.2 Error Related Parameters

Measurement algorithm conforms to ITU-T recommendation O.191, issue of 9th January 1997.

The following parameters are measured as count and rate (or ratio) values.

- Cell loss
- Cell error
- Cell misinsertion
- Severely errored cell block, SECB

The “Analyzed Cell Count” is also indicated.

2.3.3 Delay Related Parameters

Delay measurements are only possible if the generator cell stream is looped back to the receiver, i.e. when the instrument receives its own cell stream again.

Minimum cell transfer delay . . . . . min. CTD
Maximum cell transfer delay . . . . . max. CTD
Mean cell transfer delay . . . . . mean CTD
2-point cell delay variation . . . . . 2-pt. CDV_{PP}

2.3.4 Alarm Detection (Defects)

Defect	LED	Defect Seconds Count[1]	Explanation
VC-AIS	Software LEDs for history and actual status	yes	F5 layer (VC) Alarm Indication Signal
VP-AIS	Software LEDs for history and actual status	yes	F4 layer (VP) Alarm Indication Signal
VC-RDI	Software LEDs for history and actual status	yes	F5 layer (VC) Remote Defect Indication Signal
VP-RDI	Software LEDs for history and actual status	yes	F4 layer (VP) Remote Defect Indication Signal

1 A “Defect Second” is counted if the alarm state occurs at least once within a one-second interval.

Table S-5 Display of possible defects

2.3.5 Other Parameters

The following parameters are indicated as a count of defect seconds[1].

“Loss of Performance Assesment Capability” . . . . . LPAC
“Not Connected Seconds” . . . . . NCS[2]

1 A “Defect Second” is counted if the event occurs at least once within a one-second interval.
2 Only occurs for SVCs.

The “Loss of Performance Assessment Capability” state is detected if it is no longer possible to measure the error and delay-related parameters due to major disruption of the cell stream.

The “Not Connected” applies when no virtual connection is switched.

2.4 Channel Explorer

2.4.1 Activity Scan

Automatic detection of active virtual channels. Channels are distinguished by VCI and VPI. UNI and NNI interface types can be selected.

Maximum number of channels detectable simultaneously 1000
Sort function . . . . . .unsorted[1]
sorted by VPI/VCI
sorted by bandwidth

The following parameters are measured for each detected channel:

Average bandwidth . . . . . .AvBW[2] [Mbps]
Current bandwidth . . . . . .CuBW[3] [Mbps]
Proportion of cells with Congestion Indicator set. . . . . CI-BW[4] [%]
Proportion of cells with Cell Loss Priority Bit set . . . . . .CLP1-BW[5] [%]

An “aging” function can be activated optionally. This function deletes all channels that have not shown any activity for at least 30 seconds from the list of active channels.

2.4.2 Trouble Scan

Automatic detection of AIS and RDI alarms. Simultaneous display of F4 layer alarms (virtual path) and F5 layer alarms (virtual channel). UNI and NNI interface types can be selected.

Maximum number of simultaneously
detectable OAM flows (F4 or F5 layer) 1000
Sort function . . . . . .unsorted[1]
sorted by VPI/VCI

1 Unsorted means that the channels are displayed in chronological order of detection.
2 The average bandwidth is the average over the time that has elapsed since the channel was detected.
3 The current bandwidth is the average for the last 10-second interval.
4 Referred to the average bandwidth.
5 Referred to the average bandwidth.

2.4.3 AAL analysis

Automatic detection of AAL type for all channels detected during an Activity Scan.

Maximum number of simultaneously analyzed channels 1000
Different AAL types. . . . . AAL1, AAL3/4, AAL5, undetected[1] unchecked[2]

It is also possible to display the AAL type distribution graphically (pie chart). The proportion of each AAL type is given as a percentage.

1 Undetected means that the AAL type cannot be determined (e.g. an unknown AAL type or a severely errored cell stream).
2 Unchecked means that the AAL type for the channel in question was not tested (e.g. because analysis was terminated earlier by the user).

3 Signaling

The instrument simulates the signaling functions of a terminal on the user-network interface (UNI). Up to 4 connections can be switched simultaneously.

“Channel associated signaling” can be selected as an option. Subaddresses can also be optionally used.

Signaling standards . . . . . ITU-T recommendation Q. 2931,
ITU-T recommendation Q. 2961,
ATM Forum recommendation UNI 3.0,
ATM Forum recommendation UNI 3.1

Modes . . . . . “Calling”, “Called”, “Self Call”

Adress formats . . . . . .Native E. 164,
NSAP ICD,
NSAP DCC,
NSAP E.164,
NSAP E.191

Signaling channel (VPI/VCI) . . . . . .user definable

1 Only possible if ITU-T recommendation Q. 2931 protocol is selected.

3.1 Traffic Contracts

Traffic types . . . . . “CBR”, “DBR”, “UBR”, “VBR-RT”, “VBR-nRT”, “SBR”[1]
Quality of Service classes 1, 2, 3, 4
Connection type . . . . . point-to-point
Direction . . . . . bi-directional, symmetrical
bi-directional asymmetric

1 CBR: “Constant Bit Rate”, DBR: “Deterministic Bit Rate”, UBR: “Unspecified Bit Rate”, VBR-RT: “Variable Bit Rate - Real Time”, VBR-nRT: “Variable Bit Rate - non Real Time”, SBR: “Statistical Bit Rate”.
CBR, UBR, VBR-RT and VBR-nRT are ATM Forum traffic types. SBR and DBR are ITU “Bearer Capabilities.

3.2 Signaling Analysis

Detection and display of the connection status of up to 4 connections simultaneously.

Displayed states . . . . . disconnected, connecting, connected

Measurement of the connection setup time (“Channel Setup Time”).

ANT-20SE
Advanced Network Tester

Concatenated Mappings
OC-12c/STM-4c
OC-48c/STM-16c

BN 3060/90.55 to 3060/90.58

Software Version 7.20

Specifications

8

WAVETEK
WANDEL
GOLTERMANN
Communications Test Solutions

Contents

Specifications OC-12c/STM-4c

Specifications OC-48c/STM-16c

Specifications OC-12c/STM-4c

These specifications apply to the following options:

OC-12c/STM-4c mapping

OC-12c/STM-4c ERROR TEST (BULK). . . . . .BN 3035/90.90
OC-12c/STM-4c ATM TESTING. . . . . .BN 3035/90.91
OC-12v/STM-4v VIRTUAL CONCATENATION . . . . . .BN 3035/90.92

The numbers in square brackets [...] against the measurement connections correspond to the numbers printed on the instrument.

Calibrated specifications are marked ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [18], optical

Connector . . . . . 2.5 mm (PC)

"Fiber to fiber" test adapter for connecting various
2.5 mm plug connectors . . . . . see list of accessories

Output level *** . . . . . 0 dBm +2/-3 dBm

Reduction in output level
for dual wavelength version . . . . . < 0.5 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . 1310 nm (1280 to 1330 nm),
1550 nm (1480 to 1580 nm)

Laser safety class as per EN 60825-1:1994 1

The generator meets the requirements of ITU-T G.957 classes L1.1, L1.2, L1.3, L4.1, L4.2, L4.3.
Classes S1.1, S1.2 as well as S4.1 and S4.2 can be achieved by inserting an optical attenuator or the Optical Power Splitter BN 3035/90.49.

LASER ON status display

LED is on when the laser source is active.

1.2 Clock generation and bit rates

1.2.1 Clock generation

See “Specifications” for the mainframe instrument.

1.2.2 Bit rate

OC-12c/STM-4c. . . . . 622.08 Mbit/s

1.3 SDH and SONET Tx signals

- OC-12c signal generated as per Bellcore GR-253 Standard.
- STM-4c signal generated as per ITU-T Recommendation G.707.

1.3.1 OC-12c/STM-4c Tx signal

OC-12c/STM-4c signal formation:

- Signal generated internally, payload contains bulk signal or ATM cells.
- Complete signal taken from receiver.

1.3.2 Scrambling

Scrambling is as per ITU-T Recommendation G.707.
Scrambling can be activated or deactivated.

1.3.3 Overhead generation

1.3.3.1 Section overhead (SOH), Transport overhead (TOH)

Standard OC-12c/STM-4c overhead (hex)

	S O H, TOH																																			
1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	J0 C1 01	Z0 C1 AA	Z0 C1 AA	Z0 C1 AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA
2	B1 XX	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	E1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	F1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
3	D1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D3 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
4a	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4b	H1 68	H1 68	H1 68	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	H2 00	H2 00	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4c	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4d	H1 60	H1 60	H1 60	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	H2 00	H2 00	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	K2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
6	D4 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D5 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D6 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
7	D7 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D8 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D9 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
8	D10 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D11 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D12 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	E2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00

Table S-1 SOH, TOH contents; OC-12c/STM-4c

XX: Inserted through parity formation (B1, B2)

Line 4a: SDH pointers (VC-4-4c)

Line 4b: SDH pointers (VC-4-4v)

Line 4c: SONET pointers (STS-12c)

Line 4d: SONET pointers (STS-12v)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place.

Contents of SOH bytes

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: E1, F1, E2 (single byte)
- Dynamic bytes filled with PRBS11: D1 to D3, D4 to D12 (byte group)
- Dynamic bytes via DCC/ECC interface, socket [21] (V.11): E1, F1, E2 (single byte)
- Dynamic bytes via DCC/ECC interface, socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

1.3.4 VC-4c path overhead (POH), high-order

1.3.4.1 Contiguous concatenation (VC-4-4c)

Standard overhead

POH byte	**POH #1**	**POH #2 to #4** Fixed stuffing (3 columns)
J1 (ASCII)	“WG HP-TRACE”	“00”
B3 (hex)	Inserted by parity formation	“00”
C2 (hex)	“13” for ATM mapping “FE” for BULK (STM-4) “01” for BULK (OC-12)	“00”
G1 (hex)	“00”	“00”
F2 (hex)	“00”	“00”
H4 (hex)	“FF”	“00”
F3 (hex)	“00”	“00”
K3 (hex)	“00”	“00”
N1 (hex)	“00”	“00”

Table S-2 POH contents

Contents of VC-4-4c POH bytes

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

1.3.4.2 Virtual concatenation (VC-4-4v)

Only with option BN 3035/90.92

Standard overhead

POH byte	POH #1	POH #2 to #4
J1 (ASCII)	“WG HP-TRACE”	“00”
B3 (hex)	Inserted through parity formation	
C2 (hex)	“13” for ATM mapping “FE” for BULK signal (STM-4) “01” for BULK (OC-12)	“13” for ATM mapping “FE” for BULK signal (STM-4) “01” for BULK (OC-12)
G1 (hex)	“00”	“00”
F2 (hex)	“00”	“00”
H4 (hex)	“FF”	
F3 (hex)	“00”	“00”
K3 (hex)	“00”	“00”
N1 (hex)	“00”	“00”

Table S-3 POH contents

Contents of VC-4-4v POH byte #1

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

Contents of VC-4-4v POH bytes #2 to #4

- Static bytes: All except B3, H4
- All bytes as POH #1, except B3

1.3.5 Generation of pointer actions

1.3.5.1 Contiguous concatenation

Stimulation

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

1.3.5.2 Virtual concatenation

Only with option BN 3035/90.92

Stimulation of pointer #1

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

Stimulation of pointers #2 to #4

Pointer actions in pointer #1 affect pointers #2 to #4 at the same time.

A delta value (deviation) from pointer #1 can be generated for pointers #2 to #4.

Maximum delta of pointers #2 to #4 to pointer #1 . . . . . ± 40 pointers
or time . . . . . ± 6.17 µs

Increment / decrement. . . . . 1 pointer
or time . . . . . 154 ns

Setting a new delta value is through n x increment or n x decrement.

For n > 1, the spacing between two consecutive increment / decrement actions is 32 frames (4 ms).

The delta for pointers #2 to #4 is retained for pointer actions in pointer #1.

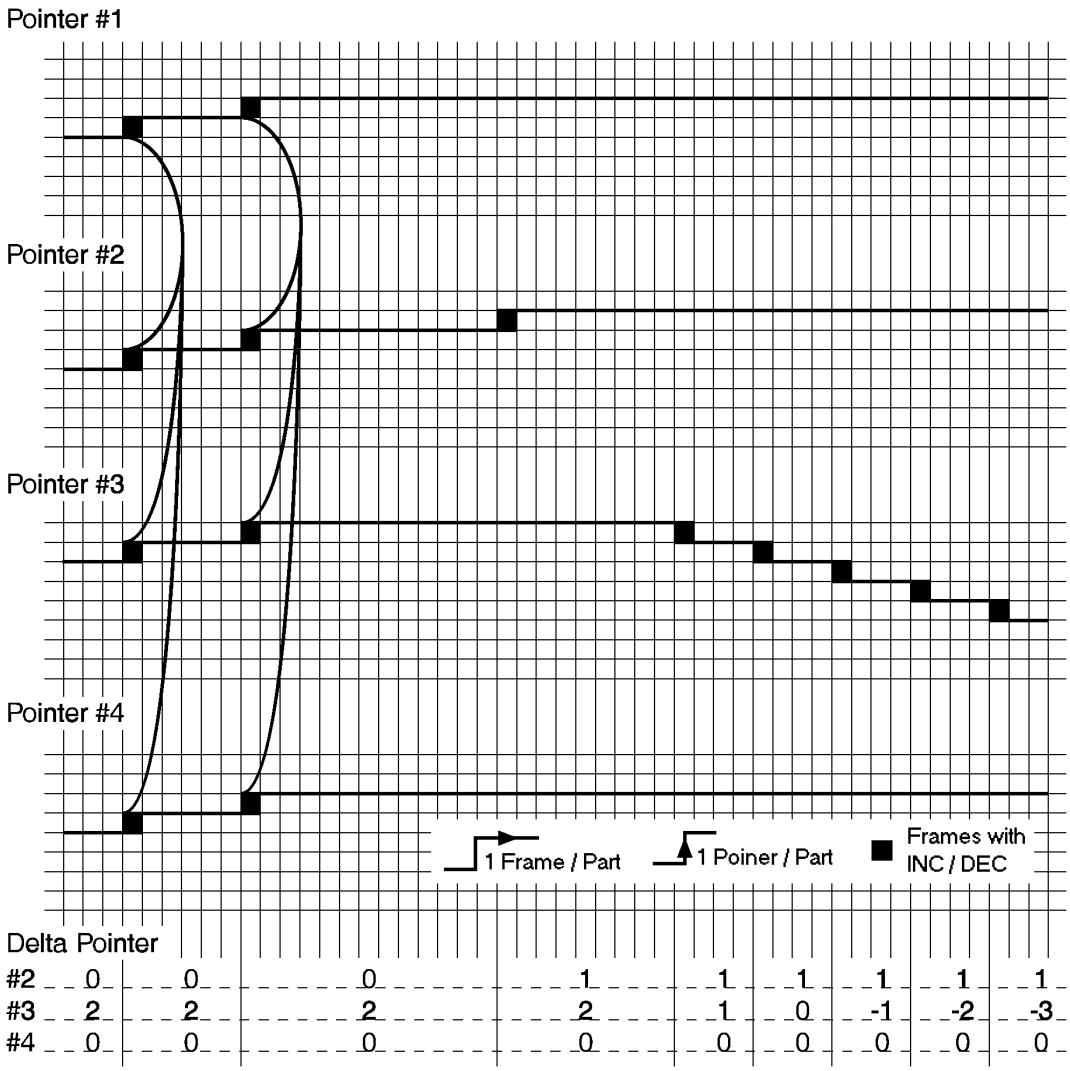


Fig. S-1 Pointer actions

1.3.6 OC-12c/STM-4c anomaly insertion

Anomaly insertion . . . . . B1, B2, B3 parity errors
REI-L/MS-REI, REI-P/HP-REI

Trigger modes . . . . . .Single
or Rate

A bit error rate is inserted when Rate is selected.

Anomaly	Single	Rate[1]
B1 (OC-12c, STM-4c)	yes	2E-4 to 1E-10
B2 (OC-12c, STM-4c)	yes	2E-3 to 1E-10
REI-L (OC-12c) MS-REI (STM-4c)	yes	2E-3 to 1E-10
B3[2] (STS-12c SPE/VC-4-4c)	yes	2E-4 to 1E-10
REI-P (STS-12c SPE)[3] HP-REI (VC-4-4c)	yes	2E-4 to 1E-10

1 Mantissa: 1 to 9, Exponent: -1 to -10 (integer values)
2 Virtual concatenation: Single: POH #1; Rate: All four POHs
3 Virtual concatenation: Insertion in POH #1

Table S-4 Anomalies (OC-12c, STM-4c) and trigger modes

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.3.7 OC-12c/STM-4c defect generation

Defect	Sensor function test	Sensor threshold test	
-	On/Off	M in N	|---t1---| |------t2------|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-622	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-L (OC-12c) RS-TIM (STM-4c)	yes	-	-
AIS-L (OC-12c) MS-AIS (STM-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-L (OC-12c) MS-RDI (STM-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP_P (STS-12c SPE) AU-LOP (VC-4-4c)[1]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-P (STS-12c SPE) AU-AIS (VC-4-4c)[1]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-P (STS-12c SPE) HP-UNEQ (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-P (STS-12c SPE) HP-PLM (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-P (STS-12c SPE) HP-RDI (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-P (STS-12c SPE) HP-TIM (VC-4-4c)	yes	-	-

1 Insertion in all four pointers (AU-4)
2 X = 1 to 4; insertion in selected pointer (AU-4) only

Table S-5 Defects

Insertion of **defects** and **anomalies** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4 Payload generation

1.4.1 BULK signal generator

Only with option BN 3035/90.90

1.4.1.1 Payload

Bit rate . . . . . 599.04 Mbit/s

Structure . . . . . unframed

1.4.1.2 Bit patterns

Digital word . . . . . .16 bits

Pseudo-random bit sequences . . . . . PRBS 15, PRBS 15 inverted, PRBS 20, PRBS 23, PRBS 23 inverted, PRBS 31, PRBS 31 inverted

1.4.1.3 Anomaly insertion

The following anomaly can be inserted in addition to those described in Sec. 1.3.6, Page S-7:

Anomaly	**Single**	**Rate**[1]
TSE	yes	1E-2 to 1E-9
1 Mantissa: 1, Exponent -2 to -9 (integer values)		

Table S-6 Additional anomaly (OC-12c, STM-4c)

Anomaly insertion . . . . . .Test sequence error (TSE)

Trigger modes . . . . . Single or Rate

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4.2 ATM generator section

Only with options BN 3035/90.70 (ATM Module) and BN 3035/90.91

1.4.2.1 Scrambling

Scrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$). The function can be disabled.

1.4.2.2 Anomaly insertion

The following anomalies can be inserted in addition to those described in Sec. 1.3.6, Page S-7.

Anomaly	**Single**	**Rate[1]**	**Sensor threshold**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
AAL-1 cell loss	yes	1E-3 to 1E-6	-
AAL-1 CRC	yes	1E-3 to 1E-6	-
AAL-1 PE	yes	1E-3 to 1E-6	-

1 Mantissa: 1 only, Exponent: -1 to -6 (integer values)
2 Uncorrectable header error
3 Correctable header error

Table S-7 Additional anomalies

The AAL-1 cell loss, AAL-1 CRC and AAL-1 PE anomalies refer to the measurement channel. Test sequence errors (TSE) are inserted in the ATM payload or in the AAL-1 payload of the test channel.

Correctable and uncorrectable header errors are inserted in the overall cell stream.

1.4.2.3 Defect generation

The following defects can be generated in addition to those described in Sec. 1.3.7, Page S-9.

Defect	Sensor function test	Single
	On / Off	
LCD[1]	yes	yes
VP-AIS	yes	yes
VP-RDI	yes	yes
VC-AIS[2]	yes	yes
VC-RDI[3]	yes	yes
Vx-AIS[4]	yes	yes
Vx-RDI[4]	yes	yes

1 LCD (Loss of Cell Delineation) is generated by uncorrectable header errors in ≥ 7 consecutive cells.
2 AIS: Alarm Indication Signal; VC: Virtual Channel; VP: Virtual Path
3 RDI: Remote Defect Indication
4 For Vx-AIS and Vx-RDI defects are inserted in the VP and VC in parallel.

Table S-8 Additional defects

1.4.2.4 Test channel

Cells

Header

UNI/NNI, VCI, VPI, PT and CLP . . . . . settable
HEC . . . . . formed automatically

Payload

Pseudo-random bit sequences . . . . . PRBS 11, PRBS 15, PRBS 20, PRBS 23
Digital word . . . . . 16 bits

Load profiles

Constant, Equidistant, Burst

Constant load profile

Load setting . . . . . 14.976 to 149760 kbit/s

Resolution dependent on load range setting
14.976 to 1482.624 kbit/s . . . . . 14.976 kbit/s
149.76 to 14826.24 kbit/s . . . . . 149.76 kbit/s
1497.6 to 149760 kbit/s. . . . . 1497.6 kbit/s

Equidistant load profile setting range

Cell spacing . . . . . 4 to 40000 cell periods
Maximum cell spacing deviation. . . . . ± 1 cell period

Resolution depending on cell spacing range setting
4 to 400 . . . . . 4 cell periods
40 to 4000 . . . . . 40 cell periods
400 to 40000 . . . . . 400 cell periods

Burst load profile setting range

Maximum burst length . . . . . 4092 cells / 2.79 ms
Burst load . . . . . 1497.6 to 149760 kbit/s
Resolution . . . . . depends on burst length

Maximum burst period . . . . . 131068 cells / 89 ms

Load units . . . . . Mbit/s, Cells/s, %
Time units . . . . . cell period

1.4.2.5 Background load

A channel is generated as background load. The test channel has priority.

Header . . . . . freely selectable

Payload . . . . . byte by byte constant, bytes freely selectable

Load profile. . . . . CBR, Fill

Constant bit rate (CBR) . . . . . 449280 kbit/s

Filling up to . . . . . 149760 / 599040 kbit/s

1.4.2.6 Fill cells

The cell stream is filled with IDLE or UNASSIGNED cells. Either can be selected.

1.4.2.7 AAL-1 segmentation

PDU signals with system bandwidths of 1,5 Mbit/s, 2 Mbit/s, etc. can be transmitted in the AAL-1 in the test channel.

Possible payload patterns for 2 Mbit/s . . . . . PRBS unframed,
PRBS in PCM30,
PRBS in PCM30CRC

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [17], optical

Connector . . . . . 2.5 mm (PC)

Fiber to fiber" test adapter for connecting various
2.5 mm plug connectors . . . . . see list of accessories

Input sensitivity
OC-12c / STM-4c *** . . . . . -8 to -28 dBm

Max. permissible input level . . . . . +2 dBm

Wavelength . . . . . 1100 to 1580 nm

The receiver meets the requirements of ITU-T G.957 Classes S1.1, S1.2, S4.1, S4.2 and S4.3.

Tolerance to jitter

measured using scrambled SDH or SONET signals:

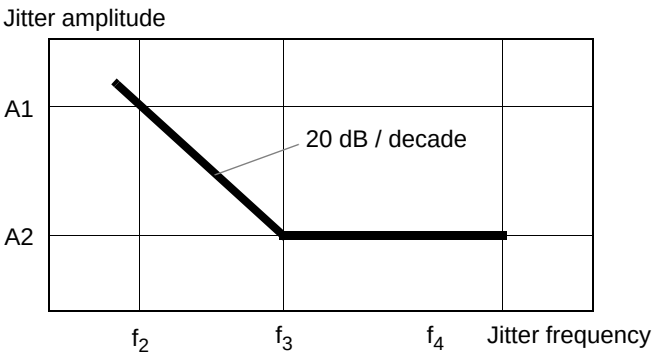


Fig. S-2 Jitter amplitude versus jitter frequency

Bit rate Mbit/s	A1 Ulpp	f_2 kHz	A2 Ulpp	f_3 kHz	f_4 kHz
51.840	1.5	2	0.15	20	500
155.520	1.5	6.5	0.15	65	1300
622.080	1.5	25	0.15	250	5000

Table S-9 ANT-20SE tolerance to jitter at system bit rates

2.1.2 Signal input [16], electrical

Connector . . . . . unbalanced (coaxial)

Socket type . . . . . SMA

Input impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Input voltage range . . . . . 200 mVpp to 1Vpp

Bit rate . . . . . 155.52 Mbit/s; 622.08 Mbit/s

Tolerance to jitter

See Tab. S-9, Page S-14

LOS (Loss of Signal) status display

The LED is on if the signal input is active but no signal is present.

2.1.3 Clock recovery

See “Specifications” for the mainframe instrument.

2.2 SDH and SONET Rx signals

- Evaluation of an OC-12c signal as per Bellcore GR-253 standard.
- Evaluation of a STM-4c signal as per ITU-T Recommendation G.707.

2.2.1 OC-12c/STM-4c Rx signal

Evaluation of OC-12c/STM-4c signals:

- Analysis of the transport overhead (TOH) / section overhead (SOH), path overhead (POH) and payload (BULK), either directly or in conjunction with the ATM Module (option BN 3035/90.70).
- Analysis of the transport overhead (TOH) / section overhead (SOH) and loop through of the OC-12c/STM-4c signal to the generator (D&C)

2.2.2 Descrambling

Descrambling is according to ITU-T Recommendation G.707.
Descrambling can be activated / deactivated.

Tip: Make sure that there are no long sequences of zeros or ones in the data stream of unscrambled input signals.

2.3 Measurement modes

2.3.1 Evaluation of section overhead (SOH), transport overhead (TOH)

Display

Complete SOH, TOH: (four channel-associated part SOH) . . . . . hexadecimal

Trace Identifier J0 (STS-12c SPE/VC-4-4c) . . . . . ASCII, plain text

Overhead Capture . . . . . see Section 1 “Extended Overhead Analysis” option BN 3035/90.15

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . E1, F1, E2 (single byte)

using pseudo-random bit sequence PRBS11 . . . . . .D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) . . . . . E1, F1, E2 (single byte)

DCC/ECC interface, socket [21] (V.11) . . . . . D1 to D3, D4 to D12, K1 to K2 (byte group)

2.3.2 Evaluation of path overhead (POH)

2.3.2.1 Contiguous concatenation

Display

Complete POH . . . . . hexadecimal

Trace Identifier J1 . . . . . ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) F2, N1

2.3.2.2 Virtual concatenation

Display

Complete POH: (four channel-associated part POH) . . . . . hexadecimal

Trace Identifier J1 (POH #1 only) . . . . . .ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 (POH #1 only) F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) (POH #1 only) F2, N1

2.3.3 Measurement of AU pointer actions

Evaluation

The AU pointer (pointer #1 in virtual concatenation) is indicated as an absolute value. The direction and number of pointer movements are detected.

NDF (new data flag) is detected and counted (pointer #1 in virtual concatenation).

The differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 are determined and recorded (virtual concatenation).

Maximum delta . . . . . ± 40 pointers / ± 6.17 µs

Display

- Number of AU pointer operations (pointer #1 in virtual concatenation):
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address (pointer #1 in virtual concatenation)
- Number of NDF events (pointer #1 in virtual concatenation)
- Corresponding clock deviation (pointer #1 in virtual concatenation)
- Differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 (virtual concatenation)
- AU-NDF and NDF-P can be indicated by the LED display on the front panel (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP” and it indicates “NDF-P” in addition to “LOP-P”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF (pointer #1 in virtual concatenation) are displayed as histograms with a selectable time resolution of seconds, minutes, hours or days.

The differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 are indicated as number of pointers and as time (µs) (virtual concatenation).

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements, NDF and delta pointer (virtual concatenation) are printed out as a table with a resolution of 1 second.

2.3.4 Anomaly measurements

Evaluation

All anomalies are counted and recorded simultaneously.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

Anomalies are indicated by LEDs:

CURRENT LED (red) is on while the anomaly is present.

HISTORY LED (yellow)is on if the anomaly occurred at least once or is still present during the current measurement interval.

Anomaly	LED
OOF-622	LOF/OOF
B1 (OC-12c/STM-4c)	B1/B2
B2 (OC-12c/STM-4c)	B1/B2
REI-L (OC-12c) MS-REI (STM-4c)	-
B3 (STS-12c SPE/VC-4-4c)	B3
REI-P (OC-12c) HP-REI (STM-4c)	-

Table S-10 LED display of anomalies

Evaluation and display of B2 errors refers to the concatenated data stream (BIP-96).

Evaluation and display of B3 errors:

- Contiguous concatenation: BIP-8
- Virtual concatenation: BIP-32

2.3.5 Defect detection

Evaluation

All defects that are present are evaluated and recorded simultaneously as far as possible. Recording takes place only within a started measurement interval.

Time resolution of defects . . . . . .100 ms

Display

Defects are indicated by LEDs:

CURRENT LED (red) is on while the defect is present.

HISTORY LED (yellow)is on if the defect occurred at least once or is still present during the current measurement interval.

Defect	LED
LOS (optical)	LOS
LOF-622	LOF/OOF
TIM-L (OC-12c) RS-TIM (STM-4c)	-
AIS-L (OC-12c) MS-AIS (STM-4c)	MS-AIS/AIS-L
RDI-L (OC-12c) MS-RDI (STM-4c)	MS-RDI/RDI-L
LOP-P (STS-12c SPE) AU-LOP (VC-4-4c)	AU-LOP/LOP-P
LOP-Cx[1]	AU-LOP/LOP-P
AIS-P (STS-12c SPE) AU-AIS (VC-4-4c)	AU-AIS/AIS-P
AIS-Cx[2]	AU-AIS/AIS-P AU-LOP/LOP-P
DPOVC[3]	AU-LOP/LOP-P
UNEQ-P (STS-12c SPE) HP-UNEQ (VC-4-4c)[4]	HP-UNEQ/UNEQ-P
PLM-P (STS-12c SPE) HP-PLM (VC-4-4c)	HP-PLM/PLM-P
RDI-P (STS-12c SPE) HP-RDI (VC-4-4c)	HP-RDI/RDI-P
TIM-P (STS-12c SPE) HP-TIM (VC-4-4c)	-

1 AU-LOP is indicated if LOP is detected in at least one AU-4 pointer.
2 AU-AIS is indicated if AIS is detected in all four AU-4 pointers.
If AU-AIS is detected in one, two or three AU-4 pointers, AU-LOP-LOP-P is indicated.
3 Virtual concatenation: DPOVC (**D**elta **P**ointer **O**verflow **V**irtual **C**oncatenation; Delta >± 40)
This defect is indicated if the maximum delta of one of the pointers #2 to #4 relative to pointer #1 is exceeded.
4 Virtual concatenation: HP-UNEQ/UNEQ-P is indicated if HP-UNEQ/UNEQ-P is detected in at least one of the four VC-4 containers.

Table S-11 LED display of defects

2.4 Payload

2.4.1 BULK signal receiver

Only with option BN 3035/90.90

2.4.1.1 Bit pattern payloads

See Sec. 1.4.1.1, Page S-10 and Sec. 1.4.1.2, Page S-10

2.4.1.2 Anomaly measurements

The following anomaly can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-18:

Anomaly	LED
TSE	TSE

Table S-12 LED display of additional anomaly

2.4.1.3 Defect detection

The following defect can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-19:

Defect	LED
LSS	LSS

Table S-13 LED display of additional defect

2.4.2 ATM receiver section

Only with options BN 3035/90.70 and BN 3035/90.91

2.4.2.1 Descrambling

Descrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$).
The function can be disabled.

2.4.3 Measurement modes

2.4.3.1 Anomaly measurements

The following anomalies can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-18.

Anomaly	LED	Explanation	
HCOR	-	Correctable Header Error	
HUNC	-	Uncorrectable Header Error	
CER	-	Cell Error Ratio	for measurements using test cells
CLR	-	Cell Loss Ratio	
CMR	-	Cell Misinsertion Rate	
AAL-1-CRC	-	AAL1 CRC Error	for AAL-1 measurements
AAL-1-PE	-	AAL1 Parity Error	
AAL-1-CLR	-	AAL1 Cell Loss Ratio	
AAL-1-CMR	-	AAL1 Cell Misinsertion Rate	

Table S-14 Indication and evaluation of anomalies

The anomalies HUNC and HCOR apply to the complete cell stream. All other anomalies apply to the measurement channel only.

2.4.3.2 Defect detection

The following defects can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-19.

Defect	LED	Explanation	
LCD	LOF / LCD	Loss of Frame / Loss of Cell Delineation	
OCR	LOF / LCD	Overflow Cell Rate[1]	
OCLR	-	Cell Loss Overflow[2]	for measurements using test cells
OCMR	-	Cell Misinserted Overflow[3]	
VC-AIS	-	Virtual Channel Alarm Indication Signal	
VC-RDI	-	Virtual Channel Remote Defect Indication	
VP-AIS	-	Virtual Path Alarm Indication Signal	
VP-RDI	-	Virtual Path Remote Defect Indication	
AAL-1-OOS	-	AAL1 Out of Sync	

1 Test channel: Maximum cell rate (CBR) = 149760 kbit/s;
Max. consecutive cells at 599040 kbit/s = 400
2 More than 255 cell losses in 100 ms or relative to the last test cell
3 More than 255 misinserted cells in 100 ms or relative to the last test cell

Table S-15 LED display of additional defects

2.4.3.3 ATM performance measurements

Error-related performance parameters

The measurements are made using test cells.

Results

Lost Cell Count, Cell Loss Ratio . . . . . CLR
Misinserted Cell Count, Cell Misinserted Rate . . . . . CMR
Error Cell Count, Cell Error Ratio . . . . . CER

Cell transfer delay

The measurement is made using test cells.

Display . . . . . rate distribution
Resolution . . . . . 160 ns to 0.355 s
Measurement range . . . . . 20 µs to 42.9 s
Measurement range offset . . . . . 0 to 0.167 s
Units . . . . . µs

Cells with transfer delays outside the measurement range are counted as class 0 (underflow) or class 127 (overflow).

Cell delay variation

The measurement is made using test cells.

Display . . . . . rate distribution,
minimum delay,
maximum delay,
average delay,
peak-to-peak-CDV

The results are only valid if no cell delays outside the measurement range are detected.

2.4.4 User channel analysis and load measurement

Cell filters (VCI, VPI, CLP) for extracting the test channel.

The VCI and CLP filters can be disabled

Mean cell rate

The measurement is made over all connections in parallel and in the test channel simultaneously.

Measurement interval . . . . . 1 s
Resolution 0.01%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Peak cell rate

The measurement is made in the test channel.

Measurement interval . . . . . .1 s
Resolution 0.1%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . .linear, logarithmic

Channel loading histogram

The channel loading histogram indicates the distribution of 100 ms measurement intervals according to measured load.

Measurement interval . . . . . 100 ms
Number of classes 101
Class “0” contains the number of 100 ms intervals in which a load of 0% was measured.
Class width 1%
Load display . . . . . Mbit/s, Cells/s, %

User channel cell distribution

Display of cells in the user channel classified as user cells, OAM cells and user cells with CLP indicator.

Measurement interval . . . . . .1 s
Display . . . . . cell count

Test channel

Maximum cell rate (CBR) . . . . . 149760 kbit/s

Max. consecutive cells at 599040 kbit/s . . . . . .400 cells

Test cell format

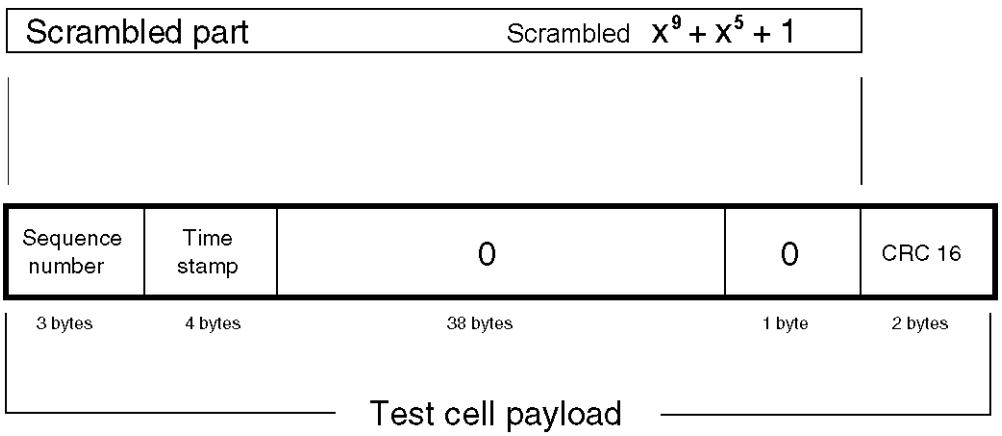


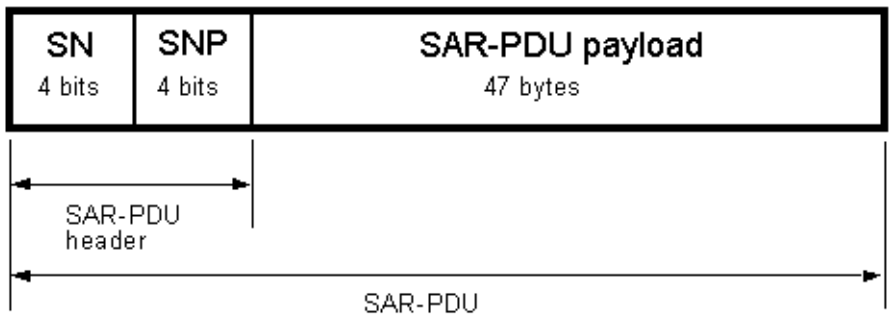
Fig. S-3 Test cell format to ITU-T O.191 (Draft 4/95)

2.4.4.1 AAL-1 reassembly

AAL-1 structured cells are reassembled from the SAR-PDU. The format is shown in the figure below. The TSE measurement is performed using framed or unframed pseudo-random bit sequences (PRBS) mapped into the SAR-PDU payload.

The following payload patterns are available for measurements:

- PRBS unframed
- PRBS in PCM-30 frame
- PRBS in PCM-30 frame (with CRC)



SN: Sequence Number
SNP: Sequence Number Protection
PDU: Protocol Data Unit
SAR: Segmentation and Reassembly

Fig. S-4 SAR-PDU format for AAL-1 cells

Notes:

Specifications OC-48c/STM-16c

These specifications apply to the following options:

OC-48c/STM-16c mappings

OC-12c/STM-4c ERROR TEST (BULK). . . . . .BN 3035/90.90
OC-12c/STM-4c ATM TESTING. . . . . .BN 3035/90.91
OC-48c/STM-16c ERROR TEST (BULK). . . . . .BN 3035/90.93

One of the following options is also required:

STM-16/OC-48 (1550 nm) . . . . . .BN 3035/91.53
STM-16/OC-48 (1310 nm) . . . . . .BN 3035/91.54
STM-16/OC-48 (1550 nm/1310 nm). . . . . .BN 3035/91.59

The numbers in square brackets [...] correspond to the numbers printed on the instrument.

Calibrated specifications are indicated by ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [47], optical

Connector . . . . . 2.5 mm (PC)

“Fiber-to-fiber” adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Output level *** . . . . . 0 dBm +0/-2 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . 1310 nm (1285 to 1340 nm)
1550 nm (1520 to 1600 nm)

Laser class to EN 60825-1:1994
Normal operation 1
Fault condition 3A

The generator fulfils the requirements of ITU-T G.957, classes S16.2, L16.2, L16.3 or S16.1, L16.1.

LASER ON status display

LED is on when the laser source is active.

1.1.2 Signal output [46], electrical

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Signal output impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Output voltage . . . . . ≥ 500 mVpp

Bit rate . . . . . 2488.32 Mbit/s

1.2 Clock generator and bit rates

1.2.1 Clock generation internal

See “Specifications” for the mainframe instrument.

Permissible clock offset . . . . . ± 50 ppm

1.2.2 Clock generation external [45]

For feeding in a jitter-modulated clock signal that must be derived from the base module clock.

Clock frequency . . . . . 2488.32 Mbit/s

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Clock input impedance . . . . . 50 Ω

Input voltage range . . . . . .300 mVpp to 1 Vpp

1.2.3 Bit rate

STM-16, OC-48 . . . . . 2488.32 Mbit/s

1.3 SDH and SONET TX signals

- Generates an OC-48c signal conforming to the Bellcore-GR-253 standards.
- Generates an STM-16c signal conforming to ITU-T recommendation G.707.

1.3.1 OC-48c/STM-16c TX signals

OC-48c/STM-16c signal formation:

- Internally generated signal: The payload in 4 x STS-12c SPE/VC-4-4c contains a “Bulk” signal or ATM cells.
- Internally generated signal: The payload of one STS-12c SPE/VC-4-4c signal contains a “Bulk” signal or ATM cells. The other three STS-12c SPE/VC-4-4c signals are filled with HP-UNEQ
- Internally generated signal: The payload of the STS-48c SPE/VC-4-16c signals contains a “Bulk” signal
- Signal taken completely from receiver

1.3.2 Scrambling

Scrambling is as per ITU-T recommendation G.707.
The scrambler cannot be switched off.

1.3.3 Overhead generator

1.3.3.1 Section overhead (SOH), Transport overhead (TOH)

STM-16, OC-48 section overhead

see Sec. 1, Page S-31

Settings can be made in the entire SOH, TOH excluding the B1 and B2 bytes and the complete pointer line (H1, H2, H3).

XX:	Inserted by parity formation (B1, B2)
Line 4a:	SDH pointers (AU-4)
Line 4b:	SDH pointers (AU-3)
Line 4c:	SONET pointers (STS-1 SPE)
Line 4d:	SONET pointers (STS-3c)
Line 4e:	SDH pointers (AU-4, VC-4-4c)
Line 4f:	SONET pointers (STS-12c SPE)
Line 4g:	SDH pointers (AU-4, VC-4-16c)
Line 4h:	SONET pointers (STS-48c SPE)
Line 9:	Z1 and Z2 are used for SONET only

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

Overhead byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead Sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11: E1, F1, E2
D1 to D3, D4 to D12 (byte group)
- Dynamic via DCC/ECC interface socket [40] (V.11): E1, F1, E2 (single byte)
- Dynamic via DCC/ECC interface socket [40] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

SOH, TOH	SOH	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	...	#1	...	#1	...	#1	...	#16
	1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	A2 28	J0 C1 01	J0 C1 02	J0 C1 03	J0 C1 04	J0 C1 05	J0 C1 06	J0 C1 07	J0 C1 08	J0 C1 09	J0 C1 0A	J0 C1 0B	J0 C1 0C	J0 C1 0D	J0 C1 0E	J0 C1 0F	J0 C1 10	...	#1	...	#1	...	#16
	2	B1 XX	-- -- 00 00	E1 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	F1 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00
	3	D1 00	-- -- 00 00	D2 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	D3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4a	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	Y 9B	H1 68	Y 9B	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4b	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	H1 68	Y 9B	H1 68	Y 9B	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4c	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	Y 93	H1 60	Y 93	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4d	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	H1 60	Y 93	H1 60	Y 93	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4e	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4f	H1 60	Y 93	Y 93	Y 93	H1 60	Y 93	Y 93	Y 93	H1 60	Y 93	Y 93	Y 93	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4g	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	4h	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	H2 00	H2 00	H2 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
	5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	K2 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00
	6	D4 00	-- -- 00 00	D5 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	D6 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00
	7	D7 00	-- -- 00 00	D8 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	D9 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00
	8	D10 00	-- -- 00 00	D11 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	D12 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00	-- -- 00 00
	9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	Z2 00	Z2 00	E2 00	M1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00

Table S-1 SOH, TOH contents; STM-16, OC-48

1.3.4 Path overhead (POH), high-order

1.3.4.1 Contiguous concatenation

Standard overhead

POH byte	POH	**"Fixed Stuff" Column #2 to #4 Container: STS-12c SPE/VC-4-4c** Fixed stuffing (3 columns)	**"Fixed Stuff" Column #2 to #16 Container: STS-48c SPE/VC-4-16c** Fixed stuffing (15 columns)
J1 (ASCII)	"WG HP-TRACE"	"00"	"00"
B3 (hex)	Inserted by parity formation	"00"	"00"
C2 (hex)	"13" for ATM mapping "FE" for BULK (STM-4) "01" for BULK (OC-12)	"00"	"00"
G1 (hex)	"00"	"00"	"00"
F2 (hex)	"00"	"00"	"00"
H4 (hex)	"FF"	"00"	"00"
F3 (hex)	"00"	"00"	"00"
K3 (hex)	"00"	"00"	"00"
N1 (hex)	"00"	"00"	"00"

Table S-2 POH contents

Contents of VC-4c POH #1 bytes

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

1.3.5 Generation of pointer actions

1.3.5.1 Contiguous concatenation

Stimulation

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

1.3.6 OC-48c/STM-16c anomaly insertion

Anomaly insertion . . . . . B1, B2, B3 parity errors
REI-L/MS-REI, REI-P/HP-REI

Trigger modes . . . . . .Single
or Rate

A bit error rate is inserted when Rate is selected.

Anomaly	Single	Rate[1]	Burst m, n (frame)
B1 (OC-48c/STM-16c)	yes	2E-5 to 1E-10	m = 1 to 196000
B2 (OC-48c/STM-16c)	yes	2E-3 to 1E-10	m = 1 to 196000
REI-L (OC-48c) MS-REI (STM-16c)	yes	2E-3 to 1E-10	m = 1 to 196000
B3 (STS-12c SPE/VC-4-4c)	yes	2E-4 to 1E-10	m = 1 to 196000
B3 (STS-48c SPE/VC-4-16c)	yes	2E-5 to 1E-10	m = 1 to 196000
REI-P (STS-12c SPE) HP-REI (VC-4-4c)	yes	2E-4 to 1E-10	m = 1 to 196000
REI-P (STS-48c SPE) HP-REI (VC-4-16c)	yes	2E-5 to 1E-10	m = 1 to 196000

1 Mantissa: 1 to 9, Exponent: -3 to -10 (integer values)

Table S-3 Anomalies (OC-12c/STM-16c) and trigger modes

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.3.7 OC-48c/STM-16c defect generation

Defect	Sensor function test	Sensor threshold test	
-	On / Off	M in N	|---t1---| |------t2------|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-2488	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-L (OC-48c) RS-TIM (STM-16c)	yes	-	-
AIS-L (OC-48c) MS-AIS (STM-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-L (OC-48c) MS-RDI (STM-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP_P (STS-12c SPE/STS-48c SPE)[1] AU-LOP (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-P (STS-12c SPE/STS-48c SPE)[1] AU-AIS (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-P (STS-12c SPE/STS-48c SPE) HP-UNEQ (VC-4-4c/VC-4-16c)	ja	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-P (STS-12c SPE/STS-48c SPE) HP-PLM (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-P (STS-12c SPE/STS-48c SPE) HP-RDI (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-P (STS-12c SPE/STS-48c SPE) HP-TIM (VC-4-4c/VC-4-16c)	yes	-	-

1 Insertion in all four pointers (AU-4) for STS-12c SPE/VC-4-4c
Insertion in all sixteen pointers (AU-4) for STS-48c SPE/VC-4-16c
2 X = 1 to 4 for STS-12c SPE/VC-4-4c
X = 1 to 16 for STS-48c SPE/VC-4-16c
Insertion in selected pointer (AU-4) only

Table S-4 Defects (OC-48c/STM-16c)

Insertion of **defects** and **anomalies** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4 Payload generation

1.4.1 BULK signal generator

Only with option BN 3035/90.90 or BN 3035/90.93

1.4.1.1 Payload

Bit rate (STS-48c SPE/VC-4-16c) . . . . . 2396.16 Mbit/s
Bit rate (STS-12c SPE/VC-4-4c) . . . . . 599.04 Mbit/s

Structure . . . . . unframed

1.4.1.2 Bit patterns

Digital word . . . . . 16 bits

Pseudo-random bit sequences . . . . PRBS 23, PRBS 23 inverted, PRBS 31, PRBS 31 inverted

1.4.1.3 Anomaly insertion

The following anomaly can be inserted in addition to those described in Sec. 1.3.6, Page S-33:

Anomaly	Single	Rate[1]
TSE	yes	1E-3 to 1E-9
1 Mantissa: 1, Exponent -3 to -9 (integer values)		

Table S-5 Additional anomaly (STS-12c SPE/VC-4-4c, STS-48c/VC-4-16c)

Anomaly insertion . . . . . Test sequence error (TSE)

Trigger modes . . . . . Single or Rate

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4.2 ATM generator for STS-12c SPE/VC-4-4c container

Only with options BN 3035/90.70 (ATM Module) and BN 3035/90.91

1.4.2.1 Scrambling

Scrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$). The function can be disabled.

1.4.2.2 Anomaly insertion

The following anomalies can be inserted in addition to those described in Sec. 1.3.6, Page S-33.

Anomaly	**Single**	**Rate[1]**	**Sensor threshold**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
AAL-1 cell loss	yes	1E-3 to 1E-6	-
AAL-1 CRC	yes	1E-3 to 1E-6	-
AAL-1 PE	yes	1E-3 to 1E-6	-

1 Mantissa: 1 only, Exponent: -1 to -6 (integer values)
2 Uncorrectable header error
3 Correctable header error

Table S-6 Additional anomalies

The AAL-1 cell loss, AAL-1 CRC and AAL-1 PE anomalies refer to the measurement channel. Test sequence errors (TSE) are inserted in the ATM payload or in the AAL-1 payload of the test channel.

Correctable and uncorrectable header errors are inserted in the overall cell stream.

1.4.2.3 Defect generation

The following defects can be generated in addition to those described in Sec. 1.3.7, Page S-34.

Defect	Sensor function test	Single
	On / Off	
LCD[1]	yes	yes
VP-AIS	yes	yes
VP-RDI	yes	yes
VC-AIS[2]	yes	yes
VC-RDI[3]	yes	yes
Vx-AIS[4]	yes	yes
Vx-RDI[4]	yes	yes

1 LCD (Loss of Cell Delineation) is generated by uncorrectable header errors in ≥ 7 consecutive cells.
2 AIS: Alarm Indication Signal; VC: Virtual Channel; VP: Virtual Path
3 RDI: Remote Defect Indication
4 For Vx-AIS and Vx-RDI defects are inserted in the VP and VC in parallel.

Table S-7 Additional defects

1.4.2.4 Test channel

Cells

Header

UNI/NNI, VCI, VPI, PT and CLP . . . . . settable
HEC . . . . . formed automatically

Payload

Pseudo-random bit sequences . . . . . PRBS 11, PRBS 15, PRBS 20, PRBS 23
Digital word . . . . . 16 bits

Load profiles

Constant, Equidistant, Burst

Constant load profile

Load setting . . . . . 14.976 to 149760 kbit/s

Resolution dependent on load range setting
14.976 to 1482.624 kbit/s . . . . . 14.976 kbit/s
149.76 to 14826.24 kbit/s . . . . . 149.76 kbit/s
1497.6 to 149760 kbit/s . . . . . 1497.6 kbit/s

Equidistant load profile setting range

Cell spacing . . . . . 4 to 40000 cell periods
Maximum cell spacing deviation . . . . . ± 1 cell period

Resolution depending on cell spacing range setting
4 to 400 . . . . . 4 cell periods
40 to 4000 . . . . . 40 cell periods
400 to 40000 . . . . . 400 cell periods

Burst load profile setting range

Maximum burst length . . . . . 4092 cells / 2.79 ms
Burst load . . . . . 1497.6 to 149760 kbit/s
Resolution . . . . . depends on burst length

Maximum burst period . . . . . 131068 cells / 89 ms

Load units . . . . . Mbit/s, Cells/s, %
Time units . . . . . cell period

1.4.2.5 Background load

A channel is generated as background load. The test channel has priority.

Header . . . . . freely selectable

Payload . . . . . byte by byte constant, bytes freely selectable

Load profile . . . . . CBR, Fill

Constant bit rate (CBR) . . . . . 449280 kbit/s

Filling up to . . . . . 149760 / 599040 kbit/s

1.4.2.6 Fill cells

The cell stream is filled with IDLE or UNASSIGNED cells. Either can be selected.

1.4.2.7 AAL-1 segmentation

PDU signals with system bandwidths of 1,5 Mbit/s, 2 Mbit/s, etc. can be transmitted in the AAL-1 in the test channel.

Possible payload patterns for 2 Mbit/s . . . . . PRBS unframed,
PRBS in PCM30,
PRBS in PCM30CRC

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [44], optical

Caution

Destruction of input [44]

The maximum input level of -8 dBm must not be exceeded. Otherwise, the optical input can be destroyed.

⇒ Insert an optical attenuator in any case:
- for RX - TX loop operation
- for higher input levels

Connector . . . . . 2.5 mm (PC)

"Fiber-to-fiber" adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Input sensitivity
STM-16/OC-48 *** . . . . . -8 to -28 dBm

Max. permitted input level . . . . . -8 dBm

Wavelength . . . . . 1100 to 1600 nm

The receiver meets the requirements of ITU-T G.957 classes S16.2, L16.2, L16.3 or S16.1 and L16.1.

Optical signal level display

Resolution . . . . . 1 dBm

Accuracy . . . . . ±3 dB

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

LOS threshold . . . . . < -30 dBm

2.1.2 Signal input [43], electrical

Connector . . . . . unbalanced (coaxial)

Type . . . . . SMA

Input impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Input voltage range . . . . . 300 mVpp to 1Vpp

Bit rate . . . . . 2488.32 Mbit/s

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

2.1.3 Clock output [42]

For the recovered receive clock

Frequency . . . . . 2488.32 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 100 mVpp

2.1.4 Clock recovery

See “Specifications” of the mainframe instrument.

2.2 SDH and SONET RX signals

- Evaluation of OC-48c signal conforming to Bellcore GR-253 standards.
- Evaluation of STM-16c signal conforming to ITU-T recommendation G.707.

2.2.1 OC-48c/STM-16c RX signal

OC-48c/STM-16c signal evaluation:

- Analysis of Transport Overhead (TOH) / Section Overhead (SOH), Path Overhead (POH) and payload (BULK) for STS-12c SPE/VC-4-4c containers either directly or in conjunction with the ATM module (option BN 3035/90.70).
- Analysis of Transport Overhead (TOH) / Section Overhead (SOH), Path Overhead (POH) and payload (BULK) for STS-48c SPE/VC-4-16c containers.
- Analysis of Transport Overhead (TOH) / Section Overhead (SOH) and loop-through of STS-12c SPE/VC-4-4c signal to transmitter (“Through” mode).

2.2.2 Descrambling

Descrambling is as per ITU-T recommendation G.707.
The descrambler cannot be switched off.

Tip: Make sure that there are no long sequences of zeros or ones in the data stream of unscrambled input signals.

2.3 Measurement modes

2.3.1 Evaluation of section overhead (SOH), transport overhead (TOH)

Display

Complete SOH, TOH: (16 channel-associated part SOH) . . . . . hexadecimal

Trace Identifier J0. . . . . .ASCII, plain text

Overhead Capture . . . . . .see Section 1 “Extended Overhead Analysis” option BN 3035/90.15

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . E1, F1, E2 (single byte)

using pseudo-random bit sequence PRBS11 . . . . . .D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) . . . . . E1, F1, E2 (single byte)

DCC/ECC interface, socket [21] (V.11) . . . . . D1 to D3, D4 to D12, K1 to K2 (byte group)

2.3.2 Evaluation of path overhead (POH)

2.3.2.1 Contiguous concatenation

Display

Complete POH . . . . . hexadecimal

Trace Identifier J1 . . . . . ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) F2, N1

2.3.3 Measurement of AU pointer actions

Evaluation

The AU pointer is indicated as an absolute value. The direction and number of pointer movements are detected.

NDF (new data flag) is detected and counted.

Display

- Number of AU pointer operations:
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address
- Number of NDF events
- Corresponding clock deviation
- AU-NDF and NDF-P can be indicated by the LED display on the front panel
  (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP” and it indicates “NDF-P” in addition to “LOP-P”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are displayed as histograms with a selectable time resolution of seconds, minutes, hours or days.

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are printed out as a table with a resolution of 1 second.

2.3.4 Anomaly measurements

Evaluation

All anomalies are counted and recorded simultaneously.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

Anomalies are indicated by LEDs:

CURRENT LED (red) is on while the anomaly is present.

HISTORY LED (yellow)is on if the anomaly occurred at least once or is still present during the current measurement interval.

Anomaly	**LED**
OOF-2488	LOF/OOF
B1 (OC-48c/STM-16c)	B1/B2
B2 (OC-48c/STM-16c)	B1/B2
REI-L (OC-48c) MS-REI (STM-16c)	-
B3 (STS-12c SPE/STS-48c SPE/VC-4-4c/VC-4-16c)	B3
REI-P (STS-12c SPE/STS-48c SPE) HP-REI (VC-4-4c/VC-4-16c)	-

Table S-8 LED display of anomalies (OC-48c/STM-16c)

Evaluation and display of B2 errors refers to the concatenated data stream (BIP-384).

Evaluation and display of B3 errors for contiguous concatenation: BIP-8

2.3.5 Defect detection

Evaluation

All defects that are present are evaluated and recorded simultaneously as far as possible. Recording takes place only within a started measurement interval.

Time resolution of defects . . . . . .100 ms

Display

Defects are indicated by LEDs:

CURRENT LED (red) is on while the defect is present.

HISTORY LED (yellow)is on if the defect occurred at least once or is still present during the current measurement interval.

Defect	**LED**
LOS (optisch)	LOS
LOF-2488	LOF/OOF
TIM-L (OC-48c) RS-TIM (STM-16c)	-
AIS-L (OC-48c) MS-AIS (STM-16c)	MS-AIS/AIS-L
RDI-L (OC-48c) MS-RDI (STM-16c)	MS-RDI/RDI-L
LOP-P (STS-12c SPE/STS-48c SPE) AU-LOP (VC-4-4c/VC-4-16c)	AU-LOP/LOP-P
LOP-Cx[1]	AU-LOP/LOP-P
AIS-P (STS-12c SPE/STS-48c SPE)[1] AU-AIS (VC-4-4c/VC-4-16c)	AU-AIS/AIS-P
AIS-Cx[2]	AU-AIS/AIS-P AU-LOP/LOP-P
UNEQ-P (STS-12c SPE/STS-48c SPE) HP-UNEQ (VC-4-4c/VC-4-16c)	HP-UNEQ/UNEQ-P
PLM-P (STS-12c SPE/STS-48c SPE) HP-PLM (VC-4-4c/VC-4-16c)	HP-PLM/PLM-P
RDI-P (STS-12c SPE/STS-48c SPE) HP-RDI (VC-4-4c/VC-4-16c)	HP-RDI/RDI-P
TIM-P (STS-12c SPE/STS-48c SPE) HP-TIM (VC-4-4c/VC-4-16c)	-

1 AU-LOP is indicated if LOP is detected in at least one AU-4 pointer.
2 AU-AIS is indicated if AIS is detected in all four AU-4 pointers.
If AU-AIS is detected in one, two or three AU-4 pointers, AU-LOP-LOP-P is indicated.

Table S-9 LED display of defects (OC-48c/STM-16c)

2.4 Payload

2.4.1 BULK signal receiver

Only with option BN 3035/90.90 or BN 3035/90.93

2.4.1.1 Bit pattern payloads

See Sec. 1.4.1.1, Page S-35 and Sec. 1.4.1.2, Page S-35

2.4.1.2 Anomaly measurements

The following anomaly can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-44:

Anomaly	LED
TSE	TSE

Table S-10 LED display of additional anomaly

2.4.1.3 Defect detection

The following defect can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-45:

Defect	LED
LSS	LSS

Table S-11 LED display of additional defect

2.4.2 ATM receiver section

Only with option BN 3035/90.70 and BN 3035/09.91

2.4.2.1 Descrambling

Descrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$).
The function can be disabled.

2.4.3 Measurement modes

2.4.3.1 Anomaly measurements

The following anomalies can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-44.

Anomaly	LED	Explanation	
HCOR	-	Correctable Header Error	
HUNC	-	Uncorrectable Header Error	
CER	-	Cell Error Ratio	for measurements using test cells
CLR	-	Cell Loss Ratio	
CMR	-	Cell Misinsertion Rate	
AAL-1-CRC	-	AAL1 CRC Error	for AAL-1 measurements
AAL-1-PE	-	AAL1 Parity Error	
AAL-1-CLR	-	AAL1 Cell Loss Ratio	
AAL-1-CMR	-	AAL1 Cell Misinsertion Rate	

Table S-12 Indication and evaluation of anomalies

The anomalies HUNC and HCOR apply to the complete cell stream. All other anomalies apply to the measurement channel only.

2.4.3.2 Defect detection

The following defects can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-45.

Defect	LED	Explanation	
LCD	LOF / LCD	Loss of Frame / Loss of Cell Delineation	
OCR	LOF / LCD	Overflow Cell Rate[1]	
OCLR	-	Cell Loss Overflow[2]	for measurements using test cells
OCMR	-	Cell Misinserted Overflow[3]	
VC-AIS	-	Virtual Channel Alarm Indication Signal	
VC-RDI	-	Virtual Channel Remote Defect Indication	
VP-AIS	-	Virtual Path Alarm Indication Signal	
VP-RDI	-	Virtual Path Remote Defect Indication	
AAL-1-OOS	-	AAL1 Out of Sync	

1 Test channel: Maximum cell rate (CBR) = 149760 kbit/s;
Max. consecutive cells at 599040 kbit/s = 400
2 More than 255 cell losses in 100 ms or relative to the last test cell
3 More than 255 misinserted cells in 100 ms or relative to the last test cell

Table S-13 LED display of additional defects

2.4.3.3 ATM performance measurements

Error-related performance parameters

The measurements are made using test cells.

Results

Lost Cell Count, Cell Loss Ratio . . . . . CLR
Misinserted Cell Count, Cell Misinserted Rate . . . . . CMR
Error Cell Count, Cell Error Ratio . . . . . CER

Cell transfer delay

The measurement is made using test cells.

Display . . . . . rate distribution
Resolution . . . . . 160 ns to 0.355 s
Measurement range . . . . . 20 µs to 42.9 s
Measurement range offset . . . . . 0 to 0.167 s
Units . . . . . µs

Cells with transfer delays outside the measurement range are counted as class 0 (underflow) or class 127 (overflow).

Cell delay variation

The measurement is made using test cells.

Display . . . . . rate distribution,
minimum delay,
maximum delay,
average delay,
peak-to-peak-CDV

The results are only valid if no cell delays outside the measurement range are detected.

2.4.4 User channel analysis and load measurement

Cell filters (VCI, VPI, CLP) for extracting the test channel.

The VCI and CLP filters can be disabled

Mean cell rate

The measurement is made over all connections in parallel and in the test channel simultaneously.

Measurement interval . . . . . 1 s
Resolution 0.01%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Peak cell rate

The measurement is made in the test channel.

Measurement interval . . . . . 1 s
Resolution 0.1%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Channel loading histogram

The channel loading histogram indicates the distribution of 100 ms measurement intervals according to measured load.

Measurement interval . . . . . 100 ms
Number of classes 101
Class “0” contains the number of 100 ms intervals in which a load of 0% was measured.
Class width 1%
Load display . . . . . Mbit/s, Cells/s, %

User channel cell distribution

Display of cells in the user channel classified as user cells, OAM cells and user cells with CLP indicator.

Measurement interval . . . . . 1 s
Display . . . . . cell count

Test channel

Maximum cell rate (CBR) . . . . . 149760 kbit/s

Max. consecutive cells at 599040 kbit/s . . . . . 400 cells

Test cell format

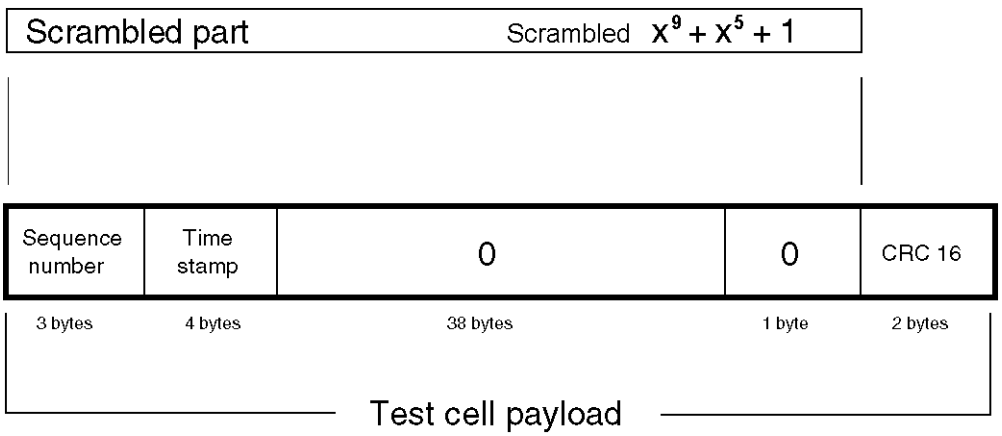


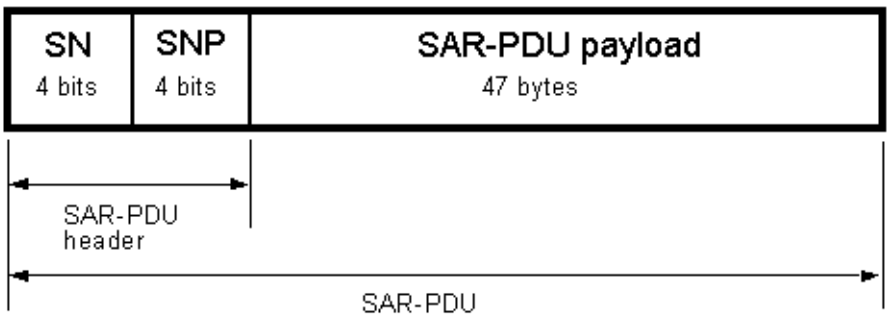
Fig. S-1 Test cell format to ITU-T O.191 (Draft 4/95)

2.4.4.1 AAL-1 reassembly

AAL-1 structured cells are reassembled from the SAR-PDU. The format is shown in the figure below. The TSE measurement is performed using framed or unframed pseudo-random bit sequences (PRBS) mapped into the SAR-PDU payload.

The following payload patterns are available for measurements:

- PRBS unframed
- PRBS in PCM-30 frame
- PRBS in PCM-30 frame (with CRC)



SN: Sequence Number
SNP: Sequence Number Protection
PDU: Protocol Data Unit
SAR: Segmentation and Reassembly

Fig. S-2 SAR-PDU format for AAL-1 cells