California INSTRUMENTS

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INSTRUCTION MANUAL

MODEL 850T/855T

Invertron®

SECTION I—DESCRIPTION

1.1 INTRODUCTION

This instruction manual contains information relative to the installation, operation, calibration and maintenance of California Instruments 850T/855T Series Precision Oscillators. A detailed theory of operation is provided as an aid for maintenance personnel. A complete parts listing, schematic and component location diagrams are also supplied.

1.2 MODEL NUMBER DESCRIPTION

All oscillators in the 850T/855T Series have a five place model number which describes the oscillator series and the number of output phases. In addition, a "D" is placed after the model number if the oscillator is to be used in the three-phase, open delta configuration. The following examples illustrate this numbering system.

Example 1: 850T-1.

This is a variable frequency oscillator with single phase output.

Example 2: 850T-3D

This is a variable frequency oscillator with two-phase 60° open delta output (Phase C leading Phase A).

Example 3: 855T-2.

This is a fixed frequency oscillator with two-phase outputs, 90° displaced. (Phase C leading Phase A).

Example 4: 855T-3.

This oscillator is fixed frequency with three-phase wye output connections.

NOTE

Although the 855T is designated as a fixed frequency oscillator and will be set to the customer specified frequency, internal switches permit reprogramming the oscillator frequency.

1.3 GENERAL DESCRIPTION

California Instruments' 850T Series variable frequency oscillators and 855T Series fixed frequency oscillators are designed to plug into and derive their power from any of the Invertron® AC Power Sources. The output of the oscillator then provides the input frequency and amplitude drive for the Power Source. They employ digital logic techniques for frequency generation with a crystal controlled oscillator serving as the reference for the digital logic circuits. This technique provides long term frequency stability not obtainable with analog circuits. The 850T Series has three frequency ranges selected with a front panel switch. There are four frequency selection controls, permitting precise adjustment of the output frequency with resolution of one part in ten-thousand. Frequency is adjustable in 0.01 Hz steps from 0.01 Hz to 99.99 Hz in the X1 range, in 0.1 Hz steps from 0.1 to 999.9 Hz in the X10 range and in 1 Hz steps from 1 to 9999 Hz in the X100 range. By setting the internal switches and making other minor internal changes to the 855T, its output frequency may be similarly adjusted to any frequency selectable in 1 Hz steps.

The crystal oscillator reference has an average frequency stability of five parts per million per degree Centigrade. Thus, with the frequency having been set at room temperature, the maximum variation would be approximately 125 parts per million (0.0125%) over the 0 to 55°C range. The oscillator frequency is divided by digital logic circuits to the selected output frequency and then filtered to remove harmonic components.

The 850T/855T Series Oscillators will shut down if the frequency is outside of factory set limits. This prevents selection of a frequency outside the operating limits of the associated power source, in the case of the 850T, and protects against a malfunction of the oscillator circuits that would produce a frequency outside these limits.

The 850T/855T Series Oscillators are equipped with a "soft start" feature that slowly increases the output amplitude from zero to the set level whenever the

unit is first turned on. The 850T also "soft starts" when resuming operation after automatic shutdown caused by selection of an out-of-limit frequency.

Both the 850T and 855T Oscillators may be equipped with optional circuit boards to provide two- or three-phase outputs. Additionally, the output phases may be set to any 30 degree increment relative to the reference phase. Because of the digital techniques employed, the electrical angle between phases remains constant irrespective of frequency.

1.4 ACCESSORY EQUIPMENT

An Extender Assembly, Part No. 4800-703 is available for use with the 850T/855T Series Oscillators, permitting test and adjustment outside of the associated power source.

1-5 SPECIFICATIONS AND PERFORMANCE DATA

Specifications and performance data for the 850T/855T Series Precision Oscillators are listed in Table 1-2. All units are factory tested to these specifications in accordance with California Instruments Division test procedures as detailed in Section V of this manual.

Table 1-1. Specifications.

FREQUENCY RESOLUTION:	1 part in 10,000
FREQUENCY ACCURACY:	0.005% at 23°C
FREQUENCY STABILITY:	5 ppm per °C. Average Temperature coefficient from 0 to 55°C.
FREQUENCY RESPONSE:	±1% from 45 Hz to 1 KHz. ±2% from 45 Hz to 5 Khz. ±3% from 45 Hz to 10 KHz.
AMPLITUDE STABILITY:	±0.1% for 24 Hrs at 23°C.
AMPLITUDE TEMPERATURE COEFFICENT:	0.02% per °C Average temperature coefficient from 0 to 55°C.
TOTAL HARMONIC DISTORTION:	0.3% max. on 855T and on X100 range of 850T. 0.15% on other ranges at full output.
PHASE ACCURACY:	
Two Phase:	90° 1° from 45 Hz to 5 KHz. 90° 2° from 5 Khz to 10 KHz. (Phase C leading Phase A)
Three Phase Delta:	60° 1° from 45 Hz to 5 KHz. 60° 2° from 5 KHz to 10 KHz. (Phase C leading Phase A).
Three Phase Wye:	120° 1° from 45 Hz to 5 KHz. 120° 2° from 5 Khz to 10 KHz.
GENERAL:	
Size:	Standard Plug-In size for all Invertron® AC Power Supplies.
Input Power:	Available from associated Invertron® AC Power Sources.
Front Panel Finish:	Gray, 26440 per Federal Standard 595 with black silk screened lettering.

CAUTION

Voltages up to 500 Volts AC are available in certain associated Invertrons®. This equipment generates potentially lethal voltages.

DEATH

on contact may result if personnel fail to observe safety precautions. Do not touch electronic circuits when power is applied. Avoid contact with connector pins C and D of the plug-in oscillator, the primary power circuits and output circuits of the associated Invertron® if oscillator is tested and/or adjusted with Invertron®.

SECTION II
INSTALLATION AND OPERATION

2.1 UNPACKING

Individual oscillators are shipped in cardboard containers with protective inner packing. Do not destroy this packing container until the unit has been inspected for possible damage in shipment.

2.2 POWER REQUIREMENTS

The California Instruments 850T/855T Series Precision Oscillators operate from +25 volts DC and −25 volts DC at 0.040 amperes. In addition, 115 volts AC at 10 volt-amperes is required. These power inputs are normally obtained from an associated Invertron® power source.

2.3 FUSE REQUIREMENTS

Separate fusing of the power sources for the California Instruments 850T/855T Series Oscillators is not required.

2.4 ACCEPTANCE TEST PROCEDURE

Inspect the unit for any possible shipping damage immediately on receipt. If damage is evident, notify carrier. **DO NOT return an instrument to the factory without prior approval.** If the unit appears to be in good condition, perform the following:

Mount the oscillator in the appropriate rack housing or, otherwise, apply +25 volts DC, −25 volts DC and 115 volts AC to the unit.

2.4.1 MODEL 850T SINGLE-PHASE OSCILLATORS

The output of a single-phase oscillator should be variable from 0 to 5.000 volts measured between pins 2 and 8 (ground) of connector J2. There is no upper level adjustment. Frequency should be variable in 0.01 Hz steps from 0.01 Hz to 99.99 Hz with the RANGE switch in the X1 position, in 0.1 Hz steps from 0.1 to 999.9 Hz with the switch in the X10 position and in 1 Hz steps from 1 to 9999 Hz with the switch in the X100 position. When monitored with an oscilloscope, distortion should not be visible. Detailed test procedures are provided in the TEST PROCEDURE section of this manual. They should be consulted if further evaluation of the oscillator is required at this time.

2.4.2 MODEL 850T TWO-PHASE OSCILLATORS

The details of paragraph 2.4.1 apply to the reference phase of these oscillators. The phase C (ϕC) output, measured between pins 8 and 9 of J2, should have the same amplitude as the ϕA output (± 0.05 volts) at any position of the front panel amplitude control. When monitored with an oscilloscope, distortion should not be visible on any phase. Detailed test procedures are provided in Section IV of this manual. They should be consulted if further evaluation of the oscillator is required at this time.

2.4.3 MODEL 850T THREE-PHASE OSCILLATORS

The details of paragraph 2.4.1 apply to the reference phase of these oscillators. The phase B (ϕB) output, measured between pins 7 and 8 of J2, and the phase C (ϕC) output, measured between pins 8 and 9 of J2, should have the same amplitude (± 0.05 volts) as the A output at any position of the front panel amplitude control. When monitored with an oscilloscope, distortion should not be visible on any phase. When monitored with a phase meter, the angle between the ϕB and ϕC outputs should be 120°. Detailed test procedures are provided in Section IV of this manual. They should be consulted if further evaluation of the oscillator is required at this time.

2.4.4 MODEL 855T SINGLE-PHASE OSCILLATORS

The details of paragraph 2.4.1 apply to these oscillators except that the frequency is fixed at that indicated in the manual addendum.

2.4.5 MODEL 855T TWO-PHASE OSCILLATORS

The details of paragraph 2.4.2 apply to these oscillators except that the frequency is fixed at that indicated in the manual addendum.

2.4.6 MODEL 855T THREE PHASE OSCILLATORS

The details of paragraph 2.4.3 apply to these oscillators except that the frequency is fixed at that indicated in the manual addendum.

2.5 MECHANICAL INSTALLATION AND WIRING

The 850T/855T Series Oscillators fit directly into the California Instruments Solid State Invertron® Series of power amplifiers. All power for the oscillator, as well as signal output(s) is coupled through the printed circuit connector at the rear of the oscillator. Table 2-1 lists the voltages and applicable connector pins.

Table 2-1. Input/Output Connections.

PIN	FUNCTION
1	Phase A Output signal low
2	Phase A Output signal high
3	Power ground
4	+25 volt input
5	−25 volt input
6	Phase B signal output low
7	Phase B signal output high
8	Phase C signal output low
9	Phase C signal output high
10	External sync input
C	115 volts AC line high
D	115 volts AC line low

The single phase versions of the 850T and 855T Series Oscillators have only a ϕA output. The two-phase (multiphase) versions have ϕA and ϕC outputs while the three-phase verisons have ϕA, ϕB and ϕC outputs.

The oscillators require 115 volts AC, which is rectified, filtered and regulated to 5 volts DC for powering the digital circuitry.

2.6 OPERATING CONTROLS

The 850T Series oscillators have four frequency selector dials on the front panel with which each digit of the output frequency is individually selected. An AMPLITUDE control varies the output level of all signal outputs from 0 to 5.0 volts. The 855T Series oscillators, being fixed frequency, have only the AMPLITUDE control on the front panel.

The output signals of the multi-phase and three-phase versions of both the 850T and 855T are factory adjusted for equal amplitude of all three phases. The GAIN control on each power amplifier of a multi-phase or three-phase system is used as a trim control to adjust each of the output leg voltages so that they are precisely equal to each other.

CAUTION

REMOVE POWER FROM THE SOLID STATE INVERTRON® BEFORE REMOVING OR INSERTING THE PLUG-IN OSCILLATOR.

SECTION III
THEORY OF OPERATION

3.1 GENERAL

The California Instruments 850T/855T Series Precision Oscillators, because they are controlled by a quartz crystal, provide a degree of frequency stability that surpasses, by an order of magnitude, that which is obtainable with analog types. Amplitude stability is also improved since the operating frequency is determined by digital logic circuits. Therefore, the basic "oscillator" is not frequency or temperature sensitive. Output amplitude stability will be affected mainly by frequency and temperature as they affect output amplifiers. Such affects are minimal. The optional multi-phase outputs of this series are developed through a single phase to multi-phase converter.

3.2 FUNCTIONAL DESCRIPTION

The functional descriptions of this section describe the circuitry of the Model 850T oscillator. The Model 855T operates in exactly the same manner except that the frequency is programmed with internal switches and is not variable at the front panel.

3.2.1 PHASE A GENERATOR

3.2.1.1 BASIC OSCILLATOR

The following paragraphs present a functional description of the basic oscillator referenced to the block diagram of Figure 3-1. The crystal oscillator operates at 10.2 MHz. A group of four rate mul-

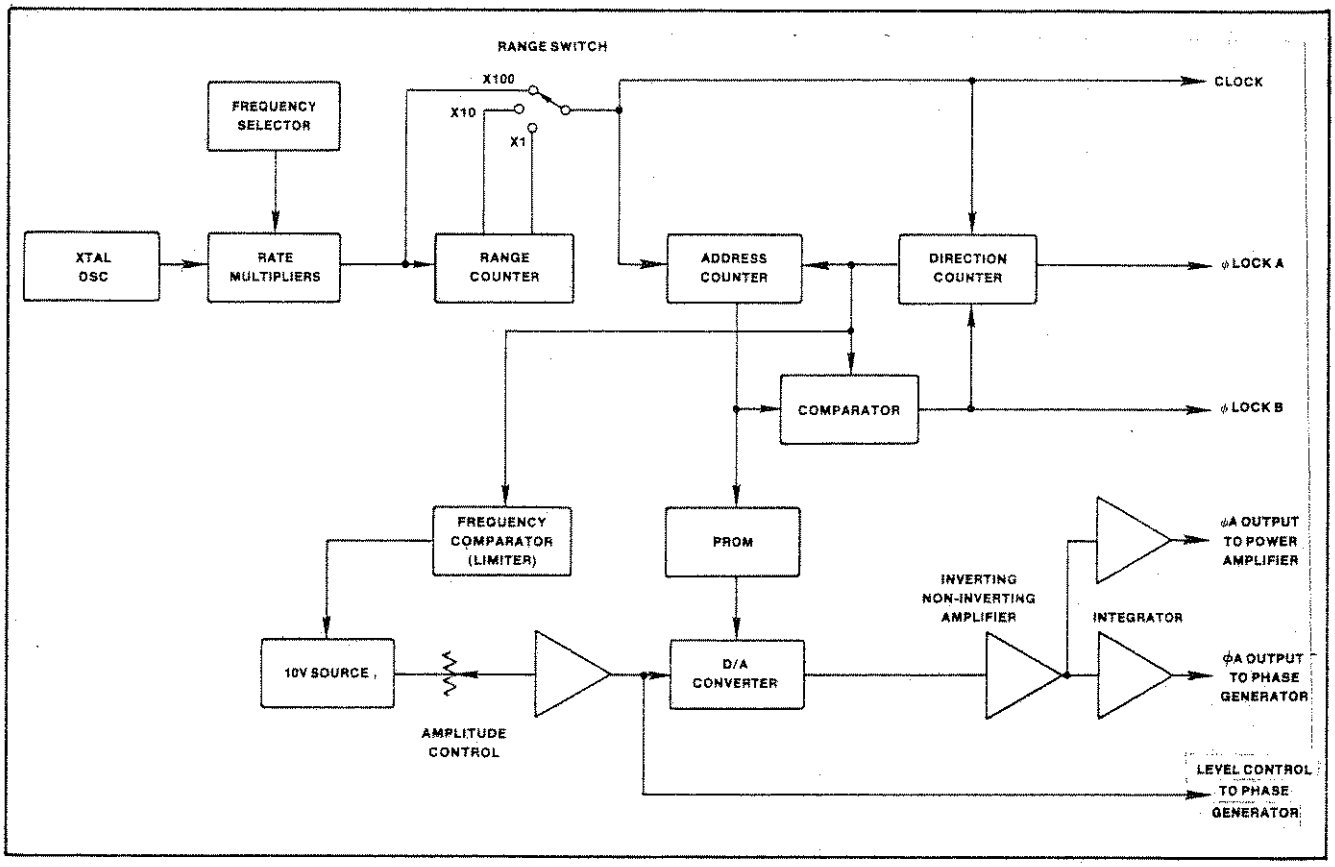


Figure 3-1. Block Diagram, ϕA Generator (Main Board).

tipliers, connected in series, control the number of oscillator pulses that will pass to their output per unit time. That number is dependent on the positions of the four panel rate (frequency) switches to which the rate multipliers are connected. Though not dividers, in the usual sense, the rate multipliers effectively divide the oscillator frequency in accordance with the panel switch settings.

The pulses at the output of the rate multipliers pass to a dual decade counter and the range switch. When the switch is in the X100 position, the rate multiplier output passes through the switch directly to the address counters. When it is in the X10 position, the rate multiplier output is divided by 10 through one half of the dual decade counter before passing to the switch and to the address counters. When it is in the X1 position, it is divided by 100 through both halves of the dual counter before passing to the switch and the address counters. This arrangement permits division of the crystal oscillator by multiplication using factors ranging from 0.001 to 0.9999. The ranges of multiplication, determined by the range switch position, are 0.001 to 0.009999, 0.01 to 0.09999 and 0.1 to 0.9999.

The address counter consists of two binary counters. The four outputs of each counter are connected to inputs of the programmable read-only memory (PROM) which would provide 256 discrete addresses. However, the number of addresses is limited to 255 as the comparator and the direction control counter cause the address counter to change its count mode from up to down at counts 255 and 765 and from down to up at counts 510 and 1020. During each complete cycle, at the output frequency, the counters count up from 000 to 255 for the first 255 clock pulses, count down to 000 during the time of clocks 256 to 510, back to 255 during the time of clocks 511 to 765 and back to 000 during the time of clocks 765 to 1020.

At each of the 255 addresses produced by the address counters, a discrete digital code appears at the output of the PROM and at the input to the digital-to-analog converter (D/A converter). As the address to the PROM progresses from 000 to 255, the PROM output codes cause the output of the D/A converter to increase in 255 steps that describe the first 90 degrees of a sinusoidal waveform. As it progresses from 255 to 000, while the counter is counting down, the second 90 degrees of a sinusoidal waveform are described. The absolute levels at the D/A converter output are determined by the 10 volt reference and the adjustment of the level control.

The waveform at the output of the D/A converter is similar to that of a sinusoidal waveform after full wave rectification except that it is generated in 510 steps (digitally) rather than as an analog signal. To formulate a quasi-sinusoidal waveform, alternate portions of the D/A converter output must be inverted. Alternate clockings of the direction control counter produce a state change at its output that is connected to the inverting/non-inverting amplifier. The state of the counter output determines whether the amplifier will be in its inverting or non-inverting mode. Since the counter output changes state at the end of each half-cycle, alternate half-cycles of the D/A converter output are inverted and the output of the amplifier is a quasi-sinusoidal waveform which is filtered by the integrating amplifier to produce a sinusoidal waveform with very low distortion.

The frequency limiter serves to prevent an output from the oscillator if the selected frequency is outside of the range of the associated power source driven by the 850T. The frequency limits are factory adjusted. The limiter consists of two timers. One limits the upper frequency and the other the lower frequency. The signal that clocks the direction control counter also triggers both sections of the frequency limiter, once for each output cycle. If the frequency is too low, one timer will have timed out before the next trigger pulse occurs. This is sensed and disables the 10 volt reference for the D/A converter, thus shutting off the output. If the frequency is too high, the second timer will not have timed out before the next tigger pulse. This, too, is sensed and also disables the 10 volt reference.

3.2.1.2 MULTI-PHASE OUTPUT GENERATOR

The reference phase, phase A (ϕA), is generated by the basic oscillator described functionally in the preceding paragraphs. Phases B and C (ϕB and ϕC) are generated on an optional second circuit board. The circuits of that board are shown in block diagram form in Figure 3-2. Note that there are similarities between Figures 3-1 and 3-2 in the counter-PROM-D/A converter areas. The address counters are clocked in the same manner as those of the basic oscillator. However, they are preset coincident with the zero degree point of the reference phase, ϕA, to a number corresponding to the difference between the reference phase and the desired angle of Phase C (ϕC). In the standard unit, this will be the equivalent of 120 degrees leading ϕA. The address counters, direction control counter, PROM, D/A converter and inverting/non-inverting amplifier operate in the same manner as those of the basic oscillator. The

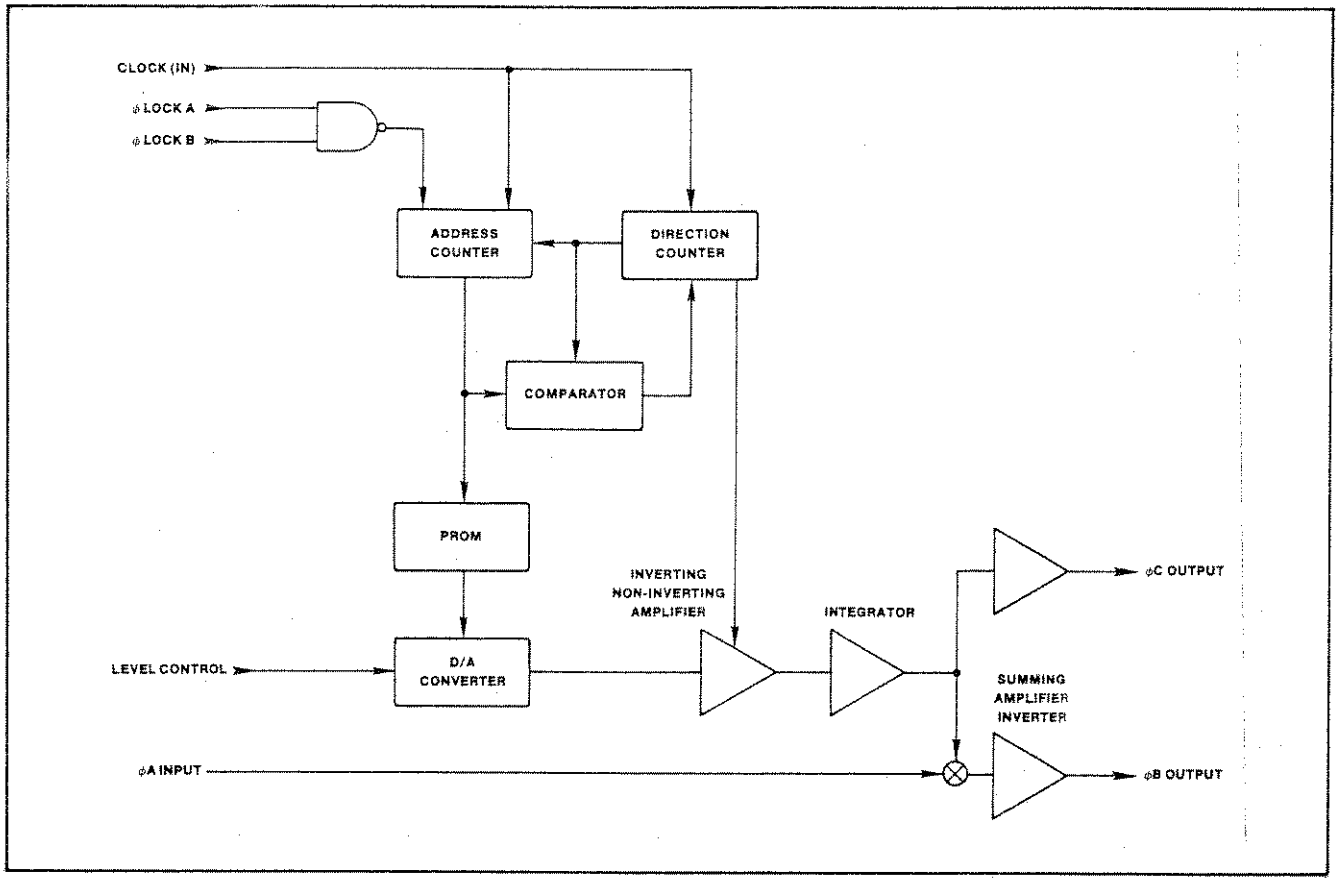


Figure 3-2. Block Diagram, Multi-Phase Generator Board.

output of the φC inverting/non-inverting amplifier is combined with the φA output in the phase B (φB) generator to create the φB output.

3.3 DETAILED CIRCUIT DESCRIPTION

The paragraphs of this section describe in detail the operation of the circuits of the Model 850T Precision Oscillator. Unless otherwise specified, all text within this section is referenced to the schematic diagrams of Figures 6-4 and 6-7. Where components consist of several discrete circuits within a single package, the individual circuits are identified in the text by the basic component identifier followed by a hyphen and the output pin number. For example, the buffer in U7 that has its output connected to pin 8 is identified as U7-8. If this device is located on circuit board A1, its complete identifier is A1U7-8. However, the prefix is used in the following paragraphs only when necessary to avoid confusion in identifying similarly numbered components located on different boards.

3.3.1 PHASE A GENERATOR

3.3.1.1 CRYSTAL OSCILLATOR

Refer to Figure 6-3. Crystal Y1, FET Q3 and associated components comprise an oscillator operating at 10.2 MHz. The oscillator output is bufferd by U7-8 and U7-10 which also convert the oscillator output to a series of TTL compatible pulses.

3.3.1.2 RATE MULTIPLIERS

A complete explanation of the operation of rate multipliers may be found in material published by the device manufacturer. Therefore, the explanation of the rate multiplier circuits herein is limited to that which is peculiar to this design.

A rate multiplier may block pulses appearing at its input from reaching its output or it may pass from one to nine pulses for every ten input pulses, depending on the states of its control inputs. In the 850T Series variable frequency oscillators, the control inputs of the rate multipliers, U1, U2, U3 and U4, are connected to the frequency control switches, S3, S4, S5 and S6. (In the fixed frequency models, they are connected to switches S1 and S2). Rate multiplier U1, for the most significant digit (MSD), is enabled at all times. From 0 to 9 pulses will appear at its output, pin 5, during the time of the first nine of each group of ten oscillator pulses. The actual num-

ber will depend on the setting of the frequency control switch, S6. During the time of the tenth oscillator pulse, its enable output, pin 7, goes low, enabling the next rate multiplier, U3. U3 counts the enable input pulses in the same manner that U1 counted the oscillator pulses. The number that pass to its output will be dependent on the setting of switch S5. However, the output pulse will have the timing and duration of the clock oscillator pulse because it is an input to each rate multiplier. This provides synchronization and uniformity of the pulses at the outputs of the mulitipliers. U4 counts the enabling outputs of U3 and U2 counts those from U4. The output pulses from the rate multipliers are then summed through NAND gate U8-8.

3.3.1.3 RANGE SELECTOR

The range selector circuit consists of dual decade counter U11 and selector switch S7. (S7 is installed only in variable frequency models). When S7 is in the X100 position, the pulses at the output of U8-8 pass directly to the address counters, U13 and U18, and to directional control counter U14. When S7 is in the X10 position, the pulses at the output of U8-8 are divided by a factor of ten in one-half of U11. When it is in the X1 position, they are divided by a factor of 100 through both sections of U11.

3.3.1.4 ADDRESS AND DIRECTION CONTROL COUNTERS

The address counters, U13 and U18, are so called since they produce the address for the two programmable memories (PROM's) U17 and U19. They are binary counters that are synchronously clocked by the output of U8-8 or by one of the outputs of U11, depending on the position of S7. However, U18 is enabled by the output of U13 only between the rising edges of the 15th and 16th clock pulses and will be clocked by the rising edge of the 16th pulse. Therefore, U13 must be clocked sixteen times for U18 to be clocked once, thirty-two times for it be clocked twice, etc. The four stage outputs of U13 and U18 are connected to the eight inputs of U17 and U19 providing 256 discrete memory addresses.

The array of exclusive NOR gates, U20 and U22, are open-collector types and their combined outputs go high, producing ϕLOCK B, when all its inputs are the same, high or low. ϕLOCK B occurs when U14-14 (Q0) is high and all stage outputs of U13 and U18 are high, except U13-14 (Q0), at counts 254 and 764. It also occurs when U13-14 is low and all stage outputs of U13 and U18 are low, except U13-14, at counts 509 and 1019. ϕLOCK B is an input to the optional multi-phase converter board and to counter U14. U14 is enabled through inverter U7-6 when ϕLOCK B goes high and is then clocked once simultaneously with U13 and U18 at clock pulses 255, 510, 765 and 1020. U13 and U18 are advanced one count, since their up/down inputs do not change state until after this clock pulse. The inputs to U20 and U22 are then no longer the same and ϕLOCK B goes high, disabling U14. However, U14 was clocked once, changing the state of its Q_0 output, pin 14, and the up/down inputs of U13 and U18. The count modes of U13 and U18 are then changed from up to down if pin 14 of U14 goes low or from down to up if it goes high. Thus U13 and U18 are forced to count up from count 001 to count 255, down from count 256 to 510, up from count 511 to 765 and down again from count 766 to 1020.

Counter U14-13 has its Q_1 output connected to FET Q7. The purpose of this connection is covered in a later paragraph. Its terminal count output, pin 15, goes low every 4060 counts to provide ϕLOCK A which is an input to the optional multi-phase converter board covered in paragraph 3.2.2.

3.3.1.5 QUASI-SINUSOID GENERATION

The digital-to-analog converter (D/A converter), U21, and the two amplifiers of U15 generate a quasi-sinsoidal waveform, consisting of 1020 discrete steps, in response to the inputs from programmable memories (PROM's), U17 and U19. The DC input for the D/A converter is provided by the 10 volt regulator, U10, and is adjusted for output level by R29 which is the front panel amplitude control.

The PROM outputs provide the digital input codes for the D/A converter. From the previous paragraphs, it should be apparent that the address for the PROM'S is being repeatedly incremented from 000 to 255 and then decremented from 255 back to 000. Thus, the digital input codes to the D/A converter are, likewise, being incremented and decremented. The PROM's are programmed so that, as their addresses are incremented from 000 to 255, their outputs cause U21 to produce what comprises the first 90 degrees of a quasi-sinusoidal waveform consisting of 255 discrete steps. The amplitude of each step is equivalent to:

$$\sin (90/255 \times A)$$

Where A is the discrete digital address (000 to 255).

As the address is decremented from 255 back to 000, U21 produces the opposite waveform which is the

second 90 degrees (91 to 180 degrees) of a quasi-sinusoidal waveform. The process of address incrementing and decrementing is repetitive. Therefore, in two complete cycles, U21 produces what appears as a sinusoidal waveform after full wave rectification except that it consists of 1020 discrete steps rather than being a pure analog signal. It is only necessary to invert alternate cycles of U21's output to achieve a quasi-sinusoidal waveform. This is accomplished in the amplifiers of U15.

FET Q7 grounds the connection between R27 and pin 3 of U15 whenever its gate is at +5 volts, changing the two sections of U15 from an inverting amplifier to a non-inverting amplifier. In a previous paragraph, it was stated that counter U14 was clocked once at counts 255, 510, 765 and 1020. Its Q_1 output, pin 13, therefore, will change state at counts 510 and 1020. Pin 13 of U14 is connected to the gate of FET Q7. Whenever it is low, Q7 is turned off and U15 inverts the output of U21. When it is high, Q7 is turned on and U21's output is not inverted. A complete cycle for U21 occurs between counts 000 and 510 and between 510 and 1020. Thus, alternate cycles will be inverted to form a quasi-sinusoidal waveform at the output of U15. R25 provides a means of equalizing the amplification of U15 in its inverting and non-inverting modes so that the alternate half-cycles of the quasi-sinusoidal waveform are equal in amplitude. The output of U15 is then integrated in U16-1 to provide a ΦA OUTPUT which is a sinusoidal waveform with very low distortion. The signal at pin 3 of U16 is sinusoidal and is passed through U16-7, which has unity gain, to provide the ΦA output of the oscillator.

3.3.1.6 FREQUENCY LIMITER

The purpose of the frequency limiter is to prevent production of an output frequency above or below the range of the AC power source that is driven by the 850T. Its circuit is shown in Figure 6-4 and is comprised of transistors Q1 and Q2, dual timer U6, dual flip flop U5, NAND gate U8-6 and associated components. The Q_1 output of counter U14 (pin 14) transitions from high to low once for every half-cycle of the output frequency. This pulse clocks both sections of U5, momentarily turns on Q1 and Q2 to discharge timing capacitors C1 and C2 and triggers both timers of U6. The section of U6 associated with Q2 is adjusted with R6 so that its time period is greater than one half-cycle of the lowest permissible output frequency. As long as the output frequency of the 850T is greater than this low limit, the output of the timer will be high when the next trigger pulse from U14 occurs. The Q output of flip flop U5-5 will not change state and the input of U8-6, connected to it, will remain high. The section of U6 associated with Q1 is adjusted with R1 so that its time period is less than one half-cycle of the highest permissable output frequency. As long as the output frequency of the 850T is less than this high limit, the output of the timer will have transitioned from high to low before the next pulse from U14 occurs. The Q output of U5-8 and the input to U8-5 connected to it will remain high.

While the frequency remains within the set limits, the output of U8-6 will be low (all its inputs are high) and Q6 will be turned off and Q8 will be turned on, completing the path from the +15 volt input to 10 volt regulator U10 which provides the DC input to D/A converter U21. If the selected frequency is below the set limit, pin 2 of U6 will go low before the next pulse. The Q output of U5-5 will be clocked low, the output of U8-6 will go high turning on Q6, turning on the LIMIT LED, CR5, turning off Q8, the DC supply to U10 and the D/A converter. If the selected frequency is higher than the set limit, pin 9 of U6 will be high at the time of the next pulse and the Q output of U5-9 will be clocked low, the output of U8-6 will go high turning on Q6, turning off Q8, the DC supply to U10 and the D/A converter.

A "soft start" feature is incorporated in the frequency limiter circuit that gradually increases the voltage applied to U10 when the unit is first started and whenever it returns to operation after shutting down because of an out-of-limit frequency condition. Q6 will be turned on when power is applied or when an out-of-limit frequency is selected. When it is turned off, R20 and C15 will delay the application of full forward bias to the base of Q8. Thus, the voltage applied to U10 will slowly increase from zero to +15 volts and the output of the D/A converter will, likewise, slowly increase.

3.3.1.7 POWER SUPPLIES

The +15 volt and −15 volt supplies are obtained by regulating the +25 and −25 volt supplies of the associated power source to those levels in the circuits of Q4 and Q5. The +5 volt supply is obtained from 115 volts AC through transformer T1, rectifiers CR3 and CR4 and +5 volt regulator U9.

3.3.2 MULTI-PHASE CONVERTER

The multi-phase converter is located on a separate, optional circuit board and the circuits of that board are shown in Figure 6-4. The multi-phase converter generates a phase C (ΦC) output from the ΦA input

which is then combined with the ϕA input to produce the ϕB output. A vector diagram showing the angular displacement of each phase with respect to the others is shown in Figure 3-3. The following paragraphs explain the functioning of the multi-phase converter.

3.3.2.1 PHASE C GENERATOR

The phase C generator consists of address counters, a directional control counter system, PROM's, a D/A converter and an inverting/non-inverting amplifier that perform the same functions as those on the ϕA generator board which were decribed in previous paragraphs. The circuits, comprised of counters U1, U2 and U3, exclusive NOR gates U7 and U8, PROM's U4 and U5, D/A converter U9 and operational amplifier U10 are interconnected in the same manner as their counterparts on the ϕA generator board. The counters are clocked by the same signal from A1U8-8 or A1U11. The DC input for the D/A converter is obtained from amplfier A1U12-6 which has its output level adjusted by the front panel amplitude control. Thus the amplitudes of the ϕA and ϕC outputs will be identical. R15 provides a fine adjustment of the ϕC amplitude.

The counters of the multi-phase converter, unlike those of the ϕA generator, are preset at the instant the ϕA output passes through the 180° point on every fourth cycle. The preset causes the waveform generated in this system to be displaced, relative to ϕA such that it lags ϕA by 120 degrees. The preset is accomplished by $\overline{\phi\text{LOCK A}}$ and ϕLOCK B through U6-8 and U6-11. $\overline{\phi\text{LOCK A}}$ goes low one clock pulse prior to the end of every fourth cycle of the output frequency (4078 clock pulses from the output of A1U8-8 or A1U11) and remains low for the next complete cycle. ϕLOCK B, as described in preceding paragraphs, goes high at counts 254, 509, 764 and 1019. Therefore, it goes high at counts 2039, 3059 and 4079. When $\overline{\phi\text{LOCK A}}$ is low and ϕLOCK B goes high, the preset mode of counters U1, U2 and U3 are enabled and preset occurs on the rising edge of the next clock pulse. The counters are preset to the count determined by the connections to their A, B, C and D inputs. S1 is not normally installed and the dotted lines across its sections 2 and 4 represent clad jumpers on the circuit board. As drawn, the A and C inputs of U1 and U2 are grounded (low) and the B and D inputs are at +5 volts. This produces a preset of AA in hexidecimal or 1010 1010 in binary. This presets the PROM address at 170. The directional control counter, U3, is preset so that its Q_A output is low and its Q_B output is high. Thus, counters U1 and U2 will be in the count down mode and U10 will be in its inverting mode. The amplitude of the waveform developed at the output of U9 from this point forward will be decreasing from maximum and, since U10 is in an inverting mode, the output of U10 will be 120° leading ϕA which is the correct phase angle for ϕC. The signal output of U10 is buffered by U12-7 to provide ϕC OUTPUT at pin 14 of J1. Capacitor C8 provides high frequency roll-off for U12-7.

3.3.2.2 B PHASE GENERATOR

The ϕB signal is obtained by summing ϕA and ϕC signals of equal amplitudes and then inverting the resultant signal through an operational amplifier. The ϕA OUTPUT signal input to this board is obtained from amplifier A1U16 which isolates it from the ϕA OUTPUT signal to the power source which is obtained at the output of A1U16-7. The ϕC signal is obtained from the output of amplifier U12-1. The two signals are summed at the input of amplifier U11-1 through the resistor network of R11 and the two sections of R3. R11 provides a fine adjustment of the ϕB angle and R7 provides a fine adjustment of the ϕB amplitude. The ϕB is buffered in U11-7 to produce ϕB OUTPUT at pin 13 of J1.

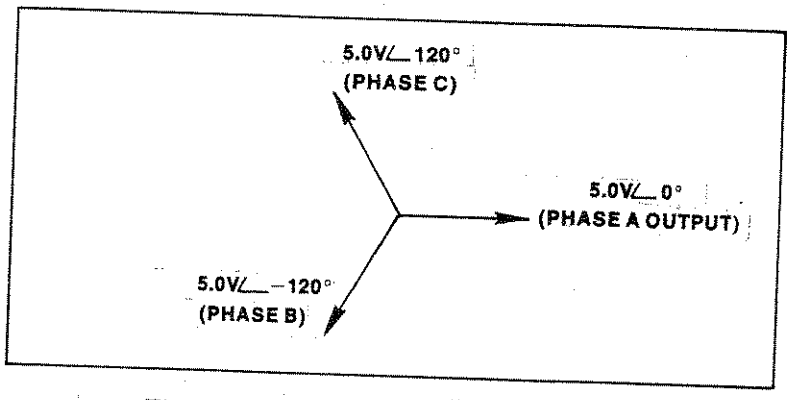


Figure 3-3. Three Phase Vector Diagram.

SECTION IV
ADJUSTMENT PROCEDURES

4.1 GENERAL

The following adjustment procedure, or any part of it, may be performed on a routine basis to insure that the oscillator remains within the specified performance limits. The procedure should always be performed after service to the oscillator.

The procedure outlines calibration of the main board (A1) which controls output frequency and phase A (ϕA) distortion, and of the Phase Board (A2) which controls the phase B (ϕB) and phase C (ϕC) amplitude and distortion.

Calibration of either the 850T or 855T Series Oscillators requires a test fixture or compatible power sources as shown in Figure 4-1. An extender accessory, Part No. 4800-703, may be used if the oscillator is to be calibrated while connected to an Invertron® power source.

4.2 PROCEDURE

4.2.1 SINGLE PHASE MODELS

4.2.1.1 DISTORTION

Connect a distortion analyzer between pin 2 and pin 8 (ground) of connector J2. If the oscillator is connected to the power source, the output of the power source may be monitored with the distortion analyzer. Adjust the front panel AMPLITUDE control to produce 5 volts RMS at the output of the oscillator, pin 2 of J2, or for full scale output of the power source. Adjust potentiometer A1R25, on the main board, for indication of lowest distortion content.

Reduce the front panel AMPLITUDE control to produce 1 volt RMS at the oscillator phase A output. Adjust A1R24 for the lowest distortion level.

CAUTION

Voltages up to 500 Volts AC are available in certain associated Invertrons®. This equipment generates potentially lethal voltages.

DEATH

on contact may result if personnel fail to observe safety precautions. Do not touch electronic circuits when power is applied. Avoid contact with connector pins C and D of the plug-in oscillator, the primary power circuits and output circuits of the associated Invertron® if oscillator is tested and/or adjusted with Invertron®.

4.2.2 TWO-PHASE MODELS

The distortion adjustment must be made prior to the

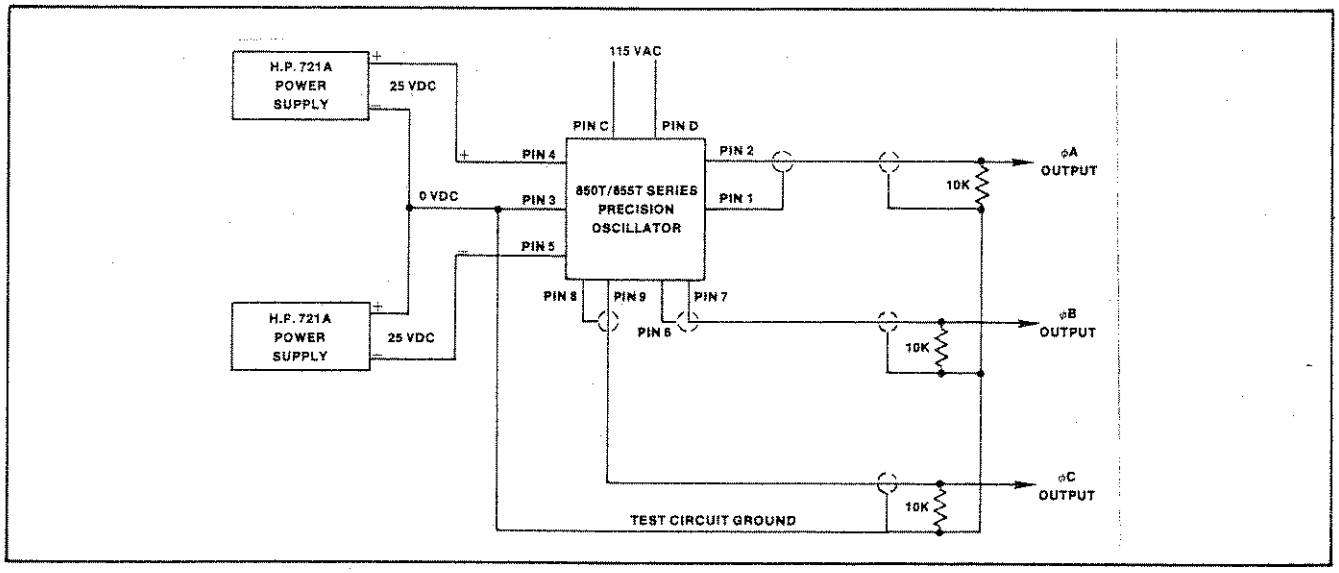


Figure 4-1. Test Circuit for 850T/855T Series Oscillators.

LEVEL adjustment of 4.2.2.2 because of interaction of the adjustments.

4.2.2.1 DISTORTION

A. Connect a distortion analyzer between pin 2 and pin 8 (ground) of connector J2. If the oscillator is connected to the power source, the ϕA output of the power source may be monitored with the distortion analyzer. Adjust the front panel AMPLITUDE control to produce 5 volts RMS at the output of the oscillator, pin 2 of J2, or for full scale output of the power source. Adjust potentiometer A1R25, on the main board, for indication of lowest distortion content.

B. Connect the distortion analyzer between pin 9 and pin 8 (ground) of connector J2. If the oscillator is connected to the power source, the ϕC output of the power source may be monitored with the distortion analyzer. Adjust potentiometer A2R14, on the phase board for an indication of lowest distortion content in the ϕC output.

Reduce the front panel AMPLITUDE control to produce 1 volt RMS at the oscillator phase C output. Adjust A2R13 for the lowest distortion level.

4.2.2.2 AMPLITUDE ADJUSTMENT

Connect an AC digital multimeter between pins 2 an 8 of J2 (A). Adjust the front panel amplitude control for 5.00 volts RMS. Connect the AC digital multimeter between pin 9 and pin 8 of J2. Adjust A2R15 for 5.00 ± 0.05 volts.

4.2.3 THREE-PHASE MODELS

There is some interaction in the following adjustments. For the correct alignment of the three-phase oscillators, the following adjustments must be made in the order shown:

A. Adjust the ϕA and ϕC distortion as directed in 4.2.2.1.

B. Adjust the level of ϕC relative to ϕA.

C. Adjust the phase angle of the ϕB output.

D. Adjust the amplitude of ϕB relative to ϕA.

4.2.3.1 DISTORTION

Perform the tests outlined in paragraphs 4.2.2.1 and 4.2.2.2.

4.2.3.2 PHASE ADJUSTMENT

A. Connect the differential phase meter between pins 2 (A), 7 (B) and ground. Adjust the frequency of variable frequency models (850T) to 100 Hz, or less. Adjust potentiometer A2R11 on the Phase Board (A2) for a phase meter indication of A leading B by 120 degrees.

4.2.3.3 AMPLITUDE ADJUSTMENT

A. Monitor the ϕA output of the oscillator with an AC digital multimeter connected between pins 2 and 8 (ground) of connector J2. Adjust the front panel AMPLITUDE control for a 5.0 volts RMS reading.

B. Connect the digital multimeter to pin 7 of connector J2. Adjust potentiometer A2R7 on the Phase Board for a 5.0 volts RMS reading.

4.2.4 FREQUENCY LIMIT ADJUSTMENT

The frequency limiter prevents the 850T/855T Series Oscillators from driving the associated power source with a frequency that is outside the power source operating limits. If the dials of the 850T are set at a frequency outside those limits, or if the frequency determining circuits should malfunction, the output of the oscillator will be shut off and a red LIMIT indicator on the front panel will light. The LIMIT indicator will be extinguished and the output will be turned back on when the dials are set to a frequency within the power source limits. The limiter is also a feature of the 855T and safeguards against a malfunction of the frequency determining circuits. The standard adjustment permits oscillator operation between the limits of 45 Hz and 5000 Hz. If a wide-band power source is to be driven by either oscillator, the limits may be readjusted.

4.2.4.1 850T ADJUSTMENT

To adjust the upper frequency limit, set the RANGE switch to X100 and select the highest frequency desired. Adjust potentiometer A1R1 on the main board (A1) to the point where the LIMIT indicator is illuminated then back off on the adjustment slightly. Select a frequency higher than the set limit and verify LIMIT indicator illumination. Similarly, set the lower limit frequency and adjust A1R6 for LIMIT indicator illumination then back off on that adjustment slightly. Select a frequency lower than the set limit and verify LIMIT indicator illumination. When adjusting the limit potentiometers, note that some hysteresis exists in the adjustments. This prevents amplitude chatter when programming frequencies around the frequency limits.

4.2.4.2 855T ADJUSTMENT

The adjustment for the 855T is accomplished in the same manner as that for the 850T described in 4.2.4.1 except that the upper and lower limits must be set with the DIP switches mounted on the main board (A1). Figure 4-2 shows the location of the DIP switches. Table 4-1 lists the switch closures necessary to program 45, 60, 400 and 5000 Hz. If it is desired to program other frequencies, contact California Instruments' Customer Service Department for assistance.

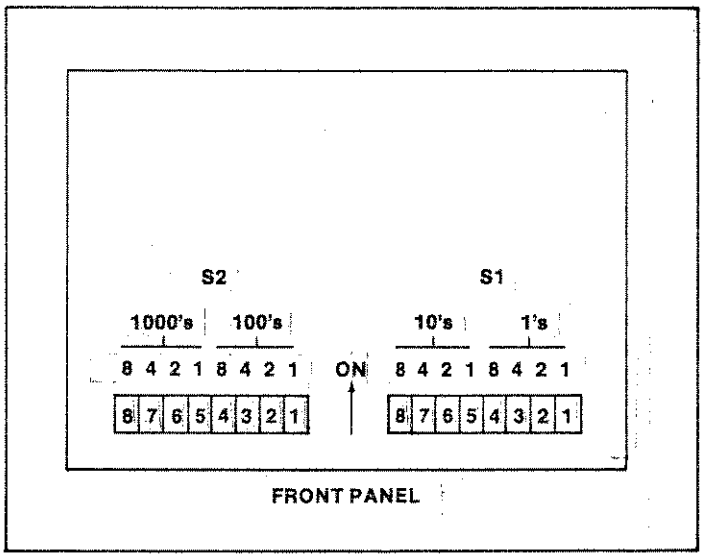


Figure 4-2. Location of Frequency Programming DIP Switches, Model 855T.

Table 4-1. Model 855T Frequency Programming.

	S2		S1	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1
45 Hz	X X X X	X X X X	X - X X	X - X -
60 Hz	X X X X	X X X X	X - - X	X X X X
400 Hz	X X X X	X - X X	X X X X	X X X X
5000 Hz	X - X -	X X X X	X X X X	X X X X

- = OFF
X = ON

SECTION V—MAINTENANCE

5.1 GENERAL

This section of the manual contains information to assist in troubleshooting the Models 850T and 855T Precision Oscillators. A table of power supply voltages and "logic tree" types of troubleshooting charts are included. A review of the Theory of Operation in Section III is recommended prior to attempting to troubleshoot either unit. The technician will then have a good understanding of the circuit operation which will further assist in the troubleshooting task.

5.2 REQUIRED TEST EQUIPMENT

The test equipment required to perform the tests outlined in this section is listed in Table 5-1.

Table 5-1. Required Test Equipment.

California Instruments Model DMM-53 Digital Multimeter.
Frequency Counter with 20 MHz capability.
Calibrated Oscilloscope with 20 MHz, or better, response.

5.3.1 POWER SUPPLY TEST

Reduce the output of the oscillator to zero and measure the +15 volt, −15 volt and +5 volt supply lines. Verify that they are within the limits shown in Table 5-2.

If the power supply voltages are within limits, proceed to the next paragraph. If they are not, troubleshoot and repair the defective power supply.

5.3.2 CLOCK GENERATOR TEST

Check the clock generator signal with the oscilloscope at A1U13, pin 2. The clock signal should be a square wave with an amplitude of 3 volts, or more, peak-to-peak. If there is no clock signal, refer to the clock generator troubleshooting chart of Figure 5-1. If the clock signal is present, but the oscillator output is absent or severely distorted, refer to the waveform synthesizer troubleshooting chart of Figure 5-2.

Table 5-2. Power Supply Voltage Limits.

LINE	TEST POINT	LIMITS
+15V	TP3	+14.6 to +16.2 VDC
−15V	TP2	−14.6 to −16.2 VDC
+5V		+4.75 to +5.25 VDC

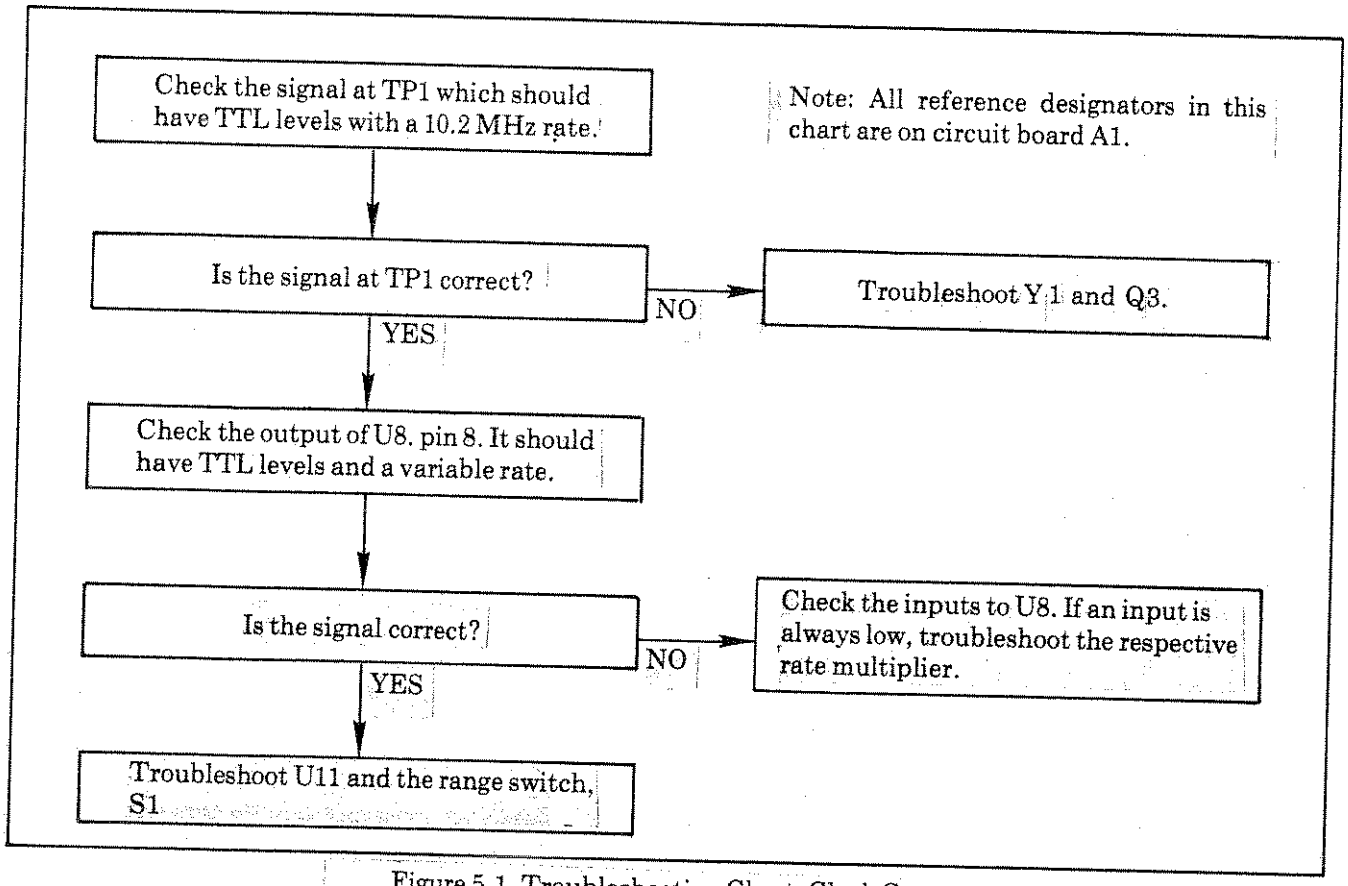


Figure 5-1. Troubleshooting Chart, Clock Generator.

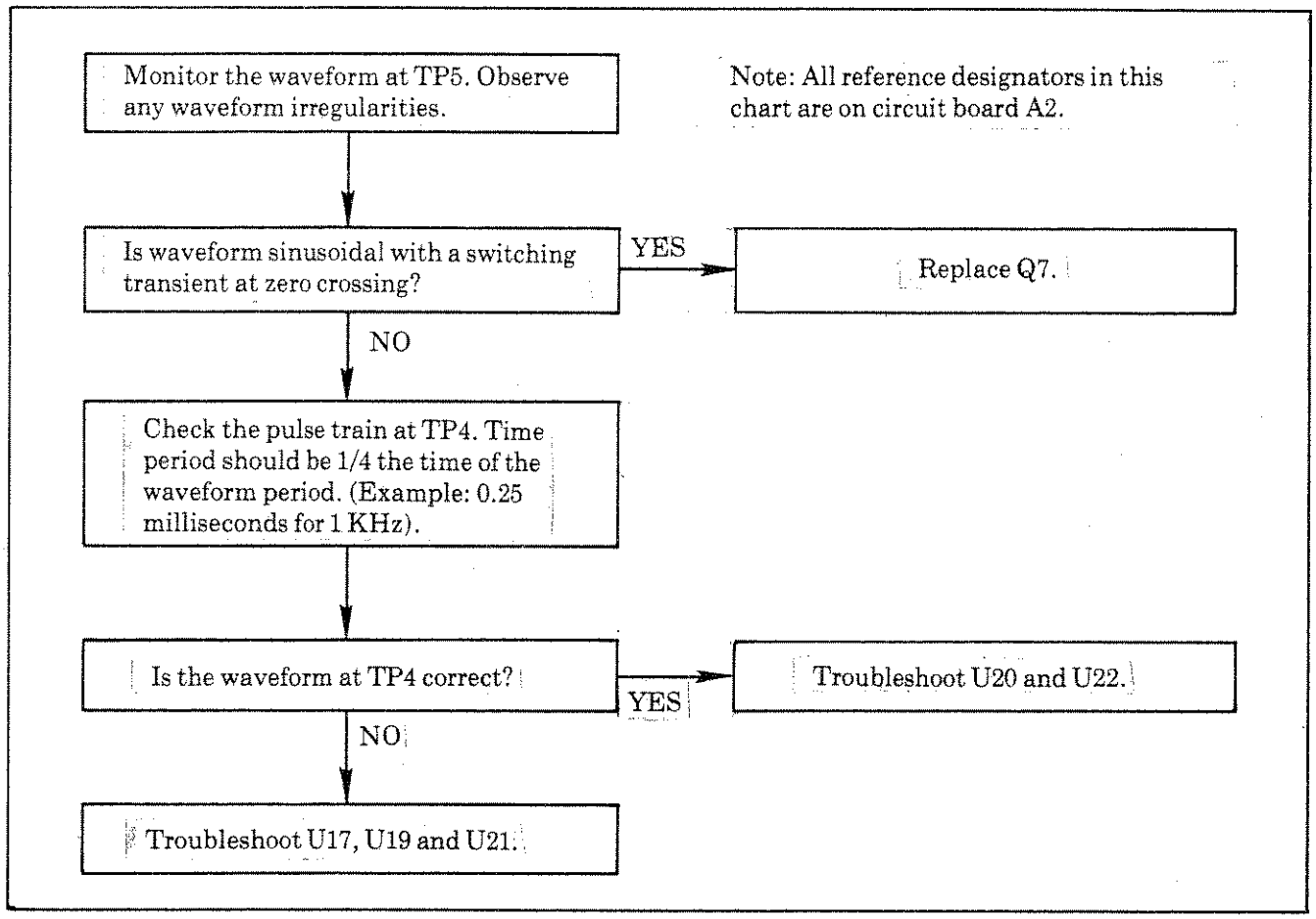


Figure 5-2. Troubleshooting Chart, Waveform Synthesizer.

SECTION VI—DIAGRAMS

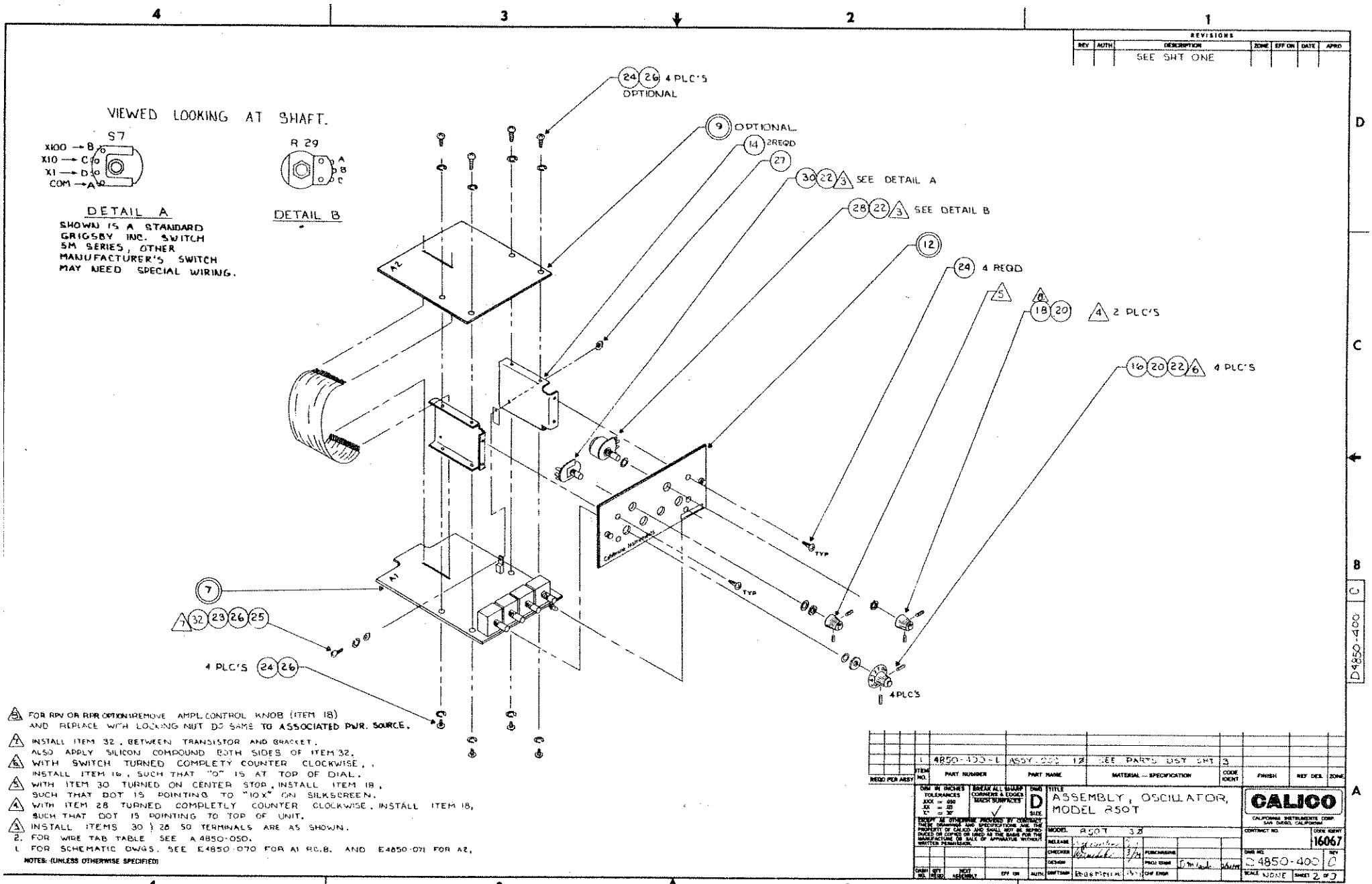
6.1 GENERAL

This section of the manual contains schematic and mechanical diagrams necessary for the operation and maintenance of the 850T/855T Series Precision Oscillators. The schematic diagrams illustrate the circuits while the mechanical assembly drawings indicate the component locations.

6-3 REFERENCE DESIGNATIONS

6-4 Partial reference designators are shown on schematic and mechanical drawings. Prefix these reference designators with assembly and/or sub-assembly designation for the complete reference designator. For example:

Assembly/Sub-Assembly	Component	Component Designation
None	T1	T1
A1	IC6	A1IC6
A2	R44	A2R44
A3	C7	A3C7
A4	Q2	A4Q2



REVISIONS

REV	AUTH	DESCRIPTION	ZONE	EFF ON	DATE	APRD
		SEE SHT ONE				

ITEM NO.	PART NUMBER	PART NAME	MATERIAL — SPECIFICATION	CODE IDENT	FINISH	REF DES	ZONE
REQD PER ASSY							
1	4850-400-L	ASSY, OSC	1#	SEE PARTS LIST SHT	3		

DIM IN INCHES
TOLERANCES
XXX = .000
XX = .00
X = .0
ANGLES = 30'

BREAK ALL SHARP CORNERS & EDGES MAXIMUM RADIUS .005

SIZE D

TITLE ASSEMBLY, OSCILLATOR, MODEL 250T

MODEL 250T 3#

CALICO
CALIFORNIA INSTRUMENTS CORP
SAN DIEGO, CALIFORNIA

CONTRACT NO. 16067

DWG NO. C 4850-400 REV C

SCALE NONE SHEET 2 OF 3

DRAWN | CHECKED | DESIGN | RELEASE | PROJ ENGR | PURCHASING | DRFTSMN

DWG NO. | REVISIONS | EFF ON | AUTH

NEXT ASSEMBLY

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NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FOR SCHEMATIC DWGS. SEE E4850-070 FOR A1 P.C.B. AND E4850-071 FOR A2.
2. FOR WIRE TAB TABLE SEE A 4850-050.
3. INSTALL ITEMS 30 & 28 SO TERMINALS ARE AS SHOWN.
4. WITH ITEM 28 TURNED COMPLETELY COUNTER CLOCKWISE, INSTALL ITEM 18, SUCH THAT DOT IS POINTING TO TOP OF UNIT.
5. WITH ITEM 30 TURNED ON CENTER STOP, INSTALL ITEM 18, SUCH THAT DOT IS POINTING TO "10X" ON SILKSCREEN.
6. WITH SWITCH TURNED COMPLETLY COUNTER CLOCKWISE, INSTALL ITEM 16, SUCH THAT "0" IS AT TOP OF DIAL.
7. INSTALL ITEM 32, BETWEEN TRANSISTOR AND BRACKET. ALSO APPLY SILICON COMPOUND BOTH SIDES OF ITEM 32.
8. FOR RPV OR RPR OPTION: REMOVE AMPL CONTROL KNOB (ITEM 18) AND REPLACE WITH LOCKING NUT DO SAME TO ASSOCIATED PWR. SOURCE.

D4850-400

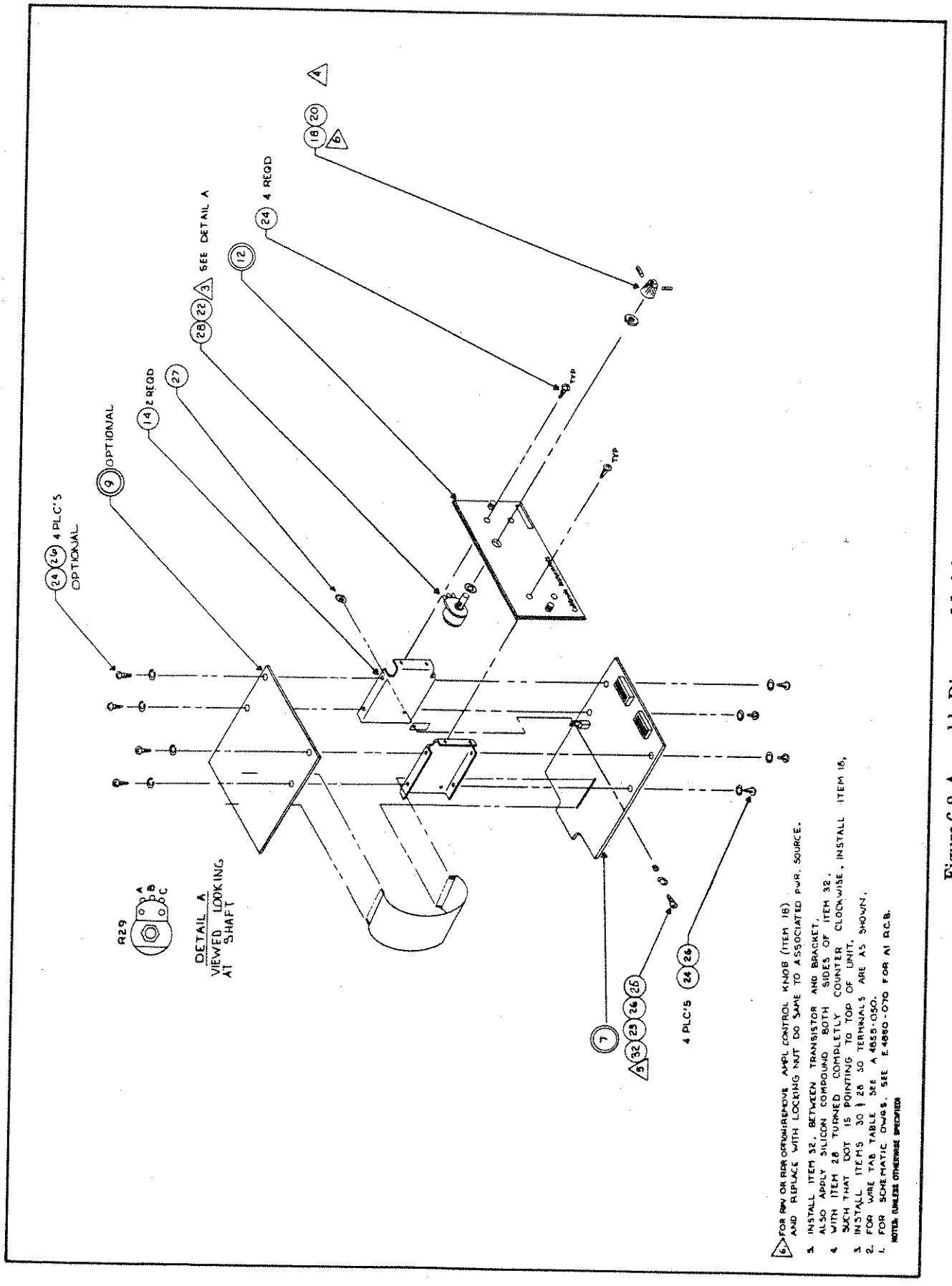

Figure 6-2. Assembly Diagram, Model 855T Oscillator.