

**SERVICE MANUAL**  
for  
**PLUG-IN PROGRAMMER**  
**MODEL PIP 9012**

**THIS SERVICE MANUAL IS INCOMPLETE WITHOUT THE PIP 9012 OPERATING MANUAL WHICH CONTAINS A DESCRIPTION OF THE SYSTEM, INSTALLATION INSTRUCTIONS, AND OPERATING INSTRUCTIONS.**

**THIS SERVICE MANUAL CONTAINS THE THEORY OF OPERATION, MAINTENANCE INSTRUCTIONS, PARTS LISTS, SCHEMATICS, AND ASSEMBLY DRAWINGS.**

**ELGAR CORPORATION**  
9250 Brown Deer Road  
San Diego, CA 92121

**PLUG-IN PROGRAMMER**  
PIP 9012 - Service

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**ELGAR**

9250 Brown Deer Road

San Diego, California 92121

619/450-0085 • 800/733-5427

FAX: 619/458-0267 • TELEX: 211063 ELSU UR

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# SAFETY NOTICE

BEFORE APPLYING POWER to the System, verify that the PIP 9012 is properly configured for the user's particular application.

## WARNING

HAZARDOUS VOLTAGES IN EXCESS OF 230 VRMS, 400V PEAK MAY BE PRESENT WHEN COVERS ARE REMOVED. QUALIFIED PERSONNEL MUST USE EXTREME CAUTION WHEN SERVICING THIS EQUIPMENT. CIRCUIT BOARDS, TEST POINTS AND OUTPUT VOLTAGES MAY ALSO BE FLOATING ABOVE (BELOW) CHASSIS GROUND.

Installation and servicing must be performed by QUALIFIED PERSONNEL who are aware of properly dealing with attendant hazards. This includes such simple tasks as fuse verification and channel reconfiguration.

Ensure that the AC power line ground is properly connected to the PIP 9012 input connector. Similarly, other power ground lines including those to application and maintenance equipment **MUST** be properly grounded for both personnel and equipment safety.

Always ensure that facility AC input power is de-energized prior to connecting or disconnecting the power cable. Similarly, the PIP 9012 circuit breaker must be switched OFF prior to connecting or disconnecting output power.

In normal operation, the operator does not have access to hazardous voltages within the chassis. However, depending on the user's application configuration, **HIGH VOLTAGES HAZARDOUS TO HUMAN SAFETY** may be normally generated on the output terminals. The Customer/User must ensure that the output power (and sense) lines be properly labeled as to the SAFETY hazards and any that inadvertent contact with hazardous voltages is eliminated.

Guard against risks of electrical shock during open cover checks by **NOT TOUCHING** any portion of the electrical circuits. Even when power is OFF, capacitors are well known to retain an electrical charge. Use **SAFETY GLASSES** during open cover checks to avoid personal injury by any sudden component failure.

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# **SECTION I**

## **THEORY OF OPERATION**

## 1.1 INTRODUCTION

The Elgar Model PIP 9012 Plug-In Programmer (PIP) is a subsystem specifically designed to be used with its companion Elgar AC Power Source. The AC Power Source is not discussed in any depth in this manual; refer to the appropriate Elgar AC Power Source manual for detailed information. Ideally, both this PIP manual and the companion AC Power Source manual should be reviewed simultaneously for a complete understanding of signals and the theory of operation.

Topics within this section provide a sound basis for understanding the role performed by the electronics in the instrument and should be a precursor to any troubleshooting or maintenance. It is also recommended that the user frequently refer to the board schematics contained in Section IV of this manual.

Topics of this section are well advanced over normal Operator/Programmer activities. Thus, the user should already be familiar with both analog and digital design, associated devices and terminology. Details of the inner workings of operational amplifiers, octal latches, DACs, etc., are in the individual device manufacturer's data books. In the text, a signal name immediately followed by a slash (/) indicates negative logic (low true or active at logic zero).

The topics in this section are arranged to present a top level view of internal intelligent digital and analog functions within the PIP 9012. These functions consist of internal firmware routines and logic combinations, analog

circuitry, and hybrids of these technologies, in order to interactively perform instrument tasks. An understanding of both top level and circuit level activities is most valuable should it be necessary to investigate suspected faults within the instrument.

## 1.2 SYSTEM OVERVIEW

Figure 1-1 displays the PIP 9012 functional relationships. Most notable is the Microprocessor Board that participates in virtually every function. The Microprocessor Board not only initializes the instrument to a safe state, but continuously runs its own firmware program to:

- Accept inputs (either keyboard or remote via the GPIB);
- Error check input setups;
- Flag discrepancies;
- Direct setups to the desired channel(s); and,
- Control precise timing of events.

### 1.2.1 System Monitoring

While developing AC power for one or more AC channel(s), the Microprocessor Board continuously monitors samples of voltage and current to flag run time errors should any faults occur.

The Microprocessor Board determines the exact nature of any flag and determines the course of action; even to a channel(s) protective shutdown.

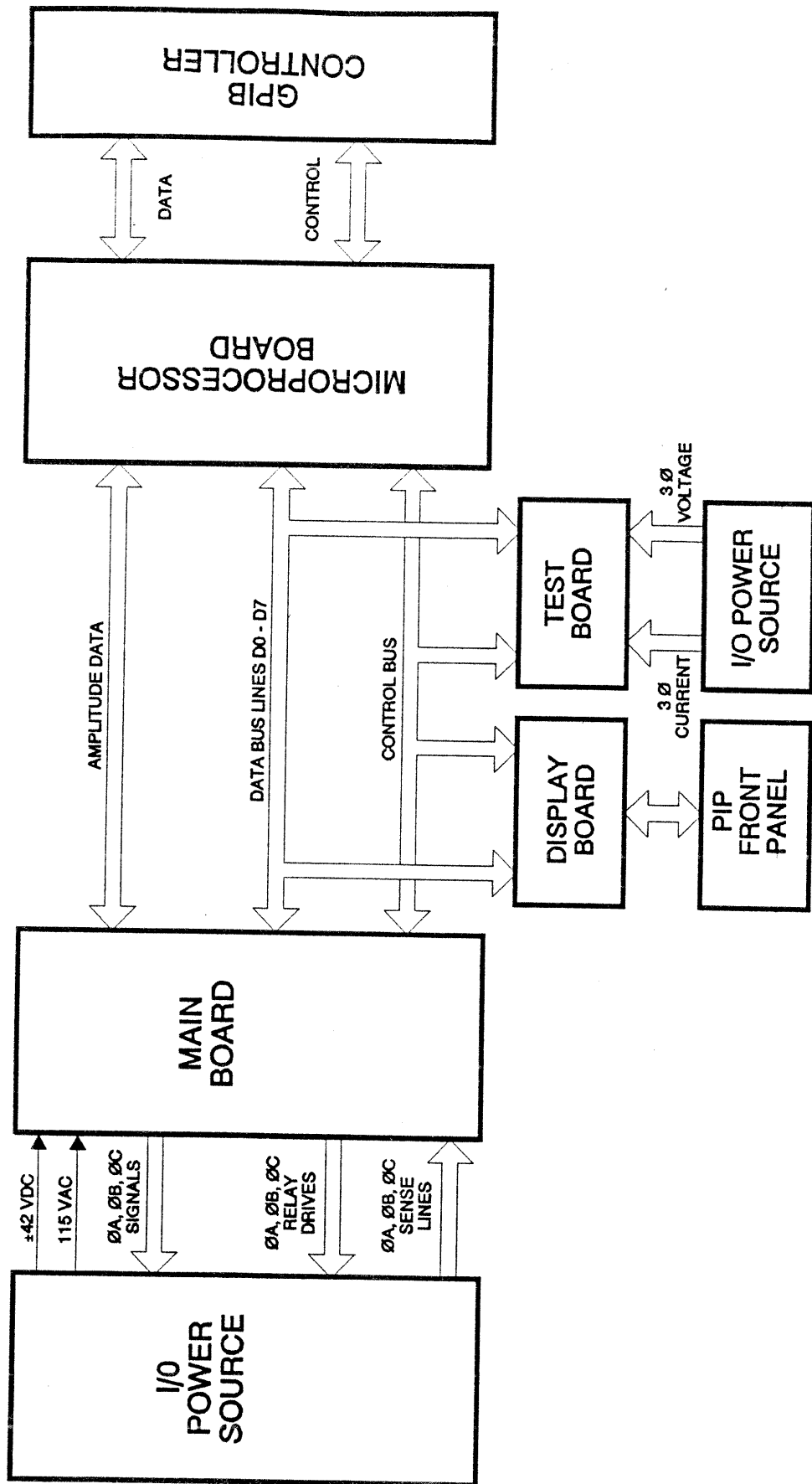


Figure 1-1. PIP 9012 Functional Diagram



Other channels in standby (output relay not connected to the load) undergo continuous checks to protect against otherwise unnoticed internal channel faults. The Test Board performs additional checks.

The display reports local and remote programming setup parameters for any specified channel and parameter. Any channel may also have its real time output voltage, current, frequency and power displayed (via the TST function).

### 1.2.2 System Operation

The PIP 9012 does not have an ON/OFF power switch; all power is derived via internal connections with its respective AC Power Source. The PIP performs several internal functions but also stimulates, controls, and interacts with its respective AC Power Source.

Upon a cold start, the AC Power Source output relays are open. Thus, any short term power up abnormalities within the PIP and AC Power Source are not seen by the external load. The Microprocessor Board initiates its own microprocessor and the GPIB interface. The initialization routine then performs several activities to identify its own contents and ensures readiness for operation. The GPIB address switch (S1-S5) is read to identify the instrument bus (GPIB) address. The initialization routine then forces all output relays to remain open and programs all channels to power up defaults (these are the same defaults as the GPIB device clear, SDC or DCL).

The entire process of cold start requires less than one second, at which time the instrument is ready for normal use. The Microprocessor Board initialization routine is completed and then exited to its idle routine. Here, the Microprocessor Board continuously scans for inputs from the GPIB, from the keyboard, and from the fault detection circuits. This idle scanning continues until AC power is removed from the instrument.

Periodically, the idle loop is momentarily interrupted from its substantial monitoring function. Activities such as confidence test, regular test (monitoring), GPIB, keyboard inputs, display updates, etc., enter and exit the routine of the idle loop.

The Microprocessor Board digitally controls the many activities of the other circuit card assemblies of the PIP 9012, as displayed in Figure 1-1. The Display Board provides local control input and output (keyboard and display) for the Microprocessor Board. The Test Board converts AC Power Source analog voltages and currents into digital measurement signals for the Microprocessor Board. The Main Board actually generates the analog frequency and amplitude low level drive signals for the AC Power Source while the Microprocessor Board directs the Main Board via its digital signals.

When power is applied to the PIP 9012, the microprocessor is cleared and, in turn, clears all registers to zero except the frequency storage register (the frequency is initialized at 400 Hz).

The storage frequency information is converted to a continuous string of pulses which is 1024 times the output frequency. This string of frequency pulses is counted down by 1024 and this drives a PROM which has a sine look-up table as its program. The sine look-up table drives a Digital-to-Analog Converter (DAC) which produces a sine wave output. This output is filtered and becomes the oscillator output signal.

The stored amplitude information is converted to a DC programming voltage by a 12-bit binary DAC which controls the output servo feedback system and, in turn, the output amplitude.

In the test mode, the sense voltage and the output from a wide band current transformer is taken to the Test Board where the measurements are made.

### 1.3 INTERCONNECT

The PIP 9012 consists of a mechanical assembly with printed circuit cards and an interconnecting ribbon cable. Connections from card-to-card are via this interconnect cable. The choice of a ribbon cable allows the service and calibration technicians easy access to the circuit cards. Except for the bottom card (Main Board), each circuit card is hinge-mounted to allow access to the other card(s) below.

The Main Board edge connector makes most of the electrical connections between the PIP (J1) and the AC Power Source. The AC Power Source routes some of these signals directly to connectors on the rear panel. Voltage sense signals may be internal or external and, thus, are routed through

the AC Power Source relay drive switches. The balance of these signals are used within the AC Power Source.

The Test Board connector provides access to the same voltage sense leads as those directed to the Main Board. The Test Board measures and reports this voltage (the Main Board amplitude regulates using voltage sense). The J2 connector has a separate ribbon cable connected directly to the AC Power Source.

Local programming is via the PIP 9012 keyboard and display. No external interconnects are involved for entry or display.

Remote programming is exclusively via the GPIB. The GPIB connector on the rear of the AC Power Source connects via a ribbon cable to the Micro-processor Board. This special interconnect minimizes stray coupling between the fast digital GPIB signals and the relatively slow undistorted analog signals of the AC Power Source. Also, the GPIB is moderately sensitive to all unnecessary cabling abnormalities.

For proper PIP 9012 operation, the external voltage sense leads on the rear of the AC Power Source must be connected to the output voltage terminals. Preferably, this is performed at the load end of the output cable. This enables the PIP 9012 motherboard to correct for any output cable voltage drops. If no (or improper) voltage sense lead connections are made, the PIP 'thinks' the output voltage is radically incorrect, interprets this as a fault condition (Open Servo), and shuts down the channel(s).

**1.4 MICROPROCESSOR BOARD**

(Refer to Schematic No. 6809912 and Assembly Drawing No. 5809912.)

The Microprocessor Board plugs into the PIP assembly as the topmost Circuit Card Assembly (CCA).

The Microprocessor Board performs intelligent functions for the PIP 9012 and AC Power Source. These functions are called "intelligent" because its microprocessor and associated firmware implement pre-programmed internal routines such as the idle loop described above.

The Microprocessor Board communicates with all internal PIP boards, including the keyboard/display for local control. Remote control (GPIB) is processed exclusively within this CCA. The Microprocessor Board has no direct connections with the AC Power Source, but implements control and measurement via communications with other boards within the PIP.

There is one five-bit DIP switch and three wire jumpers on the Microprocessor Board which must be set before power up. These are read during the power up routine and identify the environment to the microprocessor. The locations of the GPIB address switch (S1) and measurement power range jumpers are identified on the Microprocessor Board Assembly Drawing No. 5809912 (the S1 settings are identified in Section II of the PIP 9012 Operating Manual). S1 is normally shipped from the factory at GPIB decimal address 17.

**1.5 MICROPROCESSOR THEORY OF OPERATION**

(Refer to Schematic No. 6809912.)

The Microprocessor Board's microprocessor chip and associated control logic initialize the PIP 9012 when power is first applied. Table 1-1 provides a listing of the initialization parameters.

**Table 1-1. PIP 9012 Initialization Parameters**

Parameter	Initial Value
Frequency	400 Hz
Amplitude (3 phases)	0V
Phase Angle A	0°
Phase Angle B	240°
Phase Angle C	120°
Amplitude Range	0-135V
Current Limit	0
Disconnect Relay	Open

When power is applied, C19 holds U17 pin 13 high for approximately 200 ms while pin 12 of U17 goes low for the same period. This low resets the microprocessor (U18) and the GPIB interface (U27), thus creating an orderly start-up sequence.

After the Power ON resets, the microprocessor (U18) initializes the latch conditions, presets the frequency to 400 Hz, and initializes the GPIB (U27).

The oscillator (consisting of U17 pins 1 to 4) is frequency controlled to 10.24 MHz by crystal Y1. This 10.24 MHz is the frequency input required by rate multipliers U1, U2, U5, and U6. This frequency is divided by 2 in U16, then the output at U16 pin 5 (5.12 MHz) is fed to the microprocessor (U18).

U28 receives data from the keyboard which is latched by STO K. This latching is required as the keyboard information is scanned rather than causing an interrupt. U16 pin 9 stores the information that a keyboard entry was made. When port B6 (pin 30) of the microprocessor goes low, U16 is reset and U28 is enabled. This allows the microprocessor to read the data and reset U16 to be ready for the next keyboard entry.

The display MUX is controlled by output port U22. The port is updated every 2 ms and produces BCD 1248 information and MUX 1 and MUX 2. MUX1 and MUX 2 determine which of the four displays is turned on to display the BCD data (the decimal line is set high when the appropriate display is on).

Output port U12 controls the frequency range, and the function LEDs of the display and SEL1 and SEL2 lines. SEL1 and SEL2 control the output data lines from the Test Board.

The output data lines from the Test Board share input port A of U18 with the keyboard input data. The same port A lines control the operation of the Test Board when they are used as output lines.

DAC U7 is a 12-bit device that programs the output voltage amplitude. This device has built in storage latches which are actuated by pin 17. CR1 is a 6.9V reference which is amplified to -10V at U7 pin 19. The negative output current of the DAC is converted to a voltage and inverted by U4 pins 1, 2, and 3. This voltage is proportional to the output voltage and should be  $2.0V \pm 5\%$  when the voltage is programmed to 100V output.

Latches U8 and U9 store the frequency data for rate multipliers U1, U2, U5, and U6. The rate multiplier is a unique device that produces a number of pulses set by the BCD input for every ten pulse input. They can output zero to nine clocks for every ten clocks in. During the tenth clock period the down cascade occurs. The outputs of the four rate multipliers are Nanded together at U3 pin 6 and the output of U3 pin 8 is always 1024 times the output frequency of the oscillator. This frequency produces 256 steps per quarter wave.

Memory Map Decoder U24 determines which memory device is active. U23 further breaks down when the PIP 9012 function latches are addressed.

Address latch U14 stores the 8 LSB address bits while U18 sends the MSB address bit direct via pins 15 through 19.

The main program memory is U19. U20 is an expansion memory used only for special applications.

U21 is the Random Access Memory (RAM) used for storage of the message strings prior to parsing them. GIA U27, in conjunction with bus transceivers U25 and U26, controls the actual transfer of data under overall control of the microprocessor via U18. Address switch S1 to S5 is accessed by the microprocessor via U11.

## 1.6 MAIN BOARD THEORY OF OPERATION

(Refer to Schematic No. 6809907.)

The rate clock, as generated by the rate multipliers, is present on pin 10 of U9 (a 12-bit binary counter). U9 uses the 8 LSD as counting bits and Q9 and Q10 as control bits. U9 is continuously counting up and, when the 8 LSD changes from 255 to 256, the Q9 line changes state (as do the 8 LSD bits). The results of this action are that the outputs of the exclusive OR gates are the same, but now the output is counting down.

The outputs of the exclusive OR gates are sent to sine PROM U18, which converts the linear stair steps to sine weighted stair steps. As the stair steps are up/down counting, DAC U17 outputs a sine weighted half-wave of current which is converted to voltage by U3 pins 5, 6, and 7.

Amplifier U2 pins 1, 2, and 3 (together with Q6) form an invert/non-invert circuit which inverts every other half wave and the result is a sine wave on its output.

Pin 14 of U9 is a square wave at the output frequency so, when it is high, it turns on enhancement mode FET Q6. When Q6 is on, the amplifier is an inverting amplifier and when off, is a non-inverting amplifier.

Amplifier U2 pins 5, 6, and 7 (and associated components) comprise an active filter which is cornered at 22.5 kHz. This allows the sine wave to pass, but the stair steps are filtered out.

Amplifier U7 pins 1, 2, and 3 is a variable gain amplifier with the gain controlled by the output of error amplifier U7 pins 5, 6, and 7. These pins have one input to the summing junction from the programming voltage (DAC OUT) from the Microprocessor Board. It also has a voltage which is proportional to the servo voltage fed back from the load. When these voltages are equal and opposite, the error integrator summing junction is satisfied and the error integrator will idle at approximately -2V. When the servo senses a drop in voltage due to increased load, the error integrator output will go more negative, increasing the current through the photo-diode of U1. When the diode becomes brighter, the resistance of the photo resistor will drop, thus increasing the gain of variable gain amplifier U7 pin 1, 2, and 3. The increased oscillator output will have then compensated for the increased load.

If the servo is opened or the associated AC Power Source is overloaded, the error integrator will swing to negative saturation. This is sensed by comparator U16 and causes the microprocessor to shut down the output of the oscillator. If the output of the associated AC Power Source goes to a voltage higher than that programmed, the other section of U16 will sense this and again the microprocessor will shut down the output.

The B and C phases are generated in much the same manner as the A phase except that the generation PROM is a cosine program instead of a sine program. The cosine is differentially mixed with the sine in U26 pins 5, 6, and 7 and the output is of equal amplitude but at  $240^\circ$ . The  $240^\circ$  is differentially mixed with the sine (at  $0^\circ$ ) and the difference is  $120^\circ$  at U20 pin 7. The servos and fault detection circuits for the B and C phases work in the same manner as those of the A phase.

### 1.7 DISPLAY BOARD THEORY OF OPERATION

(Refer to Schematic No. 6809910.)

MUX 1 and MUX 2 from the microprocessor port are converted from 2 line to 4 line data by U3. The 4 line information is fed to U4, which is a source driver. The source driver turns on the +5V RAW (approximately +8V unregulated) to one of the four displays. At the same time, the BCD information is converted to 7 segment data and tries to drive all four displays. Since only one display has voltage applied, only that display will exhibit

the BCD/7 segment data.

Keyboard SW1 pulls both a column and a row low when a key is pressed. The fact that a column went low is detected by U5 pins 8 or 9 and is delayed by R7/C2 to prevent key bounce from double entering the data. The output of U5 pin 4 causes the processor board to latch the column and row information for later processing by the microprocessor.

### 1.8 TEST BOARD THEORY OF OPERATION

(Refer to Schematic No. 6809909.)

The Test Board consists of signal conditioning, various signal conversion devices, an Analog-to-Digital (A/D) Converter and input/output control.

The sequence starts when a data byte (DB1 to DB8) is latched into U2 by the SET bit. U2 is an octal latch with the outputs controlling analog multiplexers U5, U9, and U10.

If all the outputs from U2 are high with the exception of pins 5 and 6, then U10 pin 15 to pin 14 is on, applying the attenuated A sense voltage through U10 pin 6 to pin 7 to buffer U8 pin 5. The output of U8 is the input to TRMS converter U15 which, in turn, is applied to the active filter of U6 pins 1, 2 and 3 through U5 pin 10 to pin 11. The output of the active filter is applied to U1 pin 2. The 12-bit successive approximation A/D converter (U1) will convert the A sense voltage to digital information for the microprocessor to act upon.

A current measurement is made when the current transformer output is applied through U10 pin 2 to pin 3, to U11 pin 3. The output of U11 pin 3 is applied through U10 pin 10 to pin 11 and on to U8 pin 5. The path is the same as for the previously described A phase voltage.

When A phase wattage is selected, the A phase voltage is applied to pin 6 of multiplier U13 and the A phase current is applied to pin 1 of the same device. The instantaneous result is coupled through U5 pin 7 to pin 6 and to the active filter where it joins with the other signal paths. The voltage at pin 6 of the multiplier is the sense voltage divided by 50, so if the input voltage is 110V the pin 6 voltage is 2.2V RMS.

The current input is always scaled where 0.909 volts out of the CT is equal to 4.545A, 9.09A, 18.18A or 36.36A, depending on the model of the AC Power Source being used. This voltage is doubled by U11 pins 1, 2, and 3 and applied to pin 1 of the multiplier. For example, if there is 2.2V times 1.818V, the result will be 4V. Thus, 4V equals full scale for any model AC Power Source and the microprocessor program makes the proper manipulations to arrive at the correct answer based upon the program used.

Frequency-to-voltage converter U14 takes the logic signal that is two times the output frequency and converts this signal to a DC level proportional to the frequency. This voltage is coupled through U5 pin 15 to pin 14 where it joins the common signal path for filtering and conversion to digital.

Monostable multivibrator U3 is started by the SET signal that stored the input program. This timer will delay approximately 330 ms before starting the A/D converter. This delay is used to ensure settling of the appropriate converter and the active filter prior to making a measurement.

The SEL1 input, when low, enables U1 to output data on the data bus while SEL2 determines if it is the low byte or high byte of data.

When SET starts the sequence, the RS latch of U4 set, causing EXT INPUT 1 to go high. When U1 completes the conversion, U1 then causes EXT INPUT 1 to go low, signifying to the microprocessor that data is ready to be taken.

NOTES



## **SECTION II**

# **MAINTENANCE**

2.1 GENERAL

This section contains procedures for verification of performance disassembly, troubleshooting, and calibration of the PIP 9012. The PIP 9012 is delivered with all adjustments and calibrations completed. Further adjustment should not be required unless a malfunction occurs and/or certain critical parts are replaced.

If the procedures of this section and the circuit descriptions contained in Section I do not provide sufficient information to locate and correct a malfunction, the assistance of the Elgar Customer Service Department should be requested (refer to the PIP 9012 Operating Manual, Section III, paragraph 3.6). Equipment should not be returned to the Elgar factory without the express authorization of Elgar Corporation or its appointed representative. Elgar cannot assume responsibility for equipment returned without authorization.

WARNING

Hazardous voltages are present when operating this equipment. Read the SAFETY notices on page ii before performing any installation, operation, or maintenance.

2.2 REQUIRED TEST EQUIPMENT

The test equipment required to conduct performance verification procedures and for troubleshooting is listed in Table 2-1. Substitute equipment may be employed provided that equipment meets the accuracy specifications of the listed equipment.

Table 2-1. Required Test Equipment

Test Equipment	Recommended Type
Differential AC Voltmeter	Fluke Model 931B
Frequency Counter	H.P. Model 5315A
Digital Multimeter	Fluke Model 8050A
Oscilloscope	Tektronix Model 455
Distortion Analyzer	Krohn-Hite Model 6800
Phase Angle Meter	Dranetz Model 331

**2.3 DISASSEMBLY**

The PIP 9012 circuit boards may be accessed for calibration or maintenance by using the steps listed below (installation and removal of the PIP 9012 is described in Section II of the PIP 9012 Operating Manual).

**WARNING**

**Ensure power is removed when removing hardware holding the circuit cards, or when hinging the circuit cards.**

Perform the following:

1. Remove the AC Power Source top cover.
2. If the problem is on the Micro-processor Board, troubleshoot from the top of the board. If the trouble is not on the Micro-processor Board, remove the two screws (located approximately 3/4 of the way toward the rear of the Microprocessor Board) and hinge the Microprocessor Board up to provide access to the Main Board.

**NOTE**

The circuit boards in the PIP 9012 are sandwiched, with the Main Board at the bottom, the Test Board next to the top, and the Microprocessor Board at the top. To gain access to a board for alignment, the boards above the object board must be hinged up and out of the way as previously discussed.

**2.4 CALIBRATION ADJUSTMENTS**

All adjustments are made at the factory and should not require re-calibration unless a component has been replaced or the AC Power Source and/or the PIP 9012 has been exposed to severe vibration/shock.

If the PIP 9012 is moved from one Elgar AC Power Source to another of the same model, no re-calibration is required. If the PIP 9012 is moved to a different model, the open servo adjustment (steps 5 and 6 of paragraph 2.4.1 below) is the only adjustment required to match the PIP 9012 to the gain of the new AC Power Source.

**NOTE**

**ALL CALIBRATION IS ACCOMPLISHED IN LOCAL CONTROL.**

**2.4.1 Main Board Calibration****2.4.1.1 Quick Calibration Procedure**

Perform the following:

1. Program the PIP 9012 to 100V and 400 Hz.
2. Monitor the A phase output with the AC Digital Multimeter.
3. Open the servo leads and adjust A OPEN for 110.0V. If the PIP 9012 is a multi-phase unit, repeat this step for the B and C phase open potentiometers.

4. Close the servo leads and measure the output for exactly 100.0V output. Adjust the A-FS potentiometer for 100.0V output. If the PIP 9012 is a multi-phase unit, repeat this step for B-FS and C-FS.

#### 2.4.1.2 Standard Calibration Procedure

Perform the following:

1. Program the PIP 9012 to 100V and 800 Hz.
2. Monitor the A phase output with the AC Digital Multimeter and the distortion analyzer.
3. Adjust the THD-HI A phase and THD-LO A phase for minimum distortion on the distortion analyzer.
4. If the PIP 9012 is a multi-phase unit, monitor the B phase output and adjust THD-HI B and C and THD-LO B and C for minimum distortion on the distortion analyzer. Return the monitor to the A phase.
5. Open the servo leads and adjust A OPEN for 110.0V. If the PIP 9012 is a multi-phase unit, repeat this step for the B and C phases.
6. Close the servo and connect a clip lead from Output Low (the white binding post) to Digital Common of the PIP 9012 (the negative end of the 4700  $\mu$ F capacitor on the Main Board). Record the A phase voltage reading.
7. Move the clip lead from Output Low to Output High and adjust the A CMR so the reading equals the reading recorded in step 6 above.
8. If the PIP 9012 is a multi-phase unit, repeat steps 6 and 7 for the B and C phases. Remove the clip lead.
9. Adjust the A-FS potentiometer for 100.0V output (if the PIP 9012 is a multi-phase unit, also adjust the B-FS and C-FS potentiometers, respectively, for 100.0V).
10. Load the voltage to 10.0V and adjust A ZERO for a 10.0V output. If the PIP 9012 is a multi-phase unit, repeat this step for the B and C phases.
11. Repeat steps 9 and 10, as required, to compensate for the interaction of the adjustments.
12. If the PIP 9012 is a multi-phase unit, set the voltage to 100.0V. Connect a phase meter between the A and B phases. Adjust the 240° potentiometer for a 240° phase angle.

13. If the PIP 9012 is a multi-phase unit, set the frequency to 2000 Hz (CR)(LF) and adjust C11 for a 240° phase angle.

OPTION**2.4.2 Test Board Calibration**

1. Program the PIP 9012 to 120V and 400 Hz.
2. Using a DMM, measure the voltage from TP3 (high) to TP2 (common).
3. Adjust R8 for  $+5.000 \pm 0.001$  VDC.
4. Change the DMM to the AC 10V scale and move the high lead from TP3 to TP1.
5. Program the PIP 9012 for 1 # 4.
6. Adjust R30 for  $2.4 \pm 0.005$  VAC.
7. Move the DMM high lead to U10 pin 7 and adjust R37 for  $1.2 \pm 0.005$  VAC.
8. Program the PIP 9012 voltage to 100 VAC and adjust R44 for 100.0V on the PIP display.
9. Program the PIP 9012 voltage to 10.0 VAC and adjust R50 for 10.0V on the PIP display.
10. Repeat steps 7 and 8, as required, to compensate for the interaction of the adjustments.
11. Program the PIP 9012 voltage to 110.0V at 400 Hz and apply a load of approximately 80% of full load for the associated AC Power Source.
12. Program the PIP 9012 for 4 # 4.
13. Using a DMM, measure the AC voltage (on the 1 VAC range) at R33.
14. Using a DMM, measure the AC voltage at U11 pin 1 and adjust R36 for exactly twice the voltage measured at R33 in step 13 above.
15. Using a precision ammeter, measure the actual current to the load.
16. Adjust the current transformer adjustment until the PIP 9012 display equals the current measured by the precision ammeter in step 15 above.
17. Remove the load from the AC Power Source and monitor U13 pin 4 with a DC voltmeter.
18. Adjust R49 for zero on the DC voltmeter.
19. Reapply the load and calculate amps times volts (or use a precision voltmeter) to determine the wattage being drawn by the load.
20. Program the PIP 9012 for 7 # 4.

21. Adjust R40 so the PIP 9012 display equals the calculated wattage from step 19 above.
  22. Program the PIP 9012 to 0V at 50 Hz.
  23. Program the PIP 9012 for 0 # 4.
  24. Adjust R43 for 0050. on the PIP display.
  25. Program the PIP 9012 to 5000 Hz.
  26. Program the PIP 9012 for 0 # 4.
  27. Adjust R23 for 5000. on the PIP display.
  28. Repeat steps 22 through 27 as required to compensate for the interaction of the adjustments.
- NOTE**
- The following steps are for the three phase Test Board only.
29. Program the PIP 9012 to 100.0V at 400 Hz.
  30. Program the PIP 9012 for 2 # 4.
  31. Adjust R16 for 100.0 on the PIP display.
  32. Program the PIP 9012 for 3 # 4.
  33. Adjust R15 for 100.0 on the PIP display.
  34. Program the PIP 9012 to 400 Hz at 110.0V.
  35. Apply a load of approximately 80% of full load for the associated AC Power Source.
  36. Monitor the phase B current with a precision ammeter.
  37. Program the PIP 9012 for 5 # 4.
  38. Adjust the B phase current transformer adjustment so that the PIP display equals the readout on the precision ammeter.
  39. Move the precision ammeter to the C phase and apply the same load as specified in step 35 above.
  40. Program the PIP 9012 for 6 # 4.
  41. Adjust the C phase current transformer adjustment so that the PIP display equals the readout on the precision ammeter.

NOTES

# **SECTION III**

## **PARTS LIST**



**3.1 GENERAL**

This section contains a listing of all part numbers used in the manufacture of the PIP 9012. Parts are located on the diagrams in Section IV and correlated on the parts list by using their reference designators and/or Elgar part number.

**NOTE**

Trimming capacitors are factory selected and their replacement is considered beyond the scope of customer maintenance.

**3.2 SPARE PARTS ORDERING**

When ordering spare parts, specify the part name, part number, manufacturer, component value and rating. If complete assemblies are desired, contact Elgar Corporation, 9250 Brown Deer Road, San Diego, CA 92121. Specify the assembly number, instrument series number and instrument name when ordering.

Table 3-1 provides the Federal Stock Code Manufacturer (FSCM) identification for components used within this instrument.

Table 3-1 PIP 9012 FSCM Listing

Manufacturer	FSCM	Manufacturer	FSCM
ALLEN BRADLEY	01121	IMB	27556
AMATOM	06540	INTEL	34649
AMP	00779	KEMET	05397
ANALOG DEVICES	24355	LINEAR TECHNOLOGY	64155
BECKMAN	80740	MALLORY	8L593
BERQUIST		MOLEX	27264
BIVAR	32559	MONITOR	81654
BOURNS	32997	MONSANTO	50522
BURNDY	09922	MOTOROLA	04713
BURR BROWN	13919	NATIONAL	27014
CENTRALAB	99942	RCA	18714
CLAIREX	71785	SIGNAL TRANSFORMER	08779
CORNELL DUBLIER (CDE)	14655	SIGNETICS	18324
CTS	91637	SILICONIX	17856
DALE	71450	SMITH, H.H.	83330
ELECTRONIC APPLICATIONS	21317	SOUTHCO	94222
ELGAR	25965	SPECTROL	02111
ERIE	72982	SPRAGUE	56289
FAIRCHILD	07263	TEXAS INSTRUMENTS (T.I.)	01295
GRAYHILL	81073	T & B ANSLEY (THOMAS AND BETTS)	59730
HEWLETT PACKARD	28480	USECO	88245

### 3.3 PARTS LISTS

Table 3-2 provides the Parts Lists included in this section.

Table 3-2. PIP 9012 Parts Lists

Number	Assembly
5809912-01	MICROPROCESSOR BOARD ASSEMBLY
5809911-01	MAIN BOARD ASSEMBLY
5809910-01	DISPLAY BOARD ASSEMBLY
5809909-01	TEST BOARD ASSEMBLY
5809908-01	FINAL 9012 ASSEMBLY

## PARTS LIST

MICROPROCESSOR BOARD ASSEMBLY  
(ELGAR P/N 5809912-01)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
C1	828-10X-70	CAP MISC-VAR 8-80PF
C2	820-220-05	DIP MICA 22PF 500V 5%
C4	820-470-05	DIP MICA 47PF 500V 5%
C3,5,10-18,23	821-104-CK	.1 DISC 50V CK05BX104K
C6,8,9,20	823-106-41	CAP,TANT,10UF,25V,20%,RAD
C7	820-330-05	DIP MICA 33PF 500V 5%
C19	823-105-61	CAP,TANT,1UF,35V,20%,RAD
XU4	849-DIP-8X	DIP SOCKET 8 PIN
CR1	848-LM3-29	LM329CZ DIODE REFERENCE
XU7-9,XU11-14, XU22,25,26,28	849-DIP-20	DIP SOCKET 20 PIN
J4,XU1,2,5,6,23,24	849-DIP-16	DIP SOCKET 16 PIN
J7	5970007-02	D CABLE ASSY 4"
J6,XU19-21	849-DIP-24	DIP SOCKET 24 PIN
XU18,27	849-DIP-40	DIP SOCKET 40 PIN
XU3,XU15-17,XU29	849-DIP-14	DIP SOCKET 14 PIN
R1	801-106-05	10 M OHM 1/4 WATT 5%
R2	804-150-05	2W 5% 15R RC42GF150
R3,5	813-665-1F	1/8W 1% 6.65KR RN60C665
R4	813-301-1F	1/8W 1% 3.01K RN60C3011
R6	801-333-05	33 K OHM 1/4 WATT 2%
R7	801-512-05	5.1 K OHM 1/4 WATT 2%
RS1	818-222-SP	RES SIP 9RES 10PIN 2.2K
RS2	818-333-SP	RES SIP 9RES 10PIN 2%
U1,2,5,6	849-741-67	TTL 74167PC BCD-RATEMU
U3	849-H20-XX	HCMOS 74HC20 2X4IN-NAND
U4	849-TL0-72	LIN TLO72CP 2XFET-AM
U7	849-754-5L	CONV AD7545LN/CQ 12BITD
U8,9,12,13,22,28	849-7C3-74	CMOS MM74C374N OCTAL-LA
U10	849-H39-0X	HCMOS 74HC390 RIPPL COUNT
U11	849-H24-0X	HCMOS 74HC240 OCTAL BUFFR
U14	849-H37-3X	HCMOS 74HC373 OCTAL LATCH
U15	849-H00-XX	HCMOS 74HC00 4X2IIN-NAND

## PARTS LIST

MICROPROCESSOR BOARD ASSEMBLY  
(ELGAR P/N 5809912-01)

(CONTINUED)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
U16	849-H74-XX	HCMOS DUAL D FLIP FLOP
U17	849-H04-XX	HCMOS 74HC04 HEX INVERTER
U18	849-680-5E	CMOS MICROPROC
U19	849-273-2A	EPROM 2732A NO PROG 4KX
U21	849-611-62	RAM 2KX8 NO NEW DESIGNS!!
U23	849-H13-8X	HCMOS 74HC138 3TO8 DECODR
U24	849-MEM-EN	PROM MEM DECODE
U26	849-751-60	MOS GPIB TX/RX 75160
U27	849-991-4A	MOS GPIA TMS9914A 488
Y1	864-102-4X	XTLMC18A-10.24MHZ 005%
VR1	849-78L-10	REG UA78L10ACP 10V-T09
SW1	860-206-5X	206-5 DIP SWITCH5 CTS
	109-A15-70	STANDOFF SWAGE5/8X1/4.1
U25	849-751-61	MOS GPIB TX/RX 75161
U29	849-H02-XX	HCMOS 74HC02 4X2IN-NOR
J6A	856-243-7X	MALE HEADER 24PIN FLAT

## PARTS LIST

MAIN BOARD ASSEMBLY  
(ELGAR P/N 5809911-01)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
C1,19,20	823-106-41	CAP, TANT, 10UF, 25V, 20%
C2,3,5	823-336-51	CAP, TANT, 33UF, 25V, 10%
C4	824-478-01	4700@16V ALUM ELECTROLY
C6,8	821-104-CK	.1 DISC 50V CK05BX104K
C9	821-102-00	CAP DISC .001UF 10% 100
C13	820-102-01	DIP MICA 1000PF 1% 100V
C15	820-501-05	DIP MICA 500PF 500V 5%
C16	823-474-61	CAP, TANT, .47UF, 35V, 20%
CR1,2,5,6,10-12,14, 15,18,19,24,25,32	844-914-XX	1N914
CR3,4,30,31	845-400-4X	1N4004
CR7,8	843-474-4A	1N4744A 1W 15V ZENER
J2	849-DIP-16	DIP SOCKET 16 PIN
K1	861-6MG-3A	RELAY REED 3FORM A 6VDC
Q11	833-MP8-HI	N MPSA13 DARLINGTON 80V
Q7,10	832-P29-07	P PN2907 40V AM/SW
Q8,9	835-364-3P	N PN3643 30V HF/AM TO92
Q6	842-SD2-13	N SD213DE 30V MOSFT T7
R2,3	801-3R9-05	RES 1/4W 3.9OHM 5%
R72	801-101-05	100 OHM 1/4 WATT 2%
R47	801-241-05	240 OHM 1/4 WATT 2%
R13,45,73	801-102-05	1 K OHM 1/4 WATT 2%
R8,9	802-332-05	3.3 K OHM 1/2 WATT 2%
R43	801-472-05	4.7 K OHM 1/4 WATT 2%
R12,22,23	813-499-1F	1/8W 1% 4.99K RN60C4991
R30	813-249-1F	1/8W 1% 2.49K RN60C2491
R79	813-976-1F	1/8W 1% 9.76K RN60C9761
R4,26,27,42,44,46, 51,90	801-103-05	10 K OHM 1/4 WATT 2%
R55	801-153-05	15 K OHM 1/4 WATT 2%
R21,35,40	801-333-05	33 K OHM 1/4 WATT 2%
R84,85	818-390-3E	RES MISC 1/2W 1% 390K
R36,37,66	801-514-05	510 K OHM 1/4 WATT 2%
R24	801-105-05	1 M OHM 1/4 WATT 2%

## PARTS LIST

MAIN BOARD ASSEMBLY  
(ELGAR P/N 5809911-01)

(CONTINUED)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
R56	801-332-05	3.3 K OHM 1/4 WATT 2%
R62	801-473-05	47 K OHM 1/4 WATT 2%
R32,76	819-501-63	63P501 500R SPECTROL
R71	819-102-32	POT 1K 25TURN PC MNT
R31	819-502-64	POT 5K 10T 64W502
R25,63	819-104-63	63P104 100K SPECTROL
R93	813-249-1F	1/8W 1% 2.49K RN60C2491
U6,8	818-103-DR	RES DIP 10K 1% 8 RES
PAD, U1	109-771-73	7717-3 THERMALLOY TRANS
U1	849-VTL-2C	PHOTO RESISTOR LED DIODE
U2,3,5,7,16	849-TL0-72	LIN TLO72CP 2XFET-AM
U4,11,12	849-H86-XX	HCMOS 74HC86 4X2 XOR
U9	849-H40-40	HCMOS 74HC4040 12BIT CNTR
U17	849-N50-08	CONV DAC08E 8BIT DAC
U18	849-SA2-5D	PROM TBP28L22N SIN-LOOK
T1	850-ST5-16	ST5-16 PCB XFMR SIGNAL
	109-956-9B	STNDOFF-SWAGE 1.38"6-32

## PARTS LIST

DISPLAY BOARD ASSEMBLY  
(ELGAR P/N 5809910-01)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
R4,5,6,10	801-102-05	1 K OHM 1/4 WATT 2%
R9	801-153-05	15 K OHM 1/4 WATT 2%
R1	801-271-05	270 OHM 1/4 WATT 2%
R2,3	801-472-05	4.7 K OHM 1/4 WATT 2%
R2,3	801-512-05	5.1 K OHM 1/4 WATT 2%
R7	801-683-05	68 K OHM 1/4 WATT 2%
U6	818-103-SP	RES PAK SIP 10K (9)
U1	818-331-DS	316B331 DIP RESISTOR
U5	849-C40-93	CMOS CD4093BE 4X2IN SCH
U3	849-145-55	CMOS MC14555BCP 2X2TO4C
U4	849-298-1X	DRIV UDN2981A 8SOURCE-D
U2	849-74S-47	LS SN74LS47N 7SEG DRI
DS1,2,3,4	848-461-0X	DISPLAY,7SEGMENT,ORANGE
DS5,6,7,8,9,10	848-655-02	LED RED HI EFF WIDE ANG
Q1	832-P29-07	P PN2907 40V AM/SW T
Q2,3	835-364-3X	N 2N3643 30V HF/AM T1
Q2,3	835-364-3P	N PN3643 30V HF/AM TO92
J1	856-262-7X	RECPT 26PIN IDC ANSLEY
SW1	860-83A-02	SWT 3X4KEYBD 2OF7 CODE
C1	823-106-41	CAP,TANT,10UF,25V,20%,RAD
C2	823-105-61	CAP,TANT,1UF,35V,20%,RAD
CR1,2,3,4	844-914-XX	1N914
XDS1,2,3,4	849-DIP-14	DIP SOCKET 14 PIN
	109-908-08	SPACER LED MTG 0.08 LO
	109-302-2X	STANDOFF HINGED 1"
	111CC04-01	WASHER #4 SPLIT LOCK
	110CH04-04	SCREW 4-40 X 1/4 SBH
	2809910-01	A AW DISPLAY BD PIP9012
	6809910-01	A SCHM-DISPLAY BD 9012



## PARTS LIST

TEST BOARD ASSEMBLY  
(ELGAR P/N 5809909-01)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
R27	801-123-05	12 K OHM 1/4 WATT 2%
R26	801-222-05	2.2K OHM 1/4 WATT 2%
R24,41	801-335-05	3.3 M OHM 1/4 WATT 5%
R28,29	813-115-2F	1/8W 1% 11.5K RN60C1152
R42	813-200-1F	1/8W 1% 2KR RN60C2001F
R5	813-215-1F	1/8W 1% 2.15KR RN60C2151F
R6,45,46,47,48	813-221-2F	1/8W 1% 22.1KR RN60C221
R25	813-105-2F	1/8W 1% 10.5KR RN60C105
R3,51	813-200-2F	1/8W 1% 20KR RN60C2002F
R38	813-365-1F	1/8W 1% 3.65K RN60C 365
R4,31	813-374-1F	1/8W 1% 3.74KR RN60C374
R39	813-402-2F	1/8W 1% 40.2K RN60C4022
R1	813-576-2F	1/8W 1% 57.6KR RN60C576
R7	813-649-1F	1/8W 1% 6.49KR RN60C649
R9,14	816-536-3F	RES 536K 1% RN65C
R33	818-15T-2F	RES 15 OHM 1% 1/4W
R44	819-203-99	POT MISC 25TURN 3299W-2
R8	819-102-32	POT 1K 25TURN PC MNT
R23	819-103-32	POT 10K 1/2S 3255W-1-10
R43,49,50	819-104-99	POT3296W-1-104 25T 100K
R40	819-202-64	POT 3299W-1-202 25TURN
R30,36,37	819-501-99	POT MISC 25TURN 3299W-5
R2	801-155-05	1.5M OHM 1/4WATT 5% MF
U1	849-758-2K	CONV AD7582KN 12BIT SAA
U5,10	849-DG2-01	IC ANALOG SW :DG201ACJ
U14	849-VFC-32	CONV VFC32KP V-TO-F CON
VR1	849-79L-05	REG LM79L05ACZ NEG5V TO
U8,11	849-340-2A	LIN MC34002A 2XFET-AMP
U13	849-AD6-32	MULT AD632A ANA MULT
U15	849-434-1X	CONV 4341 RMS CONVE
U3	849-C40-98	CMOS CD4098BE 4X2IN SCH
U4	849-C40-11	CMOS CD4011BE 4X2IN NA
U6	849-TL0-72	LIN TLO72CP 2XFET-AM
U2	849-7C3-74	CMOS MM74C374N OCTAL-LA

## PARTS LIST

TEST BOARD ASSEMBLY  
(ELGAR P/N 5809909-01)

(CONTINUED)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
CR1,2	844-914-XX	1N914
CR3	848-329-BZ	DIO MISC LM329BZ 1MA 6.
C12	822-105-PP	1UF 1% GA2C105F POLYPRO
C21	822-824-PP	.82UF GA2C824F POLYPRO
C11	822-274-PP	.27UF1% GA2C274F POLYPROA
C4	822-222-05	CAP .0022UF 10% 200VFLM
C9	822-392-11	.0039 100V 1% BA1B392F
C14,18	823-105-61	CAP,TANT,1UF,35V,20%,RAD
C1,2,7,19,20	823-106-41	CAP,TANT,10UF,25V,20%,RAD
C13	820-252-01	DIP MICA 2500PF 1% 500V
C8	820-561-05	DIP MICA 560PF 500V 5%
C16	821-103-00	CAP .01 DISC 100V-150V
C3,5,6,15,17	821-104-CK	.1 DISC 50V CK05BX104K
C10	822-684-12	CAP-WRPFILL .68 100V 1%
	109-A15-30	STANDOFF SWAGE 5/8X1/4
	9950511-02	WIRE, BUS, 16 GA TINNED
	9809909-01	D PCB TEST PIP 9012
	6809909-01	B SCH TEST BD 9012
	2809909-01	D AW TEST BD PIP 9012
	856-262-7X	RECPT 26PIN IDC ANSLEY
	856-523-4Z	RECPT 15 PIN MICROSPDX
	849-DIP-28	DIP SOCKET 28 PIN
	849-DIP-16	DIP SOCKET 16 PIN
	849-DIP-14	DIP SOCKET 14 PIN
	856-523-0X	PIN-CRIMP TERMINAL
	856-523-1X	HOUSING-15 PIN CONN
	5970007-02	D CABLE ASSY 4"

## PARTS LIST

FINAL 9012 ASSEMBLY  
(ELGAR P/N 5809908-01)

<u>REF. DESIG.</u>	<u>PART NO.</u>	<u>DESCRIPTION</u>
	5809911-01	E MAIN BD ASSY 9030-10
	5809022-01	G PROC/STO BD ASY 9030
	5261014-06	B FLAT CABLE ASSY
	9809908-01	B FRONT PANEL 9030 SS
	899-263-09	RETAINER KIT FERRUL/SCR
	110AH04-A2	SCREW BINDER HD 2-56X5/
	110DH04-03	SCREW 6-32 X 3/16" SBH
	110DH05-06	SCREW 6-32 SBH 3/8
	842-TIP-29	N-TIP29B 80V AM/SW T2
	842-TIP-30	P TIP30B 80V AM/SW T2
	849-780-5P	REG UA7805UC 5V-TO2
	109-220-PD	INSULATOR 3323-07FR-56
	109-093-SW	WASHER SHOULDER
	<i>CABLE TYPE →</i> 5970080-01	B ASY CABLE GPIB 2253M2
	<i>GPIB CLO PIP TYPE →</i> 9809008-02	A CABLE INTERCONNECT
	109-IEE-MT	STUD MT GPIB PIP 552633

NOTES

# **SECTION IV**

# **DIAGRAMS**

**4.1 GENERAL**

This section contains schematic diagrams and parts layout diagrams for the PIP 9012. The schematic diagrams should be used to understand the theory of operation and as an aid in troubleshooting the unit.

Components identified as "trim" or "FSV" are factory selected parts whose values are determined at the time of final checkout.

**4.2 DIAGRAMS**

Table 4-1 provides a listing of the diagrams included in this section.

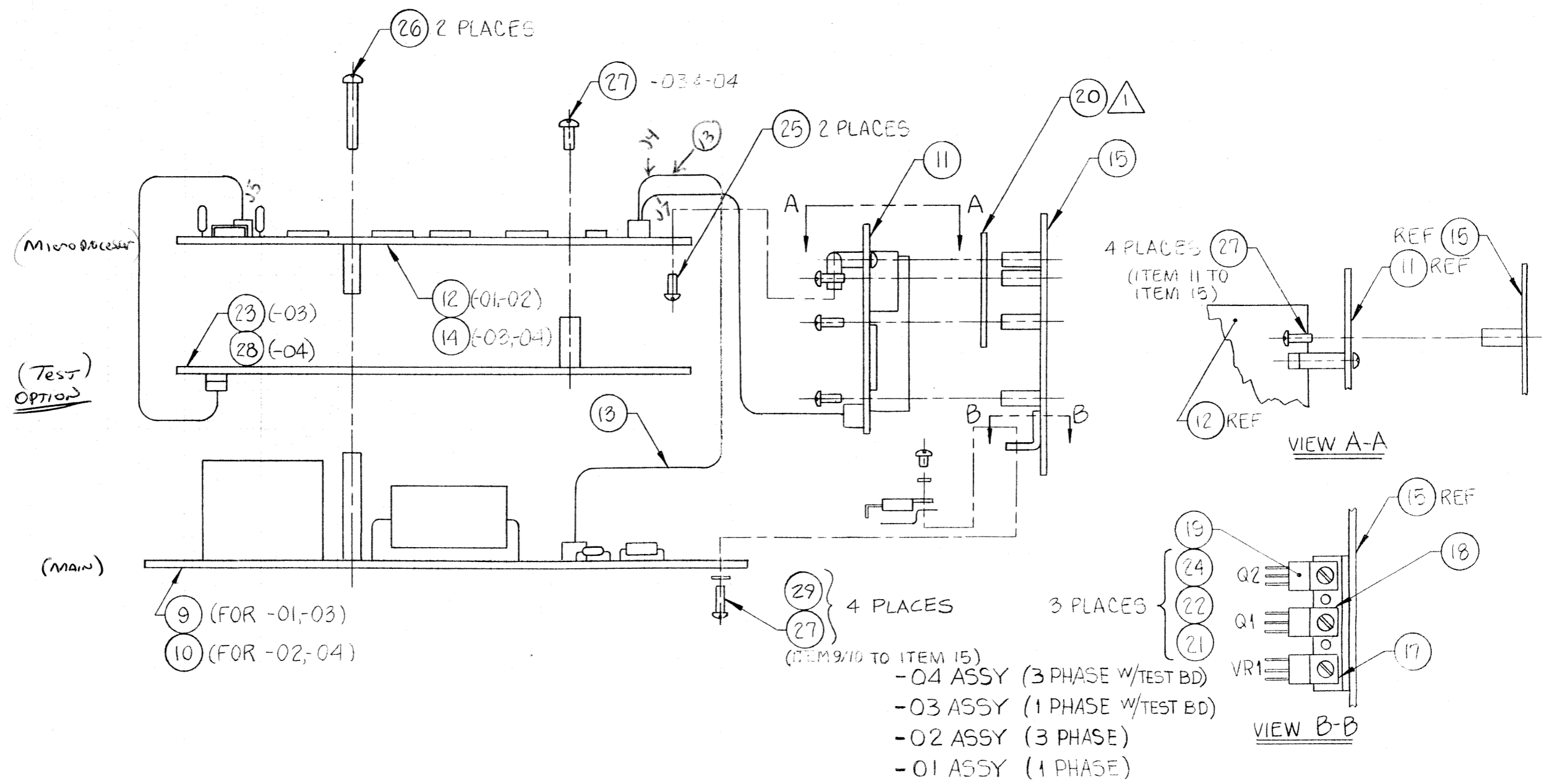
**Table 4-1. PIP 9012 Diagram Listing**

Diagram Number	Component	Sheet Number
5809915	Main Assembly	10 of 10
5809911	Main Board (Single Phase) Assembly	6 of 6
5809907	Main Board (Three Phase) Assembly	6 of 6
5809912	Microprocessor Board Assembly	6 of 6
5809910	Display Board Assembly	4 of 4
5809909	Test Board Assembly	12 of 12
6809907	Main Board Schematic	1 of 1
6809909	Test Board Schematic	1 of 1
6809910	Display Board Schematic	1 of 1
6809912	Microprocessor Board Schematic	1 of 1

Diagram sheets not included consist of Parts Lists which have been reformatted and are covered in Section III. As a result, the sheet counts on the diagrams do not apply.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT. 1	03	

D  
C  
B  
A



- 04 ASSY (3 PHASE W/TEST BD)
- 03 ASSY (1 PHASE W/TEST BD)
- 02 ASSY (3 PHASE)
- 01 ASSY (1 PHASE)

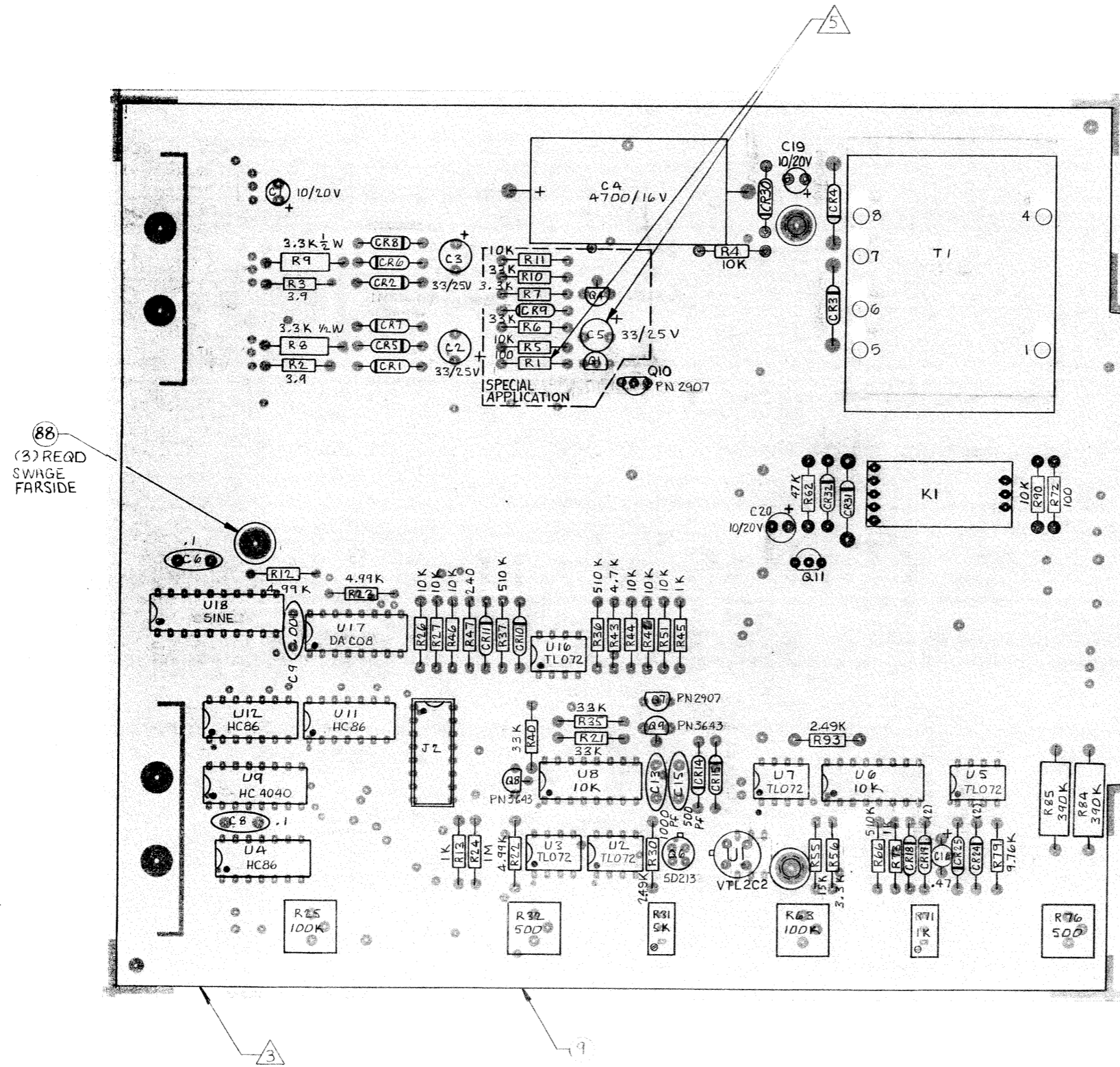
2. ITEM 16 FERRULE SCREW KIT NOT SHOWN ON FACE OF PNG.

▲ BOND ITEM 20 TO ITEM 15 USING SUPER BOND EPOXY #495.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		CONTRACT NO.		<b>ELGAR</b>	
DECIMALS FRACTIONS ANGLES		FIRST MADE FOR:			
XX ± .03	± 1/32	± 1/2°	APPROVAL	DATE	MAIN ASSY.
.XXX ± .010			DRAWN	6/8/85	
DO NOT SCALE THIS DRAWING			CHECKED	6/20/85	
MATERIAL:			PROJ ENG		
NEXT ASSY.	USED ON	FINISH	QA-REL		
APPLICATION		9012 SER ES			SIZE
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF ELGAR CORPORATION, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, ELGAR CORPORATION RESERVES ALL PATENT, PROPRIETARY, DESIGN, USE, SALE, MANUFACTURING AND REPRODUCTION RIGHTS THERETO.					C
					CODE IDENT. NO.
					5809915
					DRAWING NO.
					8
					REV
					C
					SCALE FULL
					SHEET 10 OF 10

ZONE		LTR		REVISIONS		DATE	APPROVED
				DESCRIPTION			
				SEE SHEET (1) 'A' SIZE			



88  
(3) REQD SWAGE FAR SIDE

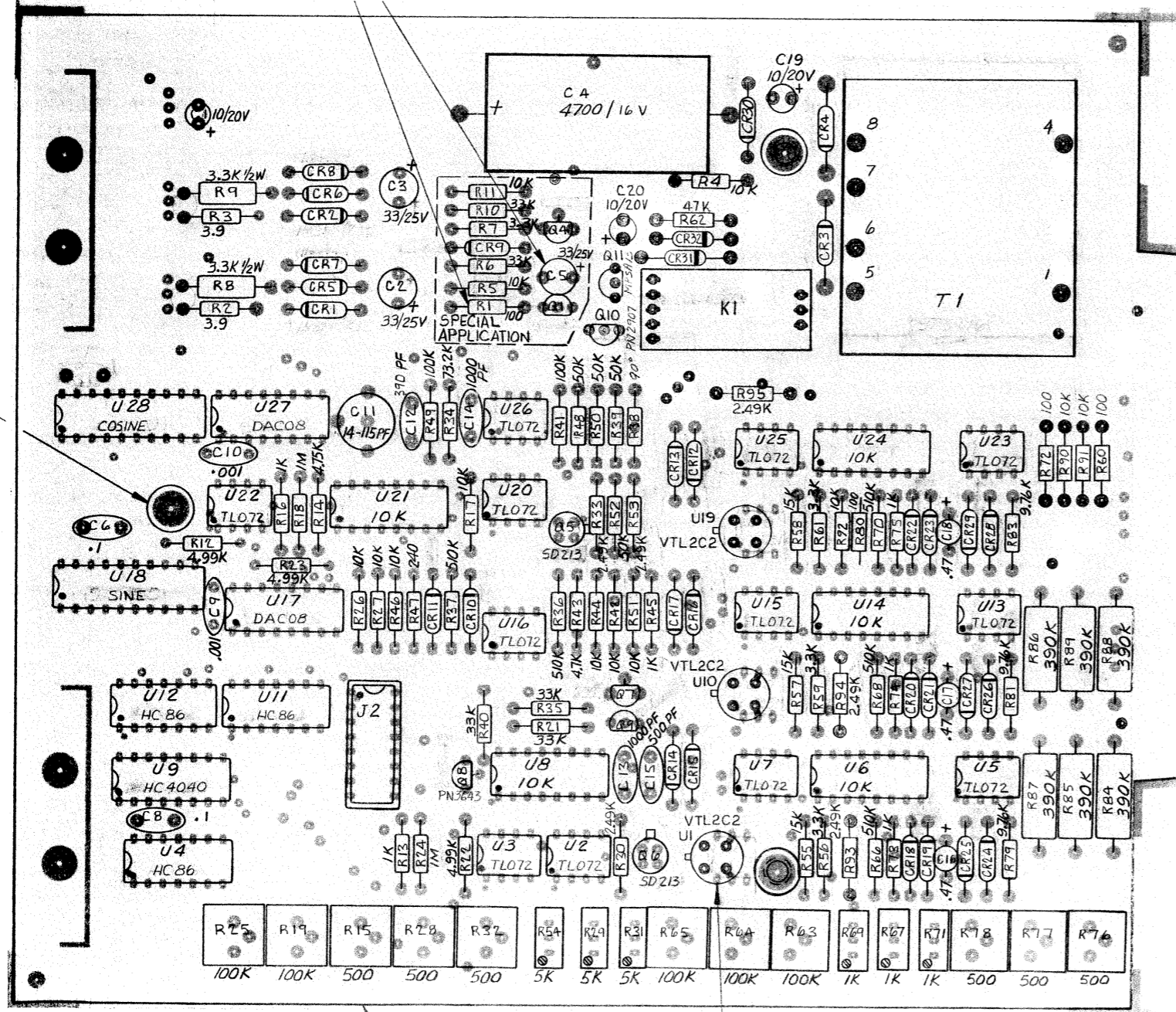
-01 ASSY SHOWN

- 5 RI, C5 INSTALLED ON -01 ASSY.
- 4 DO NOT INSTALL U18 IN A SOCKET.
- 3 IDENTIFY APPLICABLE DASH NO. AND REV. LTR.
- 2. CAPACITANCE VALUES ARE IN MICROFARADS
- 1. RESISTANCE VALUES ARE IN OHMS.
- NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON:		CONTRACT NO.		<b>ELGAR</b>
DECIMALS	FRACTIONS	ANGLES	FIRST MADE FOR:	
XX ± .03	± 1/32	± 1/2°	APPROVAL	ASSY, MAIN BD ØA PIP SERIES 9012/9030
XXX ± .010			DATE	
DO NOT SCALE THIS DRAWING			DRAWN	
MATERIAL:			CHECKED	
NEXT ASSY.		USED ON	PROJ ENG	QA-REL
APPLICATION		FINISH:		
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF ELGAR CORPORATION AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, ELGAR CORPORATION RESERVES ALL PATENT, PROPRIETARY, DESIGN, USE, SALE, MANUFACTURING AND REPRODUCTION RIGHTS THERE TO.				
SIZE	CODE IDENT. NO.	DRAWING NO.	REV	
D	25965	5809911	D	
SCALE 2:1		SHEET 4 OF 4		



ZONE		LTR		REVISIONS		DATE	APPROVED
				DESCRIPTION			
				SEE SHEET (1) A1 SIZE			



(30) READ SWAGE FAR SIDE

3

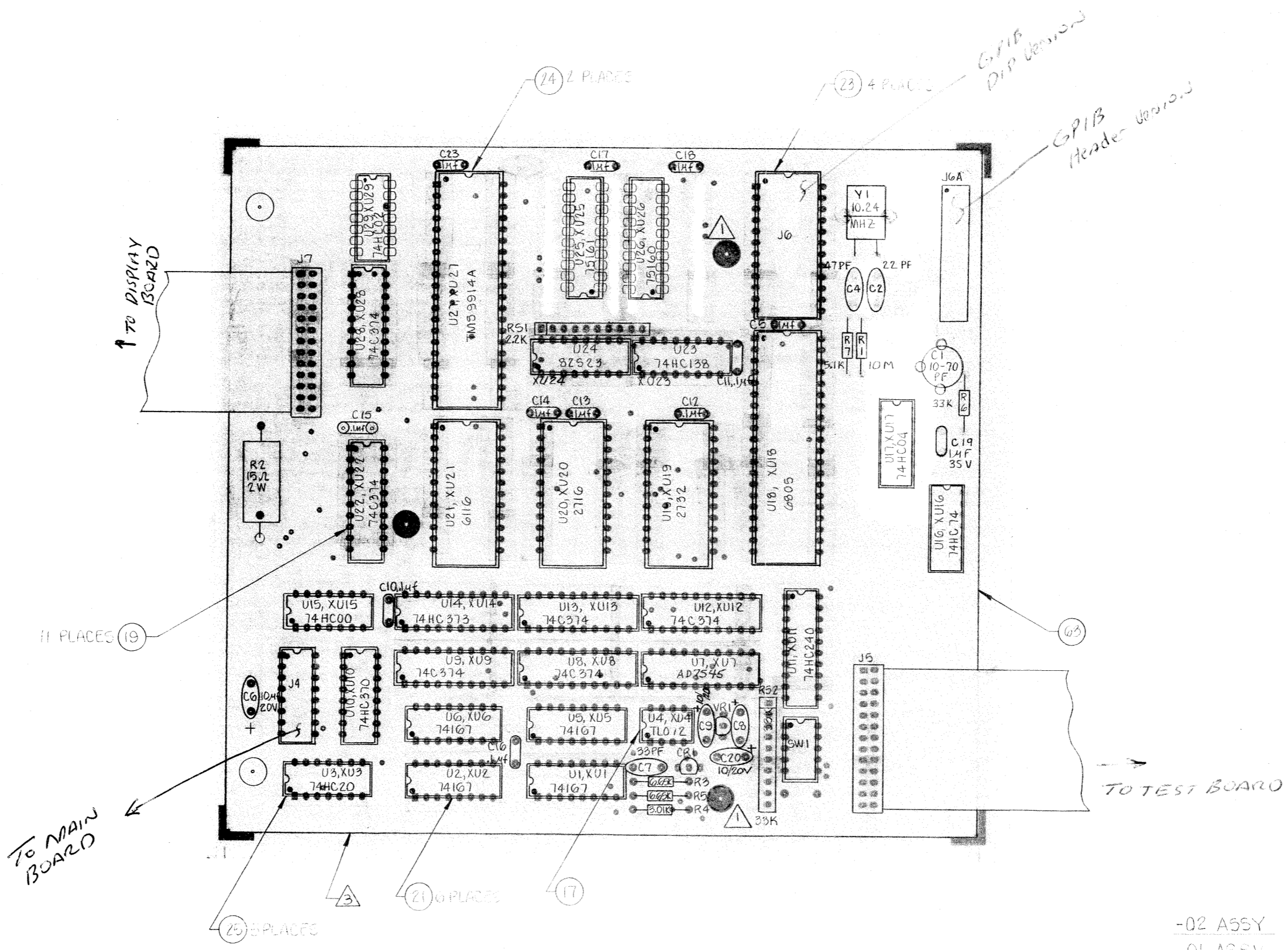
99 3PL

-01 ASSY

- 5. R1, C5 INSTALLED ON -01 ASSY.
- 4. DO NOT INSTALL U18 AND U28 IN SOCKETS.
- 3. IDENTIFY APPLICABLE ASSY DASH NO. AND REV. LTR.
- 2. CAPACITANCE VALUES ARE IN MICROFARADS.
- 1. RESISTANCE VALUES ARE IN OHMS.
- NOTES: UNLESS OTHERWISE SPECIFIED

CONTRACT NO.		FIRST MADE FOR:		<b>ELGAR</b>	
APPROVAL		DATE			
DRAWN		4-3-85		ASSY MAIN BD Ø A,B,C PIP SERIES 2012/9030	
CHECKED		4-4-85			
PROJ ENG				SIZE	
QA-REL				CODE IDENT. NO	
APPLICATION		FINISH:		DRAWING NO	
NEXT ASSY.		USED ON		D 25965	
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF ELGAR CORPORATION AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, ELGAR CORPORATION RESERVES ALL PATENT, PROPRIETARY, DESIGN, USE, SALE, MANUFACTURING AND REPRODUCTION RIGHTS THERETO.				5809907	
				SCALE 2:1	
				SHEET 5 OF 5	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT. 1	CJ	



GP1B Dip Version  
GP1B Header Version

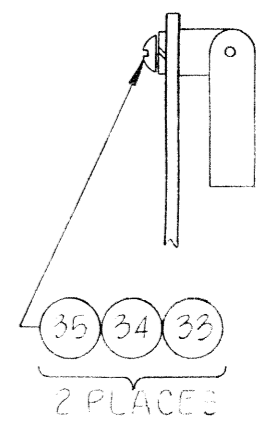
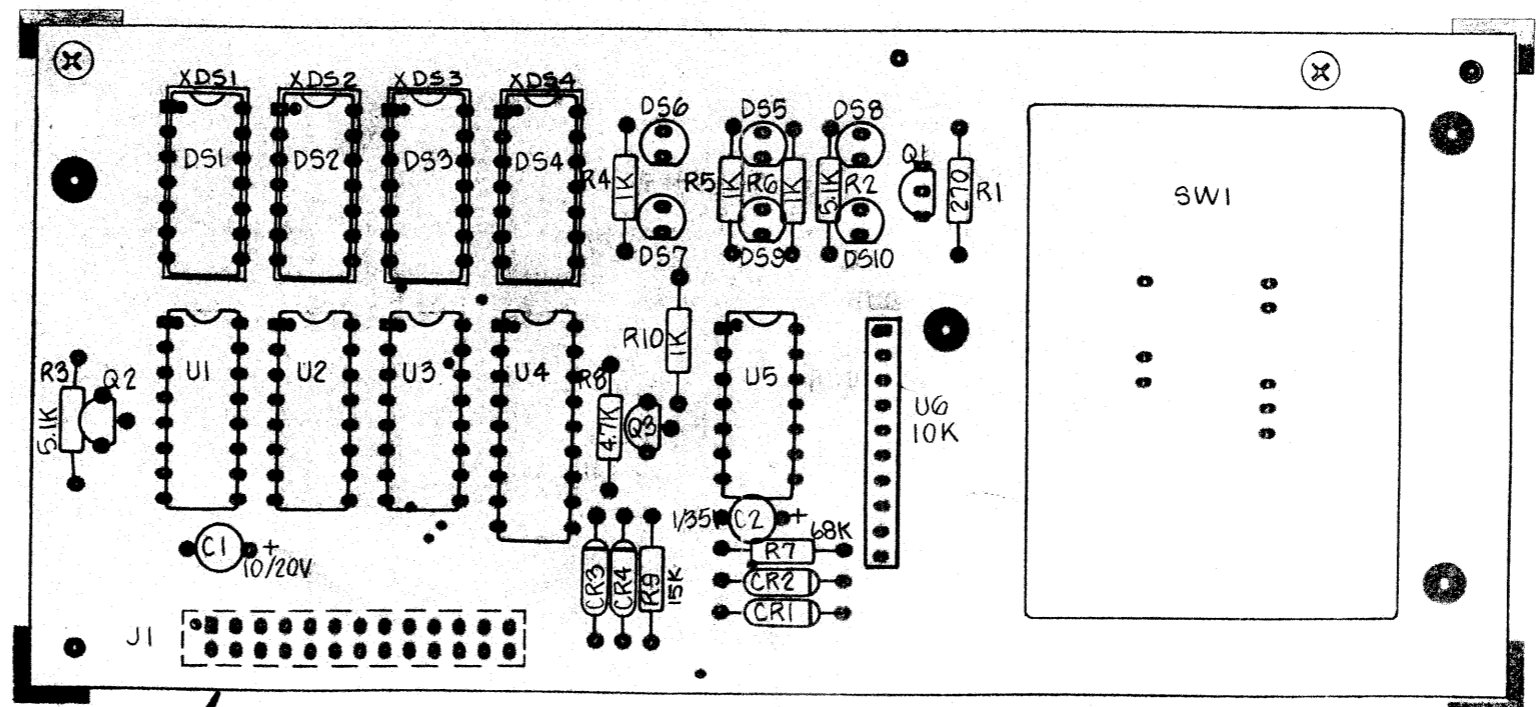
-02 ASSY  
-01 ASSY

- 3 IDENTIFY APPLICABLE ASSY DASH NO. AND REV. LTR.
- 2 U20 NOT NORMALLY INSTALLED
- 1 SPACER (ITEM 00) IS SWAGED ON NEAR SIDE

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:		CONTRACT NO.		<b>ELGAR</b>
DECIMALS	FRACTIONS	ANGLES	FIRST MADE FOR:	
.XX ± .03	± 1/32	± 1/2°	APPROVAL	
XXX ± .010			DATE	
DO NOT SCALE THIS DRAWING		MATERIAL:		PROCESSOR BD ASSY
APPLICATION		QA-REL		
NEXT ASSY. USED ON		PROJ ENG		
FINISH:		DATE		SIZE
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF ELGAR CORPORATION AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, ELGAR CORPORATION RESERVES ALL PATENT, PROPRIETARY, DESIGN, USE, SALE, MANUFACTURING AND REPRODUCTION RIGHTS THEREOF.		DATE		CODE IDENT. NO.
		DATE		DRAWING NO.
		DATE		REV
		DATE		G
		DATE		SCALE 2:1
		DATE		SHEET 10 OF 10

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

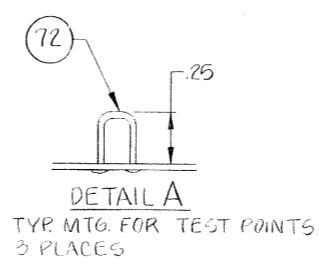
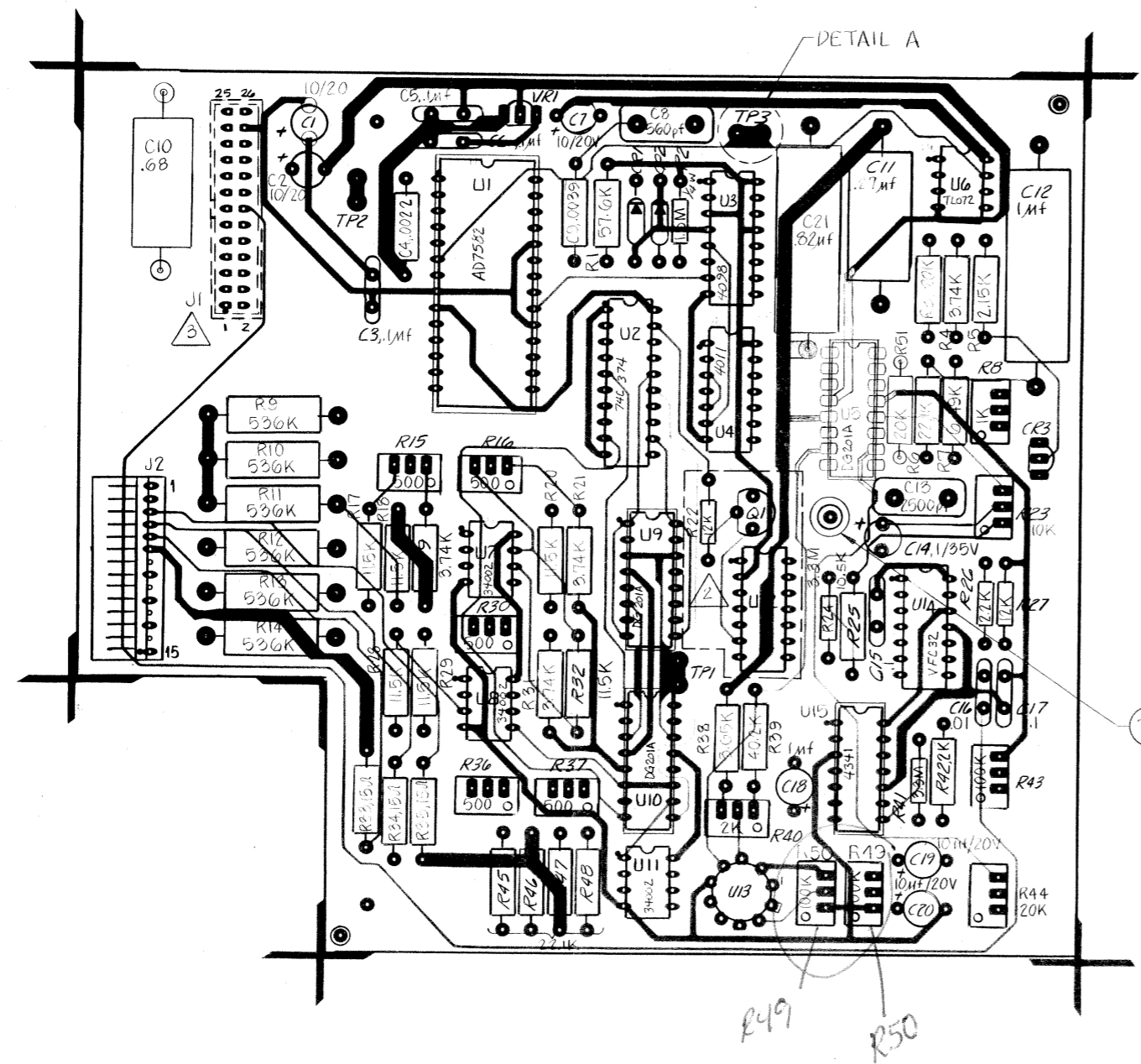


-01 ASSY SHOWN

3. IDENTIFY APPLICABLE ASSY DASH NO. AND REV. LTR.  
 2. DS1-DS4 ARE 348-401-2X.  
 1. DIODES ARE ALL 1N514.  
 NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:		CONTRACT NO.		<b>ELGAR</b>	
DECIMALS	FRACTIONS	ANGLES	FIRST MADE FOR		
.XX ± .03	± 1/32	± 1/2°	APPROVAL	DATE	DISPLAY BD ASSY
.XXX ± .010	DO NOT SCALE THIS DRAWING		DRAWN	CJ 6/5/85	
MATERIAL:		CHECKED	PROJ ENG	6/14/85	
NEXT ASSY.		USED ON		QA-REL	
APPLICATION		FINISH		SIZE	REV
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF ELGAR CORPORATION AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, ELGAR CORPORATION RESERVES ALL PATENT PROPRIETARY DESIGN USE SALE, MANUFACTURING AND REPRODUCTION RIGHTS THERETO.				C	A
				CODE IDENT NO	DRAWING NO
				25965	5809910
				SCALE 2:1	SHEET 4 OF 4

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
002	SH.T.T		
			CJ

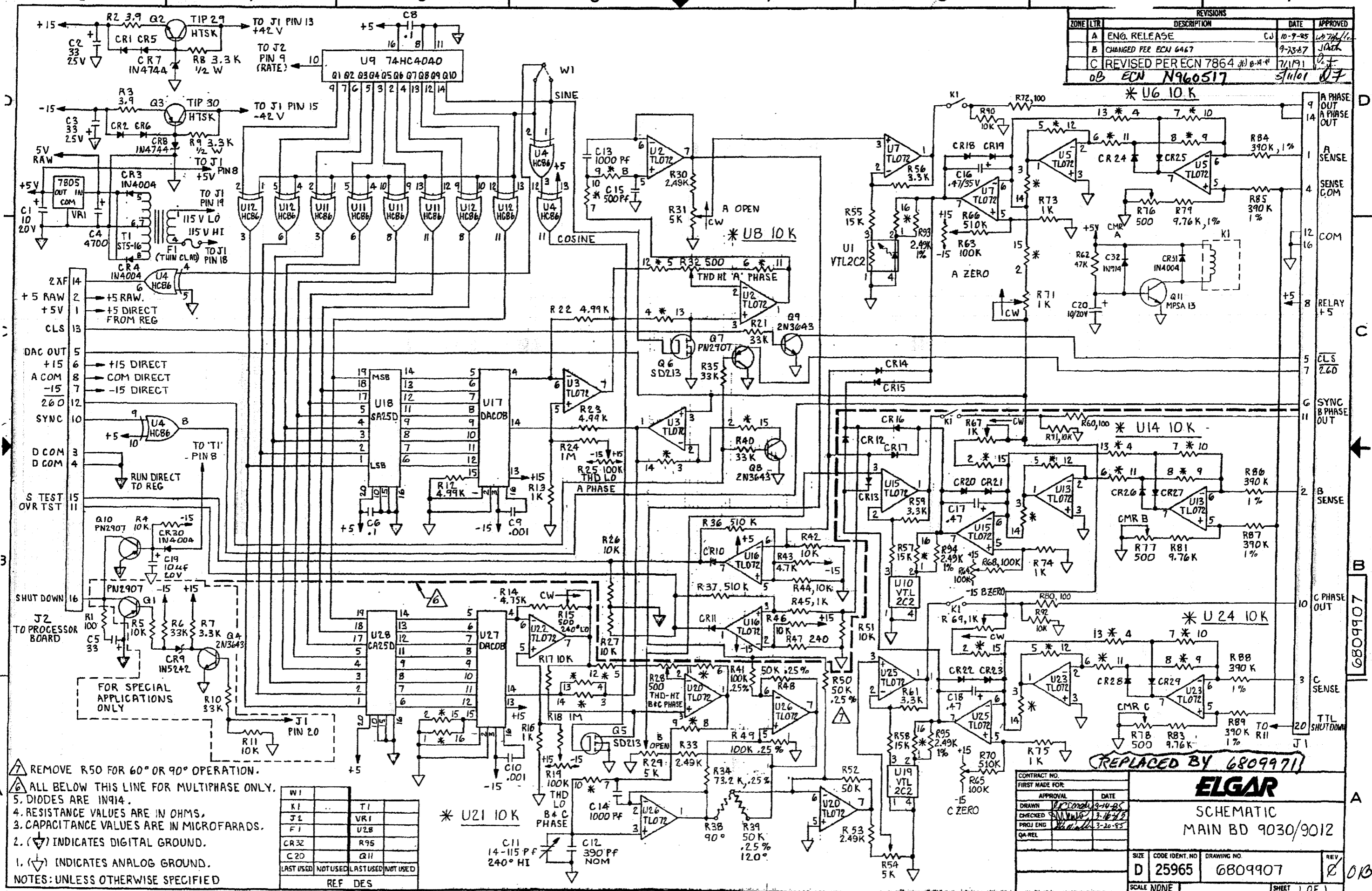


-02 ASSY 2 AND 3 PHASE  
 -01 ASSY 1 PHASE

- 4 INSTALL FROM NEAR SIDE (SWAGE FAR SIDE)
  - 3 J1 IS MOUNTED ON BOTTOM OF BD.
  - 2 SPECIAL APPLICATIONS ONLY.
1. FOR SCHEMATIC DIAGRAM SEE 6809909-C1.  
 NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES - .XX - - .XXX -		CONTRACT NO.		<b>ELGAR</b>  PRINTED CIRCUIT ASSY TEST BOARD
MATERIAL		APPROVALS	DATE	
FINISH		CHECKED	DATE	
DO NOT SCALE DRAWING		PROJ ENG.	DATE	
		9012 PIP	8-8-85	SIZE FSCM NO. DWG. NO. REV D 25965 5809909 F
		SCALE 2/1	SHEET 12 OF 12	

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
A	ENG. RELEASE	10-9-85	WJ
B	CHANGED PER ECN 6467	9-23-87	JAK
C	REVISED PER ECN 7864	7/1/91	WJ
0B ECN N960517		5/1/01	WJ



7 REMOVE R50 FOR 60° OR 90° OPERATION.  
 6 ALL BELOW THIS LINE FOR MULTIPHASE ONLY.  
 5. DIODES ARE IN414.  
 4. RESISTANCE VALUES ARE IN OHMS.  
 3. CAPACITANCE VALUES ARE IN MICROFARADS.  
 2. (∇) INDICATES DIGITAL GROUND.  
 1. (∇) INDICATES ANALOG GROUND.  
 NOTES: UNLESS OTHERWISE SPECIFIED

W1	T1
K1	VR1
J2	VR1
F1	U28
CR32	R95
C20	Q11
LAST USED	NOT USED
REF	DES

REPLACED BY 6809971

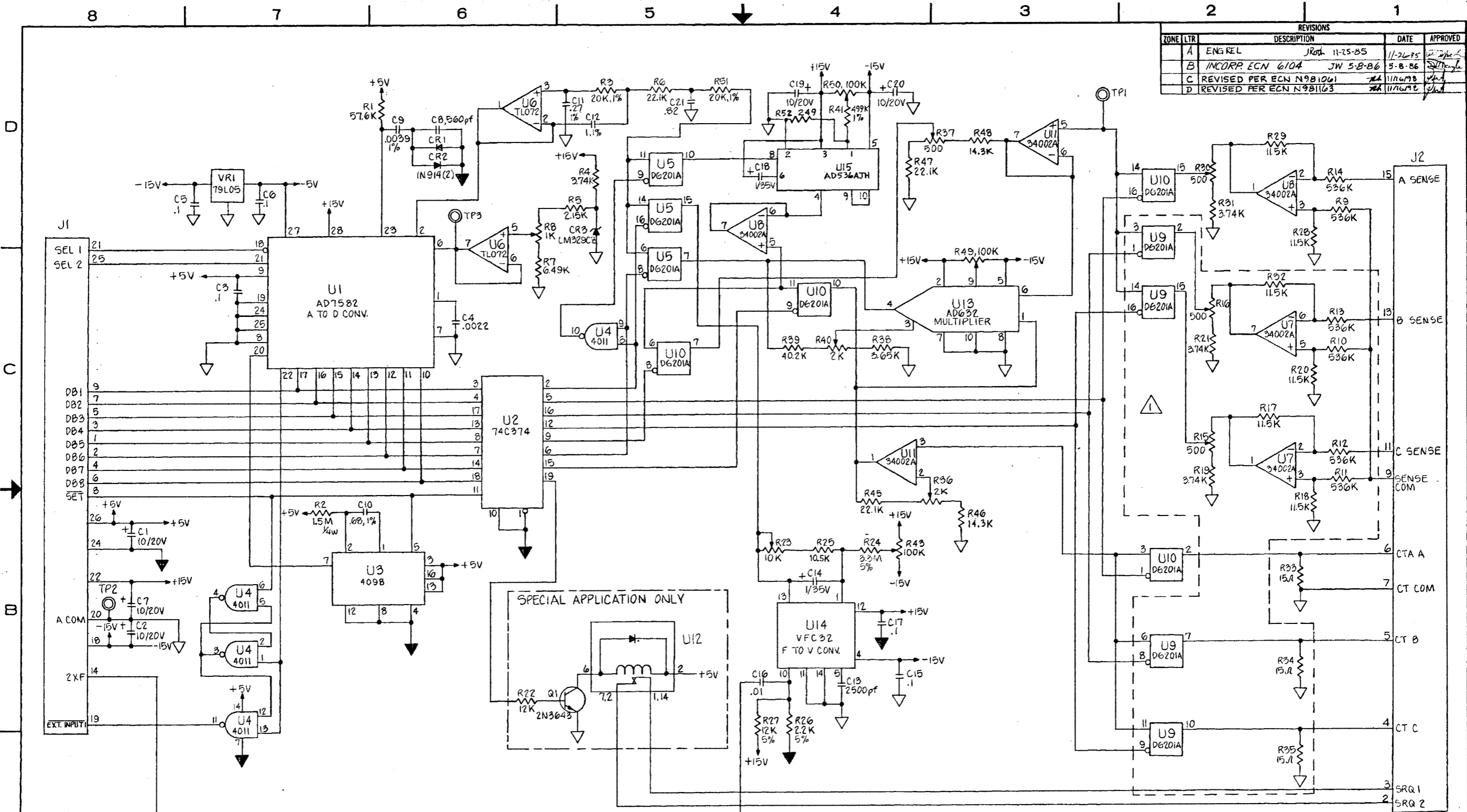
**ELGAR**

SCHEMATIC  
MAIN BD 9030/9012

CONTRACT NO.	FIRST MADE FOR:
APPROVAL	DATE
DRAWN	DATE
CHECKED	DATE
PROJ ENG	DATE
QA-REL	

SIZE	CODE IDENT. NO	DRAWING NO	REV
D	25965	6809907	010

SCALE NONE SHEET 1 OF 1



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A	ENGR EL	JRd. 11-25-85	11-26-85	[Signature]
B	INCD RP	ECN 6104 JW 5-B-86	5-8-86	[Signature]
C	REVISED PER	ECN N981001	11/16/88	[Signature]
D	REVISED PER	ECN N981103	11/16/88	[Signature]

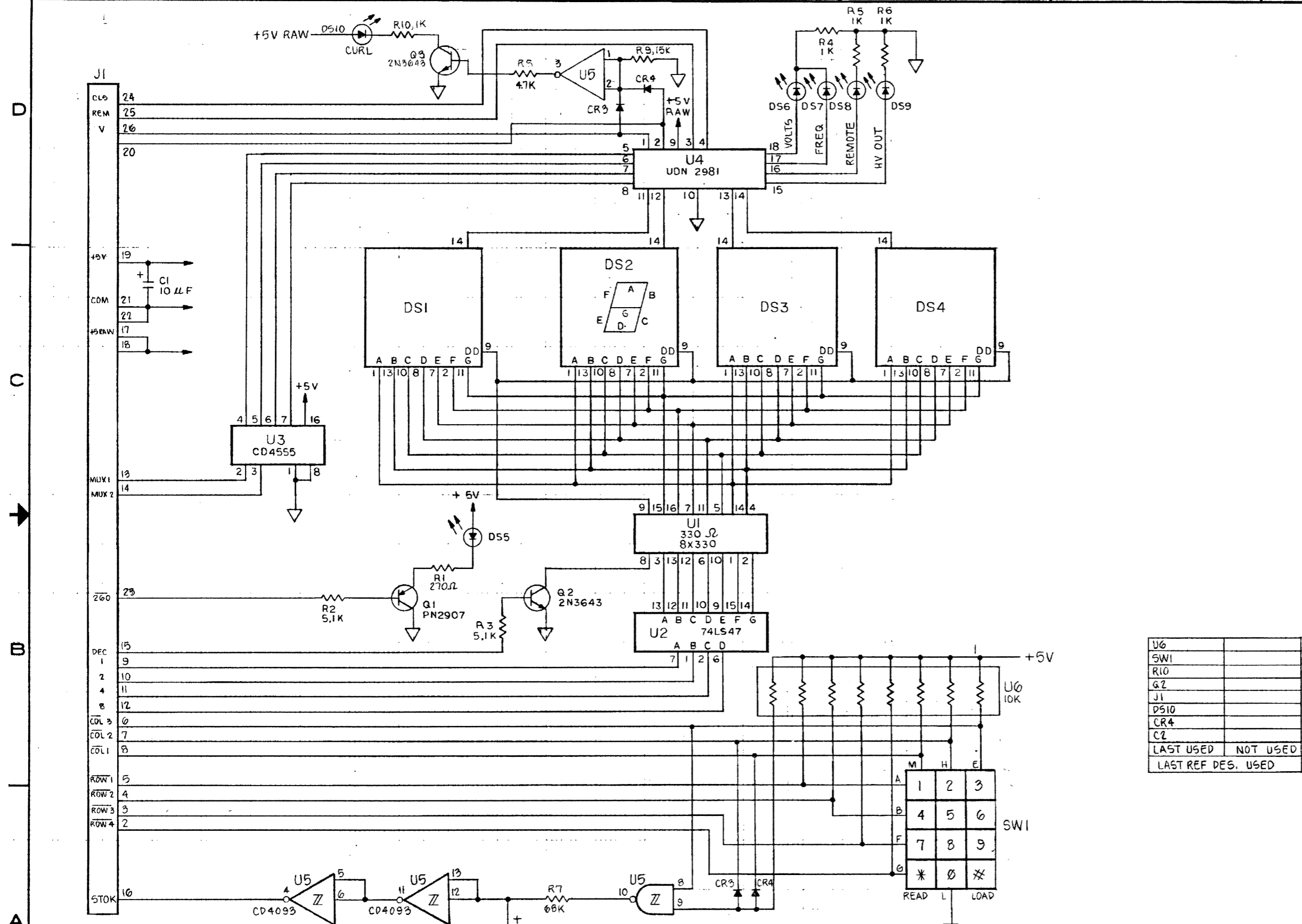
- 4.  $\nabla$  DIGITAL COMMON  $\nabla$  ANALOG COMMON.
- 3. ALL CAPACITORS ARE IN MICRO FARADS.
- 2. ALL RESISTORS ARE 1/8W, 1%, AND IN OHMS
- $\triangle$  COMPONENTS NOT USED FOR PHASE I VERSION.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: DECIMALS FRACTIONS ANGLES .XX ± .03 ± 1/32 ± 1/2° XXX ± .010 DO NOT SCALE THIS DRAWING		CONTRACT NO. FIRST MADE FOR: APPROVAL DATE DRAWN CJS 6/17/85 CHECKED [Signature] 8-7-85 PROJ ENG [Signature] 8-8-85 QA-REL		<b>ELGAR</b>	
NEXT ASSY. USED ON APPLICATION		MATERIAL:		TEST BD. SCHEMATIC	
FINISH:		9012 PIP		SIZE D	CODE IDENT. NO. 25965
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6809909

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		ENG. REVISION	11-26-83	



U6	
SW1	
R10	
Q2	
J1	
DS10	
CR4	
C2	
LAST USED	NOT USED
LAST REF DES.	USED

2. DIODES ARE ALL IN914.  
 1. RESISTORS ARE ALL 1/4W, 5%.  
 NOTES: UNLESS OTHERWISE SPECIFIED.

CONTRACT NO.		<b>ELGAR</b>	
FIRST MADE FOR:	APPROVAL:	DATE:	
DRAWN:	CHECKED:	DATE:	
PROJECT:	QA REL:		
SIZE: D		CODE IDENT. NO.: 25965	DRAWING NO.: 6809910
SCALE: NONE		SHEET 1 OF 1	

