KEPCO

DIGITAL PROGRAMMER

SN
QUARTER-RACK

Model SN 488-122

Serial No. H1302844

instruction manual

KEPCO®

KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, N.Y. 11352 U.S.A. • (212) 461-7000 • TWX #710-582-2631 • Cable: KEPCOPOWER NEWYORK

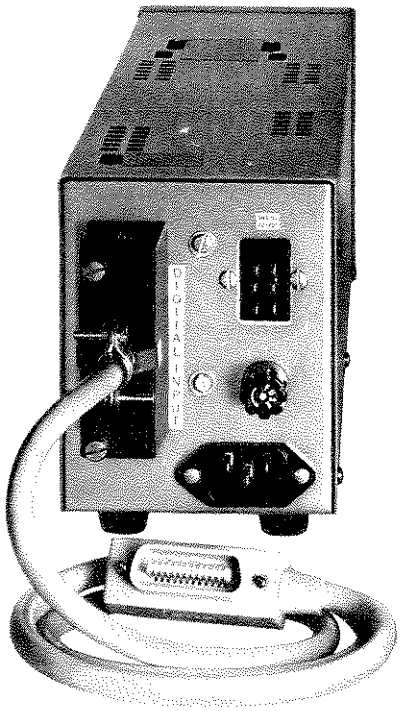


FIG. 1-1 KEPCO QUARTER-RACK DIGITAL PROGRAMMER.
(SERIES SN 488 SHOWN).

SECTION I – INTRODUCTION

1-1 SCOPE OF MANUAL

1-2 This manual contains instructions for the installation, operation and maintenance of the Series SN 488 and SN 500 Digital Programmers, manufactured by Kepco Inc., Flushing, New York, U.S.A.

1-3 GENERAL DESCRIPTION

1-4 The Kepco Series SN 488 and SN 500 Digital Programmers make it possible to control the output of a suitable power supply by means of digital input signals. The SN Programmer is used as the interface between a digital data bus and the d-c power supply to be programmed. The SN programmers accept digital data from the data bus and convert this data to an analog voltage output, which serves as the control signal input for the d-c power supply (See Fig. 1-2). In response to the control signal, the d-c power supply is programmed to the magnitude initially commanded by the data bus controller.

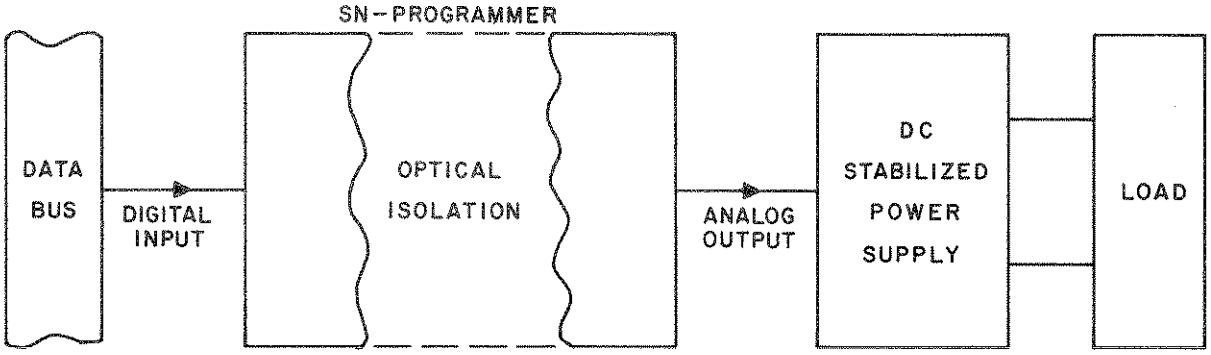


FIG. 1-2 DIGITAL POWER SUPPLY PROGRAMMING SYSTEM

1-5 There are two SN series of programmers:

A) Series SN 500 for data buses using parallel data transfer.

B) Series SN 488 for the General Purpose Interface Bus (GPIB or IEEE-488). The SN 488 implements the AH1 (Acceptor Handshake) and the L1 (Listener) as well as the Listener–Only function.

MODEL	NUMBER OF CHANNELS	INPUT CODING	RESOLUTION
SN 488-121	ONE	BINARY	12 BIT
SN 488-122	TWO	BINARY	12 BIT
SN 488-031	ONE	BCD	3-DIGIT
SN 488-032	TWO	BCD	3-DIGIT
SN 500-121	ONE	BINARY	12 BIT
SN 500-122	TWO	BINARY	12 BIT
SN 500-031	ONE	BCD	3-DIGIT
SN 500-032	TWO	BCD	3-DIGIT

TABLE 1-1 KEPCO SN 488 AND SN 500 DIGITAL PROGRAMMERS

1-6 All SN models as listed in Table 1-1, have the following common features:

A) OPTICAL ISOLATION: Digital and analog grounds can be separated by a maximum of 1000 volts.

B) SINGLE OR DUAL CHANNEL OPERATION: SN models for single or dual control channel operation may be selected. Single channel SN models may be converted to dual channel operation by the addition of a printed circuit board (See Par. 1-10 "ACCESSORIES (NOT SUPPLIED)." On dual channel SN models, each channel is completely isolated from the other. The two channels can, therefore, drive independent instruments or two functions of the same instrument. On a Kepco ATE power supply, for example, the output voltage and the current limit, or the output current and the voltage limit can be programmed together with a two channel SN model. Digital addressing of the SN model selects one of the two control channels.

C) POLARITY AND RANGE. The analog output of the SN programmer is : 0 to (±)10V (high range) or 0 to (±)1V (low range). Both, polarity and range are selectable via digital input commands.

D) CODING AND RESOLUTION. All SN models are available with either 3-digit BCD or 12 bit binary input coding. Resolution for 3-digit BCD is one part in 999, for 12 bit binary it is one part in 2^{12}=4096.

E) TIMING:

1) Data Transfer Time:

SN 500 Series: Approximatley 35 microseconds. NOTE: Data must be present and stable during the STROBE pulse (2 microseconds minimum). Although the complete transfer requires 35 microseconds before the SN 500 Programmer can be strobed again, the DATA BUS can be used for other instruments or programmers following the end of the 2 microseconds STROBE pulse.

SN 488 Series: Approximatley 60 microseconds.

2) Data Transfer Rate: Determined by the data bus controller.

1-7 DATA FORM

SN 500 SERIES			SN 488 SERIES
DATA	:	12 bit	DATA FORM: NCVVV (ASCII)
RANGE, CHANNEL 1	:	1 bit	where: N = Channel select, 1 or 2
RANGE, CHANNEL 2	:	1 bit	C = Control character:
POLARITY, CHANNEL 1	:	1 bit	C = 0 POSITIVE OUTPUT, HIGH RANGE
POLARITY, CHANNEL 2	:	1 bit	C = 1 NEGATIVE OUTPUT, HIGH RANGE
STROBE	:	1 bit	C = 2 POSITIVE OUTPUT, LOW RANGE
CHANNEL SELECT	:	1 bit	C = 3 NEGATIVE OUTPUT, LOW RANGE
NOTE: Delete "RANGE, CHANNEL 2" and "POLARITY CHANNEL 2" for single channel models.			VVV = Channel field as a percentage of full scale, where "full scale" is ±10 volts in the HIGH RANGE and ±1 volt in the LOW RANGE. Channel field range for 12 bit binary SN numbers is "000" to "FFF" and "000" to "999" for BCD models.

1-8 SPECIFICATIONS: See Table 1-2.

MODELS		SN 488-				SN 500-			
		121	122	031	032	121	122	031	032
NUMBER OF CHANNELS		1	2	1	2	1	2	1	2
INPUT CODING	Binary	X	X			X	X		
	BCD			X	X			X	X
RESOLUTION	12 Bit	X	X			X	X		
	3 Digit			X	X			X	X
OUTPUT VOLTAGE	High Range	± 10V							
	Low Range	± 1V							
OUTPUT CURRENT		± 2 mA max.							
OUTPUT IMPEDANCE		<0.05 ohms							
LINEARITY ERROR 0 to +70°C		± 1/2 LSB							
TEMPERATURE COEFFICIENT	Full Scale	± 35 PPM/°C max.							
	Zero High Range	± 20 μV/°C max.							
	Zero Low Range	± 10 μV/°C max.							
LOGIC INPUT		TTL COMPATIBLE							
DIGITAL INPUT FORMAT		BYTE SERIAL BIT PARALLEL				PARALLEL			
INTERFACE FUNCTIONS IMPLEMENTED		AH1, L1				—			
A-C INPUT	Voltage	105-125V/210-250V SELECTABLE BY SWITCH							
	Frequency	50-440 MHz							
	Power	≈ 12 VA							

TABLE 1-2 SPECIFICATIONS, SN 500 AND SN 488 MODELS.

1-9 ACCESSORIES (SUPPLIED):

A) A-C LINE CORD, removable.

B) ANALOG OUTPUT CONNECTOR, KEPCO P/N 143-0303.

C) DIGITAL INPUT CONNECTOR, KEPCO MODEL PC-12, for SN 500 models only.

1-10 ACCESSORIES (NOT SUPPLIED):

A) KEPCO MODEL SN 612, 12 bit binary add-on channel on a printed circuit board.

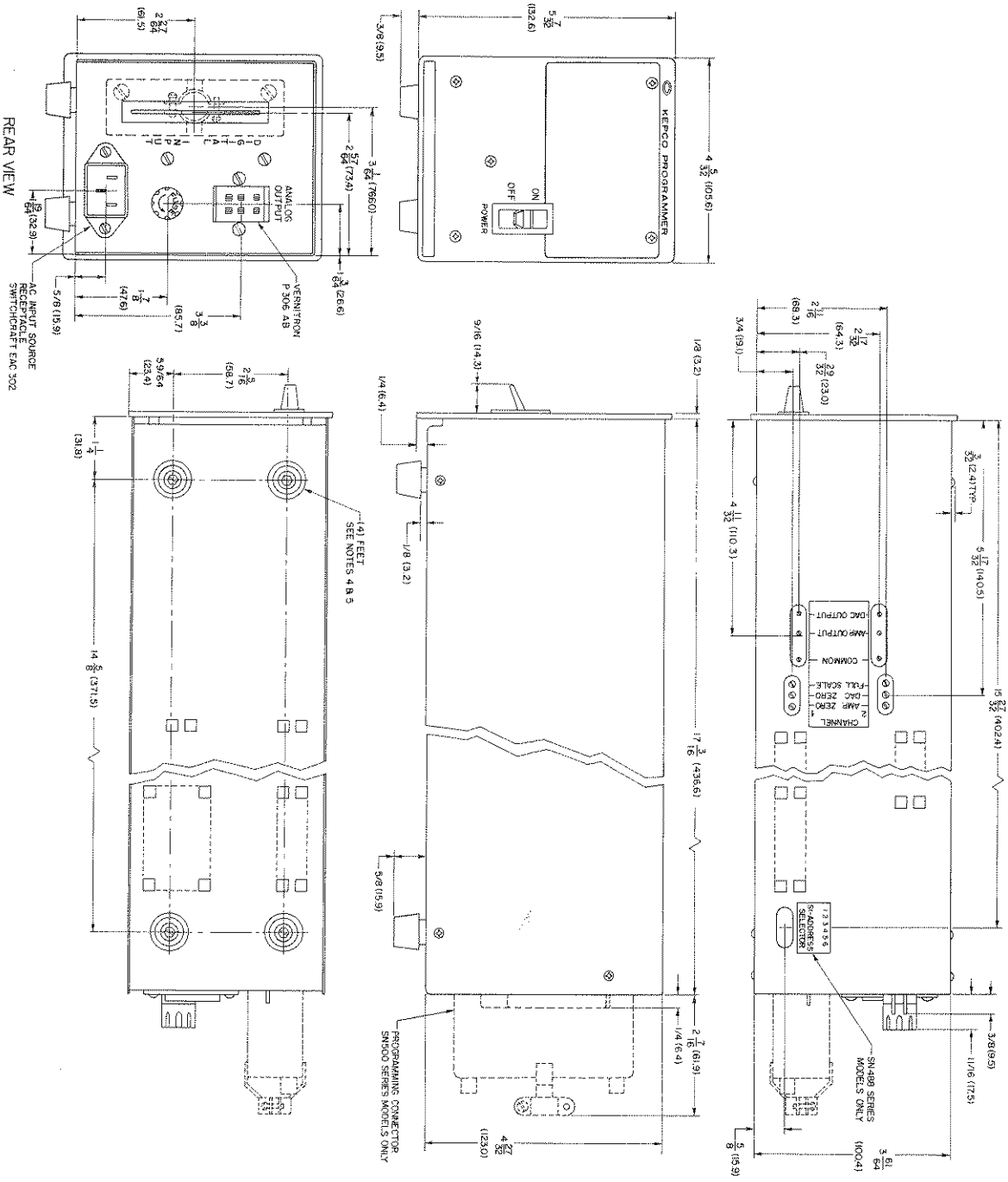
B) KEPCO MODEL SN 603, 3-digit BCD add-on channel on a printed circuit board.

NOTE: Kepco Models SN 612 and SN 603 convert any single channel SN 500 or SN 488 to the corresponding two-channel model.

C) CONNECTING CABLE FOR SN 488 MODELS:

KEPCO MODEL SNQ 488-1 (1 meter long) and, KEPCO MODEL SNQ 488-2 (2 meter long). These cables connect the SN 488 models to the GPIB bus.

D) MOUNTING HARDWARE: Both, SN 500 and SN 488 models are built in Kepco's "QUARTER-RACK" package. All SN models can, therefore, be mounted in any Kepco mounting accessory, which accepts Kepco quarter-rack models (See Main Catalog).



NOTES:

1. THIS DRAWING IS USED FOR THE FOLLOWING MODELS: SN488-031, SN488-032, SN488-121, SN488-122, SN500-031, SN500-032, SN500-121, SN500-122.
2. MATERIAL:
   A: CHASSIS NO. 16 GA C.R.S.
   B: FRONT PANEL: 1/8 THICK ALUMINUM
   C: COVER: NO 20 GA C.R.S.
3. FINISH:
   A: CHASSIS: CADMIUM PLATE WITH CHROMATE WASH.
   B: FRONT PANEL: LIGHT GRAY PER FEDERAL STD 595, COLOR NO 26440.
   C: COVER: CHARCOAL GRAY VINYL TEXTURE.
4. RACK MOUNTING REMOVE (4) FEET FROM BOTTOM OF CHASSIS
5. (4) PLASTIC MOUNTING INSERT UNDER FEET, FOR 8-18 x 5/8 SELF-THREADING SCREWS. (WITH 1/8 THICK MOUNTING PLATE)
6. DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS
7. TOLERANCES:
   A- BETWEEN MOUNTING HOLES ± 1/64 (0.4)
   B- ALL FRONT PANEL DIMENSIONS TO MIL-STD-189. EXCEPT AS NOTED.
   C- ALL OTHERS DIMENSIONS ± 1/32 (0.8),

FIG. 1-3 MECHANICAL OUTLINE

SECTION II – INSTALLATION

2-1 UNPACKING AND INSPECTION

2-2 The Kepco SN Programmer has been inspected, tested and calibrated prior to packing, and is ready for installation and operation. Before installation, the SN Programmers should be inspected for shipping damage. If such damage is found, retain the shipping container and notify the responsible carrier.

2-3 TERMINATIONS: See Fig.'s 2-1 and 2-2.

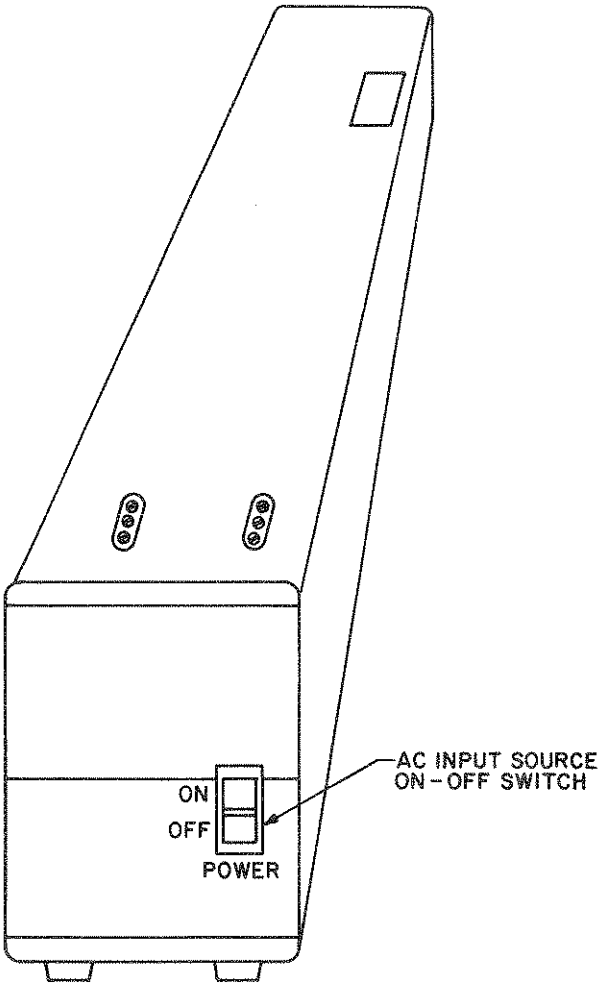


FIG. 2-1 FRONT PANEL, SN PROGRAMMER

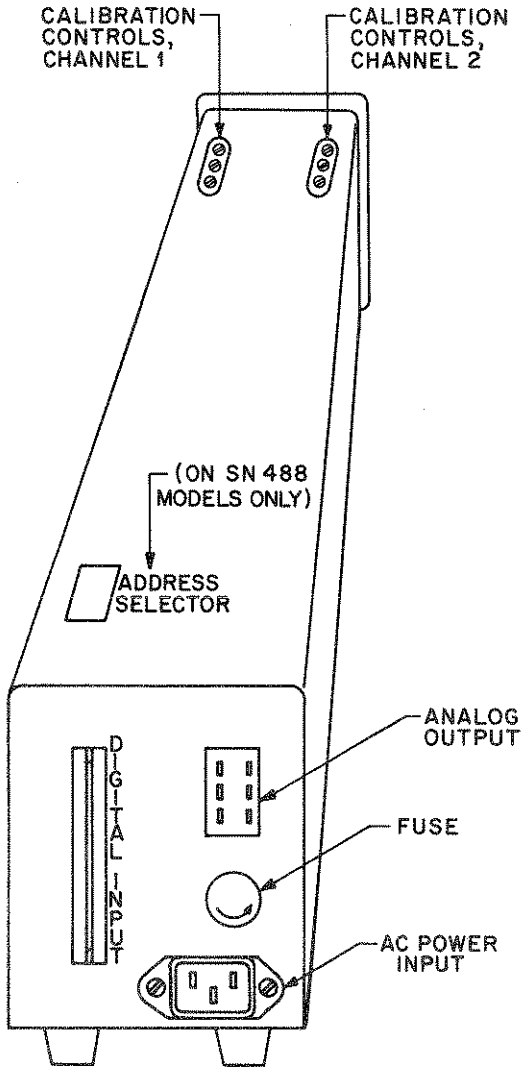


FIG. 2-2 SN PROGRAMMER, REAR

2-4 A-C SOURCE INPUT SELECTION

2-5 The Kepco SN Programmer is normally delivered for operation on a nominal 115V a-c source. For operation on a nominal 230V a-c source, proceed as follows:

1) Remove unit cover and transfer A-C SOURCE SELECTOR to the "230" position (See Fig. 2-3).

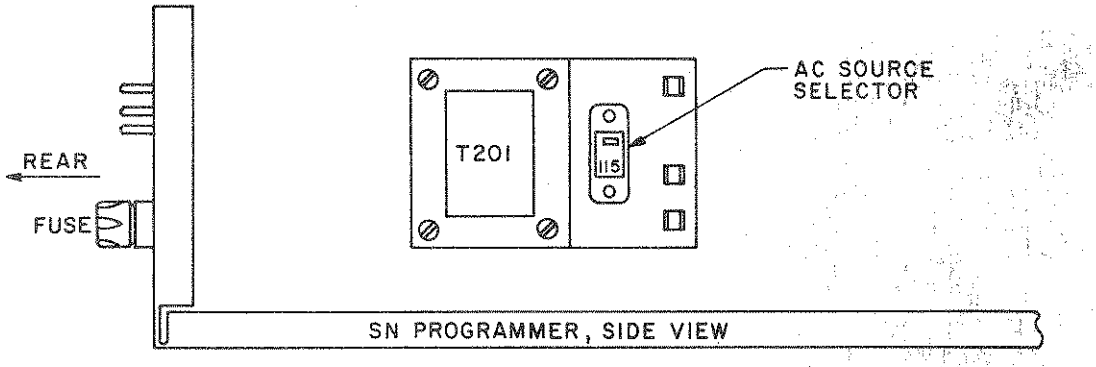


FIG. 2-3 A-C SOURCE VOLTAGE SELECTION

2) Exchange FUSE with one having one half the rating of the fuse used for 115V a-c service.

3) Re-install unit cover.

2-6 COOLING

2-7 Power dissipating components in the SN Programmer are cooled by convection. *Bottom and side panel openings must be kept clear from obstructions to insure proper air circulation.*

2-8 Periodic cleaning of the cabinet's inside is recommended. If the cabinet is mounted into confined spaces (rack installations, etc.) care must be taken that the surrounding temperature does not exceed 70°C.

2-9 INSTALLATION

2-10 The SN Programmer may be operated on the bench or may be installed into any Kepco rack mount, suitable for quarter-rack models. For rack mounting, the four bottom feet must be removed, and the four remaining plastic spacers plus the self-threading screws, which formerly held the bottom feet, are used to mount the SN Programmer into the rack mount.

SECTION III – OPERATION

3-1 GENERAL

3-2 Operation of the Kepco SN DIGITAL PROGRAMMER requires the following steps:

1) Connect the SN Programmer to the a-c power source (See Section II, Par. 2-4).

2) Connect the DIGITAL INPUT of the SN Programmer to the Data Bus (See Par.'s 3-3 to 3-8).

3) Connect the ANALOG OUTPUT of the SN Programmer to the power supply to be programmed (See Par.'s 3-8 to 3-16).

4) Establish the digital program to be transmitted via the Data Bus to the SN Programmer (See Par.'s 3-17 to 3-20).

These steps are discussed in detail in the following paragraphs.

3-3 DIGITAL INPUT DESCRIPTION, SN 500 SERIES

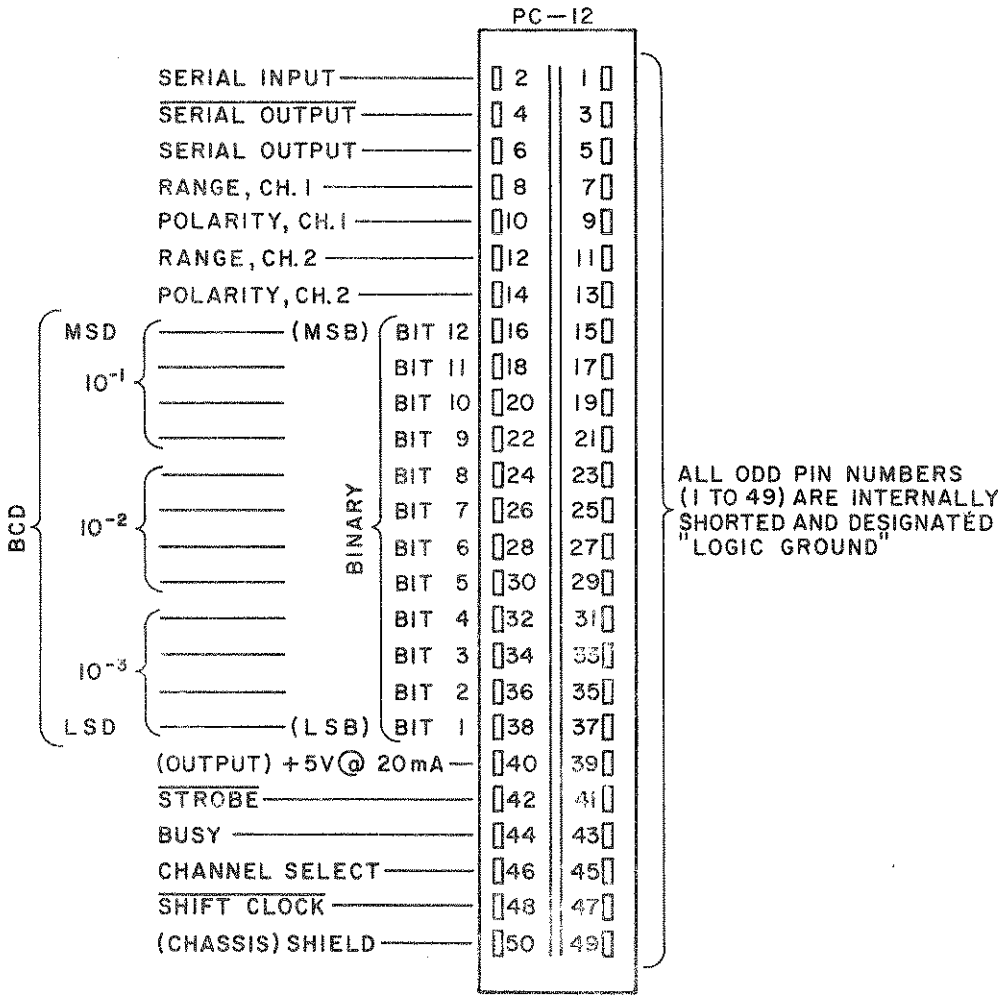


FIG. 3-1 DIGITAL INPUT CONNECTOR (PC-12) FOR SN 500 SERIES

3-3 DIGITAL INPUT DESCRIPTION (CONT'D)

A) PIN 2 — SERIAL INPUT
PIN 4 — $\overline{\text{SERIAL OUTPUT}}$
PIN 6 — SERIAL OUTPUT

WIRE JUMPER FOR NEGATIVE LOGIC

WIRE JUMPER FOR POSITIVE LOGIC (SUPPLIED)

Pins 2, 4, and 6 serve to select either POSITIVE LOGIC (L=0, H=1) by placing the jumper from pin 2 to pin 6, or NEGATIVE LOGIC (L=1, H=0), by placing the jumper from pin 2 to pin 4. The SERIAL OUTPUT may also be used for other purposes and may be synchronized by means of the $\overline{\text{SHIFT CLOCK}}$ output.

B)

PIN 8	— RANGE, CHANNEL 1	L= HIGH RANGE (0-10V)	H= LOW RANGE (0-1V)
PIN 10	— POLARITY, CHANNEL 1	L= POSITIVE OUTPUT	H= NEGATIVE OUTPUT
PIN 12	— RANGE, CHANNEL 2	L= HIGH RANGE (0-10V)	H= LOW RANGE (0-1V)
PIN 14	— POLARITY, CHANNEL 2	L= POSITIVE OUTPUT	H= NEGATIVE OUTPUT

All four RANGE and POLARITY selection terminations have been provided for manual preselection of range and polarities on both channels. If RANGE and POLARITY are machine controlled, only pins 8 and 10 are needed, since a CHANNEL SELECTOR command is required to preselect each channel. Note: Pin 12 should be connected to pin 8 while pin 14 should be connected to pin 10. If, however, the application calls for fixed polarity and range, the appropriate pins can be hardwired according to the requirements.

C) PARALLEL DATA INPUT PINS:

PINS:	16	18	20	22	24	26	28	30	32	34	36	38
BITS:	12 MSB	11	10	9	8	7	6	5	4	3	2	1 LSB
DECADE	10^{-1}				10^{-2}				10^{-3}			
BCD	8	4	2	1	8	4	2	1	8	4	2	1

D) PIN 40 D-C LOGIC SUPPLY OUTPUT, 5V at 20mA maximum. May be used to connect pull-up resistors for establishing pre-wired logic states or to drive external logic within the given ratings.

E) PIN 42—$\overline{\text{STROBE}}$. The negative going edge of the strobe signal (H → L) enables the loading of the Temporary Storage Registers with the data presented on the data pins. The minimum duration of $\overline{\text{STROBE}}$ must be 2 μsec.

F) PIN 44—BUSY (H = busy, L = not busy). This output delivers a status signal to the bus. On the first clock transition (H → L), following the STROBE signal, the BUSY line goes high (H) and remains high until the first clock transition (H → L) following data transfer (approximately 35 μsec), indicating the SN 500 is ready to accept new data.

G) PIN 46—CHANNEL SELECT (H → CHANNEL 1, L= CHANNEL 2).

H) PIN 48—$\overline{\text{SHIFT CLOCK}}$. This output is used to synchronize the SERIAL OUTPUT.

J) PIN 50—SHIELD (CHASSIS). Chassis and Case connection of the SN 500.

K) PINS 1 thru 49 (Odd No.'s): LOGIC GROUND.

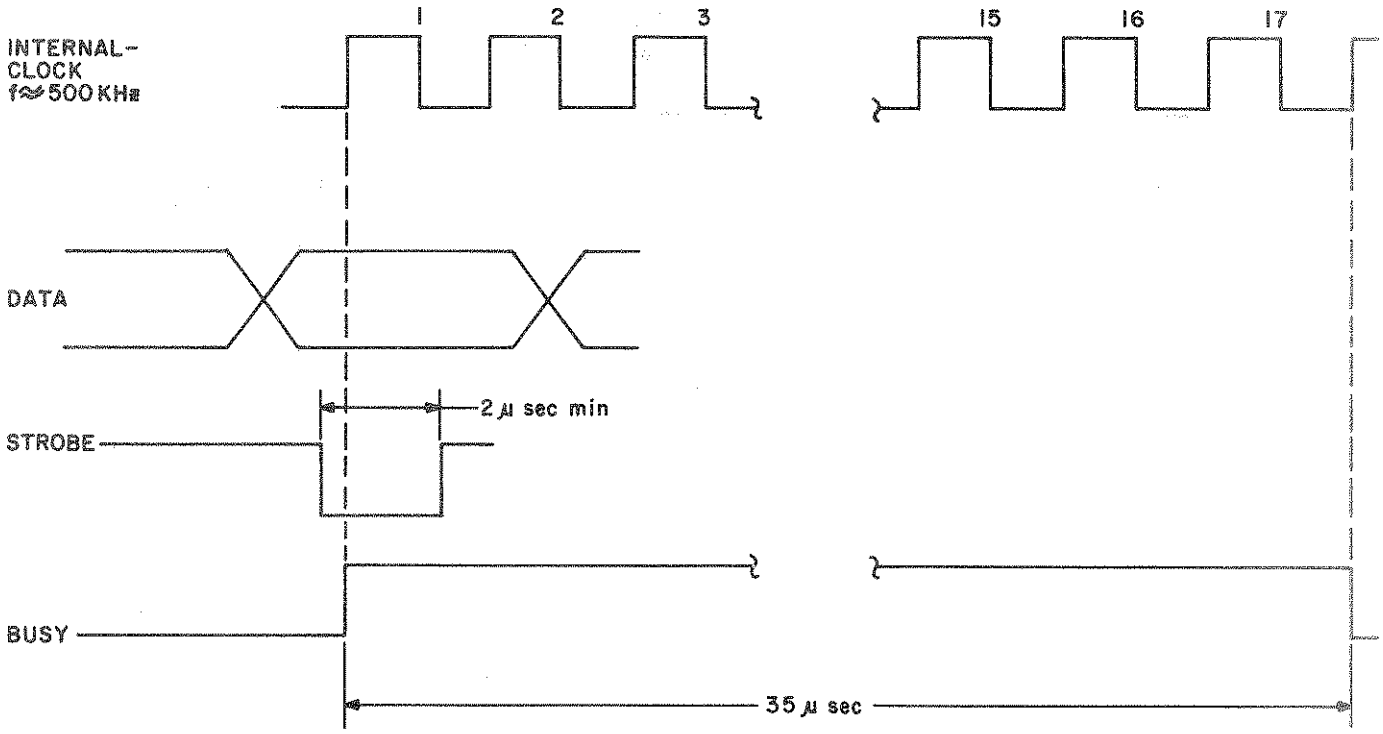


FIG. 3-2 TIMING DIAGRAM, SN 500 SERIES

3-4 DIGITAL INPUT DESCRIPTION, SN 488 SERIES

3-5 The Kepco SN 488 Series of Digital Programmers are designed to operate on the GPIB (IEEE 488) bus. Once the programmer address is (manually) set as described below (Refer to Par. 3-6), the SN 488 Programmer is connected, by means of the digital input cable (Kepco Model SNQ 488-1 or -2) to the GPIB bus. Data rate, input commands, and timing are determined by the GPIB bus protocol and are, therefore, not described here (See ANSI MC1.1–1975 or IEEE 488–1975).

3-6 SETTING THE SN 488 PROGRAMMER ADDRESS. Remove the cover, and locate the Address Selector Switch (S1) on the printed circuit board (A1). Set switch positions according to the selected address (See Table 3-1).

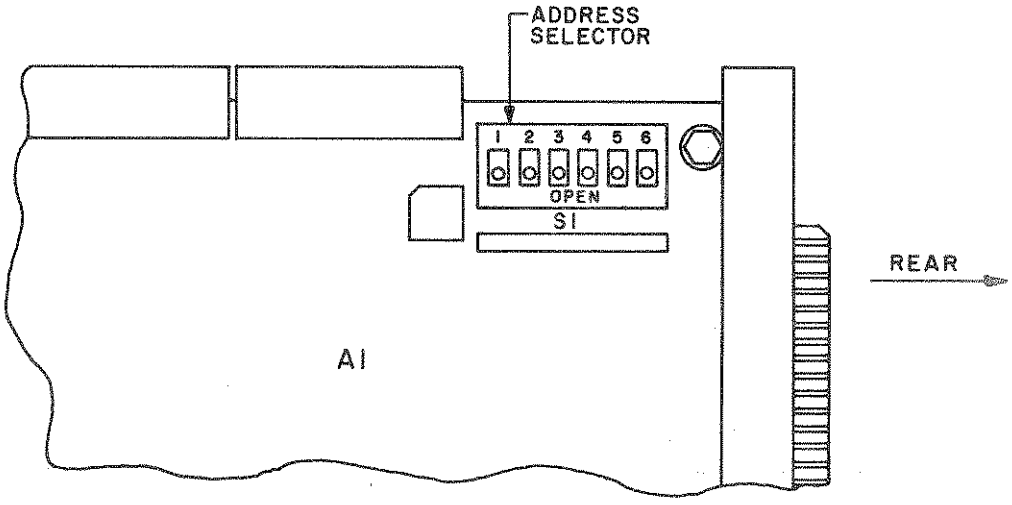


FIG. 3-3 LOCATION OF ADDRESS SELECTOR SWITCH

NOTE: The address selector switch (S1) is a miniature multiple rocker switch with positions S1-1 thru S1-6.

SWITCH POSITIONS ON ADDRESS SELECTOR SWITCH (S1)

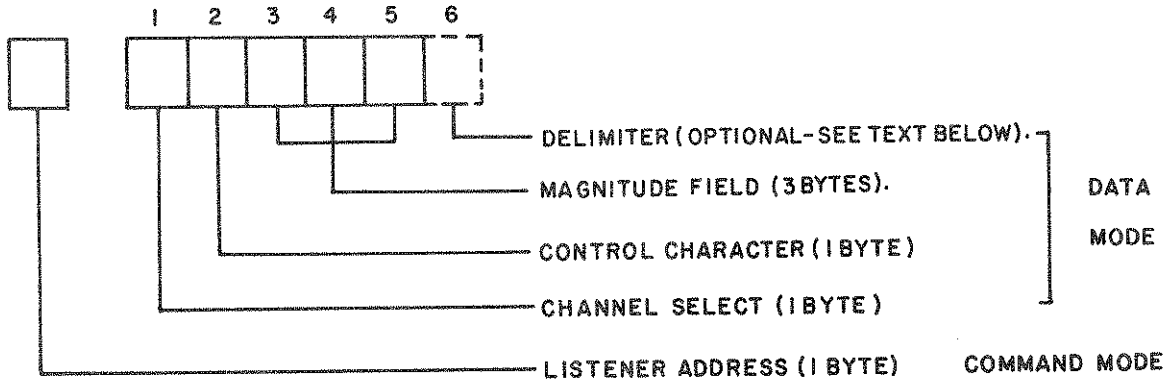
ASCII CHARACTER	DECIMAL ADDRESS	SI-1	SI-2	SI-3	SI-4	SI-5	LISTEN ONLY SI-6
NOT APPLICABLE		X	X	X	X	X	0
SP	0	0	0	0	0	0	1
!	1	1	0	0	0	0	1
"	2	0	1	0	0	0	1
#	3	1	1	0	0	0	1
$	4	0	0	1	0	0	1
%	5	1	0	1	0	0	1
&	6	0	1	1	0	0	1
'	7	1	1	1	0	0	1
(	8	0	0	0	1	0	1
)	9	1	0	0	1	0	1
*	10	0	1	0	1	0	1
+	11	1	1	0	1	0	1
,	12	0	0	1	1	0	1
–	13	1	0	1	1	0	1
.	14	0	1	1	1	0	1
/	15	1	1	1	1	0	1
0	16	0	0	0	0	1	1
1	17	1	0	0	0	1	1
2	18	0	1	0	0	1	1
3	19	1	1	0	0	1	1
4	20	0	0	1	0	1	1
5	21	1	0	1	0	1	1
6	22	0	1	1	0	1	1
7	23	1	1	1	0	1	1
8	24	0	0	0	1	1	1
9	25	1	0	0	1	1	1
:	26	0	1	0	1	1	1
;	27	1	1	0	1	1	1
<	28	0	0	1	1	1	1
=	29	1	0	1	1	1	1
>	30	0	1	1	1	1	1

X = DON'T CARE
0 = ON (SWITCH CLOSED)
1 = OFF (SWITCH OPEN)

PROGRAMMING NOTE:
The *complete* ASCII character (7-bits) must be programmed.

TABLE 3-1 LISTENING ADDRESS SELECTION ON THE KEPCO SN 488 SERIES

3-7 INPUT FORMAT, SN 488 SERIES. Once the address of the SN 488 Programmer is set as described in Par. 3-6, and the programmer is connected to the the GIPB bus, operation can proceed. The SN 488 Programmer requires the following commands and data sequence from the CONTROLLER:



3-8 Once the SN 488 Programmer is addressed by the LISTENER ADDRESS command, five (5) consecutive data bytes are needed to complete a program for one channel. Multiple channel program instructions may be strung together without a delimiter character. If, however, after five (5) consecutive data bytes, the bus should go immediately into the COMMAND MODE, a delimiter byte is required. This delimiter byte can be a CR (Carriage Return), LF (Line Feed) or a "," (Comma). Alternately, a delay of at least 30 microseconds should be imposed upon the Controller prior to changing the ATTENTION LINE (ATN) to the low (true) state. Address and instructions are all ASCII characters. The five program bytes are defined as follows:

ASCII CHARACTER	RANGE	OUTPUT POLARITY
0	HIGH	POSITIVE
1	HIGH	NEGATIVE
2	LOW	POSITIVE
3	LOW	NEGATIVE

BYTE 3, 4, 5: MAGNITUDE FIELD OF THE SELECTED CHANNEL

The magnitude field is coded as follows:

A) For BCD models, the magnitude field bytes must be ASCII characters in the range from 0 to 9. The maximum magnitude field coding is, therefore, 999 representing an analog output voltage of (±) 10 volts or (±) 1 volt, depending on the coding for range and polarity selection.

B) For 12 bit models, the magnitude field bytes must be ASCII characters in the range from 0 to 9 or A to F. The maximum magnitude field coding is, therefore, FFF representing an analog output voltage of (±) 10 volts or (±) 1 volt, depending on the coding for range and polarity selection.

3-9 CONNECTIONS BETWEEN SN PROGRAMMER AND THE POWER SUPPLY TO BE PROGRAMMED.

3-10 The analog output signal of the SN programmer is terminated at the rear of the unit by means of a 6 PIN plug (P202), as shown in Fig. 3-4.

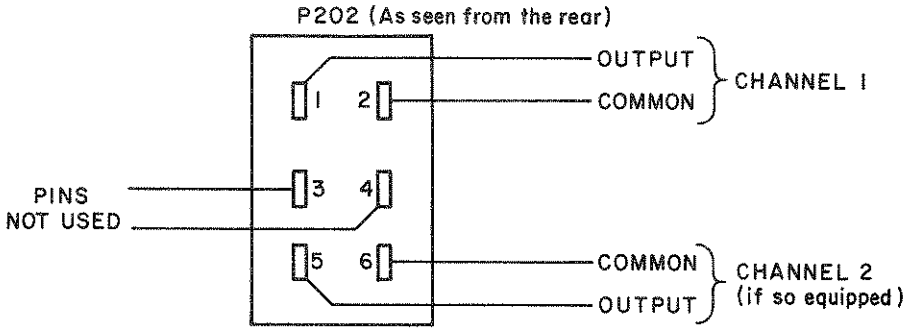


FIG. 3-4 ANALOG OUTPUT, SN 500/SN 488 PROGRAMMERS

3-11 The analog output voltage from the SN Programmer serves as the control voltage for the connected power supply. A wide variety of Kepco Power Supplies can be controlled by the SN Programmer (Refer to Table 3-2). As seen from the table, some Kepco Power Supply Models can be controlled directly by the analog voltage output of the SN Programmer, while for others the SN output voltage is converted to a control current, simply by placing an appropriate resistor in series. On many Kepco Power Supply Models, the output voltage and output current can be controlled together (by means of a two-channel SN Programmer), while on others only single channel control can be excercised (Output Voltage *or* Output Current). Several basic interconnections between Kepco Power Supplies and SN Programmers are described on the following pages. The diagrams shown are simplified representations of Kepco Power Supplies. Coupling resistors and control positions where chosen to produce from zero to maximum rated output voltage or current in response to the SN Programmer analog outputs of 0 to 10 volt or 0 to 1 volt. The circuits may be scaled to any desired programming voltage/power supply output ratio. Detailed information for each Kepco Power Supply Model is contained in the power supply's instruction manual.

NOTE: EITHER SIDE OF THE POWER SUPPLY OUTPUT MAY BE GROUNDED.

3-12 The table below (See Table 3-2) lists the major groups of Kepco programmable power supplies, suitable for operation with the Kepco SN Programmers. From the table, the connection requirements can be quickly determined. For special requirements, please consult your Kepco Representative, or the Kepco Application Engineering Department, Flushing, New York.

KEPCO MODEL GROUP	PROGRAMMING SIGNAL FOR FULL OUTPUT		CONNECTIONS REQUIRED	
	VOLTAGE CONTROL	CURRENT CONTROL	VOLTAGE CONTROL	CURRENT CONTROL
* APH(1)	0–5V	0–1V	DIRECT CONNECTIONS	
ATE(1)	0–10V	0–1V	DIRECT CONNECTIONS	
* BHK(1)	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-7
BOP	0–1 mA	0–1V/0–0.5V(2)	See FIG. 3-5	See FIG. 3-6
BOP HIGH VOLTAGE(1)	0–10V	0–10V	DIRECT CONNECTIONS	
CC	N.A.	0–1 mA	N.A.	See FIG. 3-6
CCP	0–1 mA	0–1 mA	See FIG. 3-5	See FIG. 3-6
JQE	0–1 mA	0–1V/0–0.5V(2)	See FIG. 3-5	See FIG. 3-6
JMK(1)	0–1 mA	0–1V/0–0.5V(2)	See FIG. 3-5	See FIG. 3-7
OPS–I,II	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-6
OPS–III to VIII (1)	0–1 mA	0–1V/0–0.5V(2)	See FIG. 3-5	See FIG. 3-7
* OPS–X(1)	0–1 mA	0–1V/0–0.5V(2)	See FIG. 3-5	See FIG. 3-7
* OPS IX-B (1)	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-7
PAT	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-6
PCX	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-6
PTR(1)	0–1 mA	0–1V	See FIG. 3-5	See FIG. 3-7

N.A. – NOT APPLICABLE.

(1) – SIMULTANEOUS VOLTAGE/CURRENT CONTROL POSSIBLE.

(2) – MODELS WITH OUTPUT CURRENT TO 5 AMPERES: 1V.
– MODELS WITH OUTPUT CURRENT 5 A AND GREATER: 0.5V.

* – FOR ALL UNITS OVER 1000 VOLTS, THE POSITIVE OUTPUT TERMINAL MUST BE GROUNDED.

TABLE 3-2 KEPCO PROGRAMMABLE POWER SUPPLIES AND THEIR PROGRAMMING SIGNAL AND CONNECTION REQUIREMENTS.

3-13 OUTPUT VOLTAGE CONTROL. Many Kepco Power Supplies require a d-c control current of 0 to 1 mA for zero to maximum output in the voltage mode. This requirement is readily satisfied by connecting a series resistance of 10k ohm as shown in Fig. 3-5. THE RESISTOR SHOULD BE LOCATED AS CLOSE TO THE POWER SUPPLY "NULL JUNCTION" TERMINAL AS POSSIBLE.

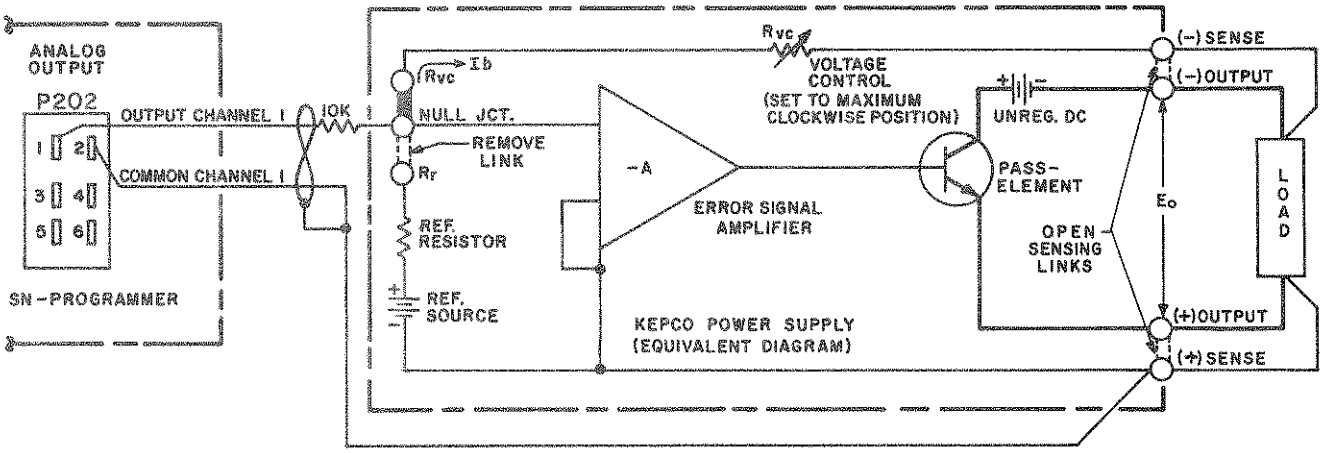


FIG. 3-5 OUTPUT VOLTAGE CONTROL WITH A TYPICAL KEPCO POWER SUPPLY AND THE SN PROGRAMMER

3-14 Certain precautions should be observed when making the interconnection between the KEPCO SN PROGRAMMER and the power supply:

1) The wiring from the programmer output to the power supply input should be tightly twisted and shielded to protect against static and magnetic "pick-up".

2) The wiring from the programmer output to the power supply input should be as short as possible if the series resistor (R_i = 10k ohm) is used as shown. If the input leads must be longer than a few inches, the input resistor should be placed close to the power supply's "Null Junction" terminal. Since the output from the KEPCO SN PROGRAMMER is (without the resistor) a low impedance line, noise "pick-up" is greatly reduced in this manner.

3-15 OUTPUT CURRENT CONTROL. Kepco Power Supplies designed as current stabilizers (CC and CCP groups for example) as well as many Kepco voltage stabilizers connected for external current sensing and control may be controlled by the method shown previously for output voltage control (See Par. 3-13). The illustration below (See Fig. 3-6) shows both cases. The component shown with dashed lines are added for current control with a voltage stabilized power supply. The previous remarks on interconnecting precautions (See Par. 3-14) are equally valid in this case.

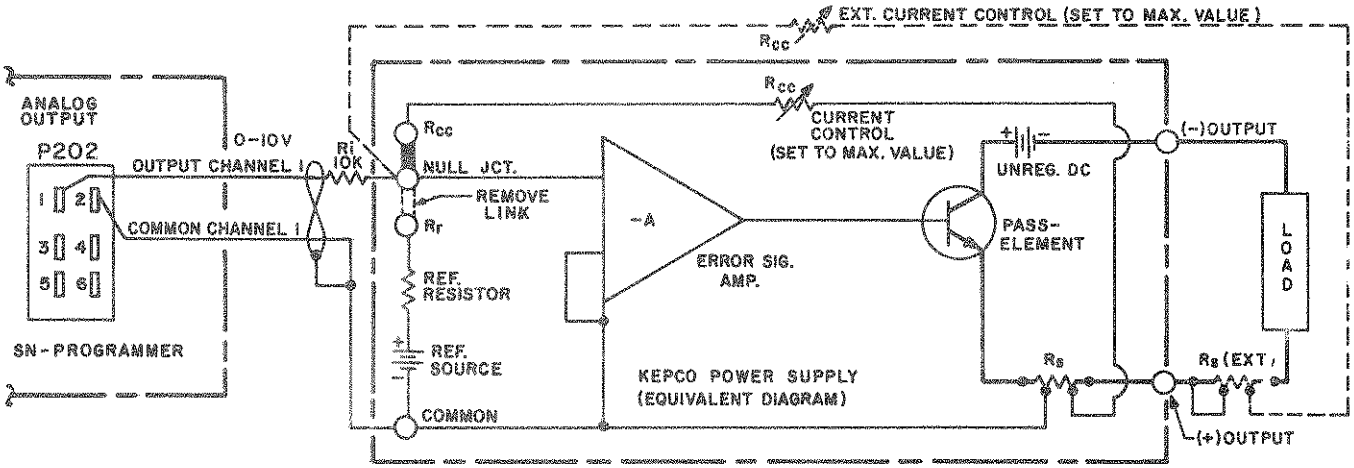


FIG. 3-6 OUTPUT CURRENT CONTROL USING A KEPCO CURRENT STABILIZED POWER SUPPLY OR A KEPCO VOLTAGE STABILIZED SUPPLY WITH EXTERNAL SENSING AND CONTROL RESISTOR (EXT. COMPONENTS, SHOWN WITH DASHED LINES).

3-16 COMBINED OUTPUT VOLTAGE/OUTPUT CURRENT CONTROL. For Kepco Power Supplies so identified in Table 3-3, a two-channel SN PROGRAMMER may be used to control voltage and current output together, as shown in Fig. 3-7.

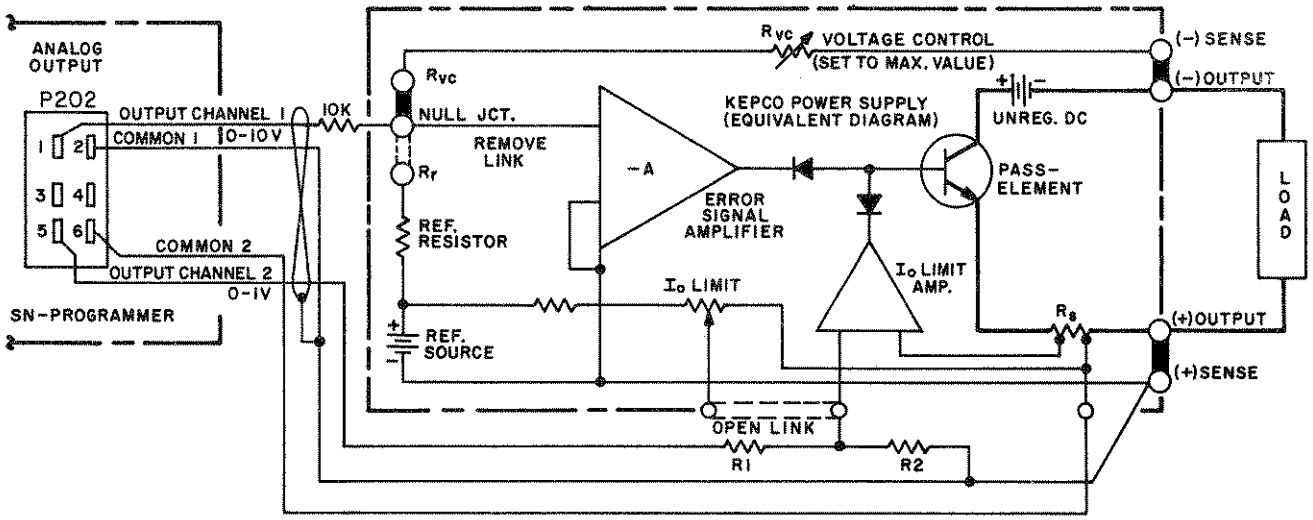


FIG. 3-7 COMBINED OUTPUT VOLTAGE/OUTPUT CURRENT CONTROL WITH A TYPICAL KEPCO POWER SUPPLY AND KEPCO 2-CHANNEL SN PROGRAMMER.

NOTE: On models requiring 0.5 volt current control voltage, a voltage divider, consisting of the two 500 ohm resistors (R1, R2) may be installed. System will yield 0 to full current output for 0–1 volt input from CHANNEL 2 INPUT.

3-17 SOME CODING EXAMPLES

3-18 SN 500-BCD MODELS. Example: The output voltage of a Kepco Model JQE 100–1M is to be controlled in the range from zero to 50 volts by means of a Kepco Model SN 500-031 Digital Programmer.

A) According to Table 3-2, the interconnections between the SN programmer and the JQE are shown in Fig. 3-5. The relevant terminal numbers on the JQE rear barrier strip can be found in the Operating Section of the JQE manual.

B) Reviewing the SN 500 input description (Par. 3-3) and the requirements of our example, we proceed as follows:

1) Selecting positive logic, a wire jumper is connected between pins 2 and 6 on the SN 500 DIGITAL INPUT CONNECTOR (PC-12).

2) Since we need the positive, high range output from the SN 500 (0 to +10 volts), pins 8 and 10 must be connected to logic ground (or permanent LOW must be transmitted by the controller).

3) Since the SN 500-031 is a single channel model no connection is required to pin 46: Interval pull-up resistor connects pin 46 to +5V (logic high, or a permanent HIGH must be transmitted by the controller).

4) Now the $\overline{\text{STROBE}}$ (Pins 42 on PC-12) and the BUSY line (Pin 44 on PC-12) as well as the PARALLEL DATA INPUT PINS (Pins 16 to 38 on PC-12) are wired to the data bus and operation can proceed.

C) The desired output voltage levels are coded according to the parallel data input description given in Par. 3-3C. A few examples are given in the table below ("FULL SCALE" or "FS", in our example, is the maximum JQE output voltage = 100V, produced from the SN 500 analog output of 10 volts).

PC-12 PINS:	16	18	20	22	24	26	28	30	32	34	36	38
DECADE	10^{-1}				10^{-2}				10^{-3}			
BCD	8	4	2	1	8	4	2	1	8	4	2	1
FS—1 LSB	1	1	1	1	1	1	1	1	1	1	1	1
1/2 FS	0	1	0	1	0	0	0	0	0	0	0	0
0V + 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1
0 VOLTS	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 3-3 CODING EXAMPLES, SN 500 BCD MODELS

To calculate the BCD coding for any intermediate power supply output voltage, the following expressions can be used:

$$\frac{999}{X} = \frac{E_O \text{ max.}}{E_O} \quad \text{or} \quad X = \text{INTEGER}\left(999 \times \frac{E_O}{E_O \text{ max.}}\right)$$

Where: 999 = Full Scale BCD Code
X = BCD Code for Intermediate Power Supply Output Voltage (E_O)
E_O max. = Maximum Power Supply Voltage
E_O = Required Intermediate Power Supply Output Voltage

If , for example, 40 volts output are required, the BCD code is:

$$X = \text{INTEGER}\left(999 \times \frac{40}{100}\right) = 399 \text{ (or 400).}$$

SN 500 12 BIT BINARY MODELS. Except for the output level coding, all other comments, made on the SN 500 BCD models apply (See Par. 3-17A thru B). The desired output voltage levels for the 12 bit binary models are coded according to the parallel data input description given in Par. 3-3C. A few examples are presented in the table below ("FULL SCALE" or "FS" is the maximum output voltage of the power supply, produced from the maximum analog output of the SN 500 (10 volts).

PC-12 PINS:	16	18	20	22	24	26	28	30	32	34	36	38
BITS	12 MSB	11	10	9	8	7	6	5	4	3	2	1 LSB
VALUE	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}
FS-1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	0	1	0	0	0	0	0	0	0	0	0	0
0 VOLTS	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 3-4 CODING EXAMPLES, SN 500 BINARY MODELS

To calculate the binary coding for any intermediate power supply output voltage, the following expressions can be used:

$$\frac{FFF}{X} = \frac{E_O \text{ max.}}{E_O} \text{ or } X = \text{INTEGER}\left(FFF \times \frac{E_O}{E_O \text{ max.}}\right)$$

Where:
- FFF = Full Scale Binary Code (HEXADECIMAL or BASE 16)
- X = Binary Code (HEX) for Intermediate Power Supply Voltage
- E_O max. = Maximum Power Supply Voltage
- E_O = Required Intermediate Power Supply Voltage

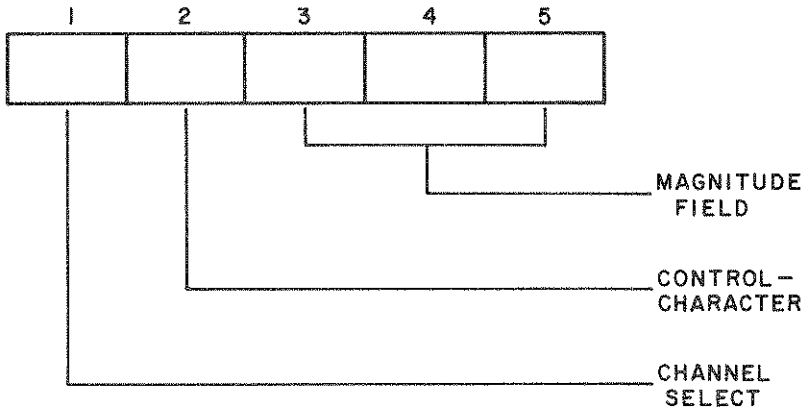
If, for example, 10 volts are required from a 50 volt power supply, the binary code is:

$$\frac{FFF_{16}}{X_{16}} = \frac{4096_{10}}{X_{10}} = \frac{50}{10}, \quad X \text{ (INTEGER)} = \frac{4096_{10}}{5} = 819.2_{10} = 333_{16}$$

3-20 SN 488 BCD MODELS. Example: The output voltage and the output current of a Kepco Model ATE 55–2M are to be controlled over their rated ranges by means of a Kepco Model SN 488-032 Digital Programmer:

A) According to Table 3-2, the interconnections between the SN Programmer and the ATE are "DIRECT CONNECTIONS," that is, the analog outputs of the SN 488 Programmer (channel 1 and channel 2) can be connected directly to the ATE rear programming connector (Refer to Section III of your ATE Instruction Manual).

B) Reviewing the SN 488 input description (Par. 3-6) and the requirements of our example, we proceed to code the five required consecutive instruction bytes as follows:



BYTE 1: Code ASCII "1", for VOLTAGE CONTROL.
Code ASCII "2", for CURRENT CONTROL.

BYTE 2: Code ASCII "0", when OPERATING ON CHANNEL 1 (0 to +10V).
Code ASCII "2", when OPERATING ON CHANNEL 2 (0 to +1V).

BYTE 3, 4, 5: To calculate the CHANNEL 1 (VOLTAGE) MAGNITUDE FIELD, use the expression:

$$999/X = E_O \text{ max.}/E_O$$

Where:
- 999 = Full Scale BCD Code
- X = BCD Code for Required Output Voltage (E_O)
- E_O max. = Maximum Power Supply Output Voltage
- E_O = Required Output Voltage

For the ATE 55–2M in the example given, the coding for an output of 30 volts would be:

$$\frac{55}{30} = \frac{999}{X}, \quad X \text{ (INTEGER)} = 544 \text{ (or } 545).$$

Bytes 3, 4, 5 would therefore be coded (ASCII) 545.

C) To calculate the Channel 2 (current) Magnitude Field, calculate the required coding using the expression:

$$999/X = I_O \text{ max.}/I_O$$

Where:
- 999 = Full Scale BCD Code
- X = BCD Code for Required Output Current
- I_O max. = Maximum Power Supply Output Current
- I_O = Required Output Current

For the example given, the coding for an output current of 0.5 Ampere would be:

$$2/0.5 = 999/X, \quad X \text{ (INTEGER)} = 249 \text{ (or } 250)$$

Bytes 3, 4, 5 would therefore be coded (ASCII) 250.

3-21 SN 488 12 BIT BINARY MODELS. Except for the MAGNITUDE FIELD CODING (BYTES 3, 4, 5) all other comments made about the SN 488 BCD models apply (See Par. 3-19A thru B). The desired output levels for the 12 bit binary models are coded using the expression:

$$\frac{FFF_{16}}{X_{16}} = \frac{E_O \text{ max.}}{E_O} \quad \text{For the Output Voltage Field}$$

AND

$$\frac{FFF_{16}}{X_{16}} = \frac{I_O \text{ max.}}{I_O} \quad \text{For the Output Current Field}$$

Where:
- FFF_{16} = Full Scale Binary Code (HEX)
- X_{16} = Binary Code (HEX) for Required Output (E_O or I_O)
- E_O, I_O = Required Output Quantity
- E_O max., I_O max. = Maximum Power Supply Output Quantities

A) For the given example parameters, the coding for an output voltage of 12 volts would be:

$$\frac{FFF_{16}}{X_{16}} = \frac{4096_{10}}{X_{10}} = \frac{55}{12}, \quad X_{10} \text{ (INTEGER)} = \frac{4096_{10}}{4.58} = 894_{10} = 37E_{16}$$

Bytes 3, 4, 5 would therefore be coded (ASCII) 37E.

B) For the given example parameters, the coding for an output current of 1.5 Ampere would be:

$$\frac{FFF_{16}}{X_{16}} = \frac{4096_{10}}{X_{10}} = \frac{2}{1.5}, \quad X_{10} \text{ (INTEGER)} = \frac{4096}{1.33} = 3080_{10} = CO8_{16}$$

3-22 SYSTEM CALIBRATION

3-23 ACCURACY. The digital power supply programming system, consisting of a controller or computer, the SN Digital Programmer, and the power supply to be programmed, must be carefully calibrated if optimum accuracy is expected.

WARNING

IF MEASUREMENTS AND/OR CALIBRATIONS ARE PERFORMED WITH THE POWER SUPPLY TO BE PROGRAMMED CONNECTED TO THE SN PROGRAMMER, STANDARD HIGH-VOLTAGE PRECAUTIONS MUST BE EXERCISED IF THE ANALOG COMMON OF THE PROGRAMMING SYSTEM IS OPERATED UNGROUNDED (FLOATING).

3-24 RESOLUTION. Since the SN Programmer is capable of resolving voltage steps in the order of magnitude of the output ripple of the power supply, the importance of carefully shielded leads from the analog output of the SN Programmer to the input of the power supply cannot be overstated. Perhaps just as important are the use of short twisted wires, from the power supply output terminals to the load. The power supply output ripple, especially in the current mode of operation, must be held as low as possible by the use of a good analog ground.

3-25 POWER SUPPLY CALIBRATION. Before connecting the power supply to be programmed to the digital programming system, its "zero output for zero input" should be carefully calibrated as described in the power supply instruction manual.

3-26 SN PROGRAMMER CALIBRATION. All Kepco SN Programmers are factory calibrated and system tested before delivery to the customer. If re-calibration should be required, the following procedure can be used:

A) EQUIPMENT REQUIRED:

1) SYSTEM CONTROLLER

2) D-C VOLTMETER, 0-10 volts, minimum accuracy ± 0.1%, minimum input impedance 1000 ohms per volt (MI).

NOTE: FOR OPTIMUM ACCURACY, ALLOW A WARM-UP TIME OF AT LEAST 15 MINUTES FOR THE CALIBRATION SET-UP.

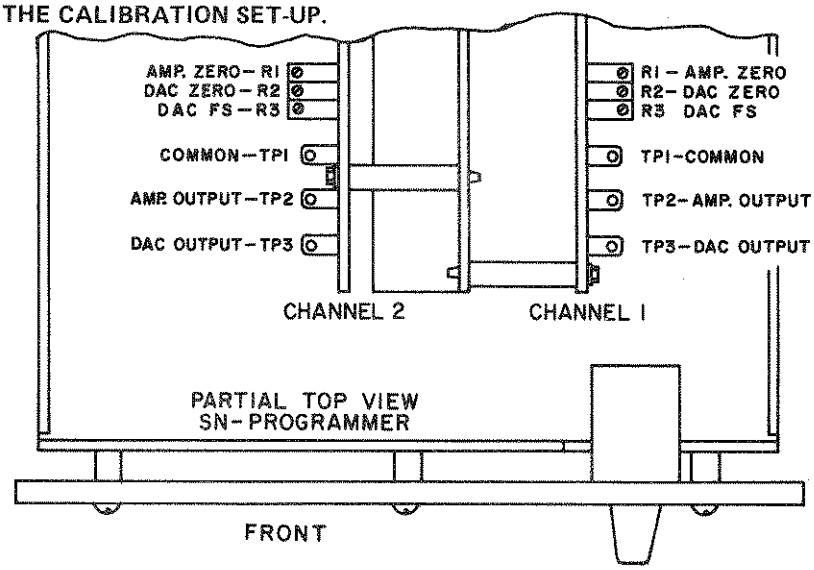


FIG. 3-8 LOCATION OF TEST POINTS AND CALIBRATION CONTROLS, SN 488 AND SN 500 DIGITAL PROGRAMMERS

B) Refer to Fig. 3-8 for the location of TEST POINTS and CALIBRATION CONTROLS. Proceed as directed on the FLOW-CHART, Fig. 3-9 and Fig. 3-10.

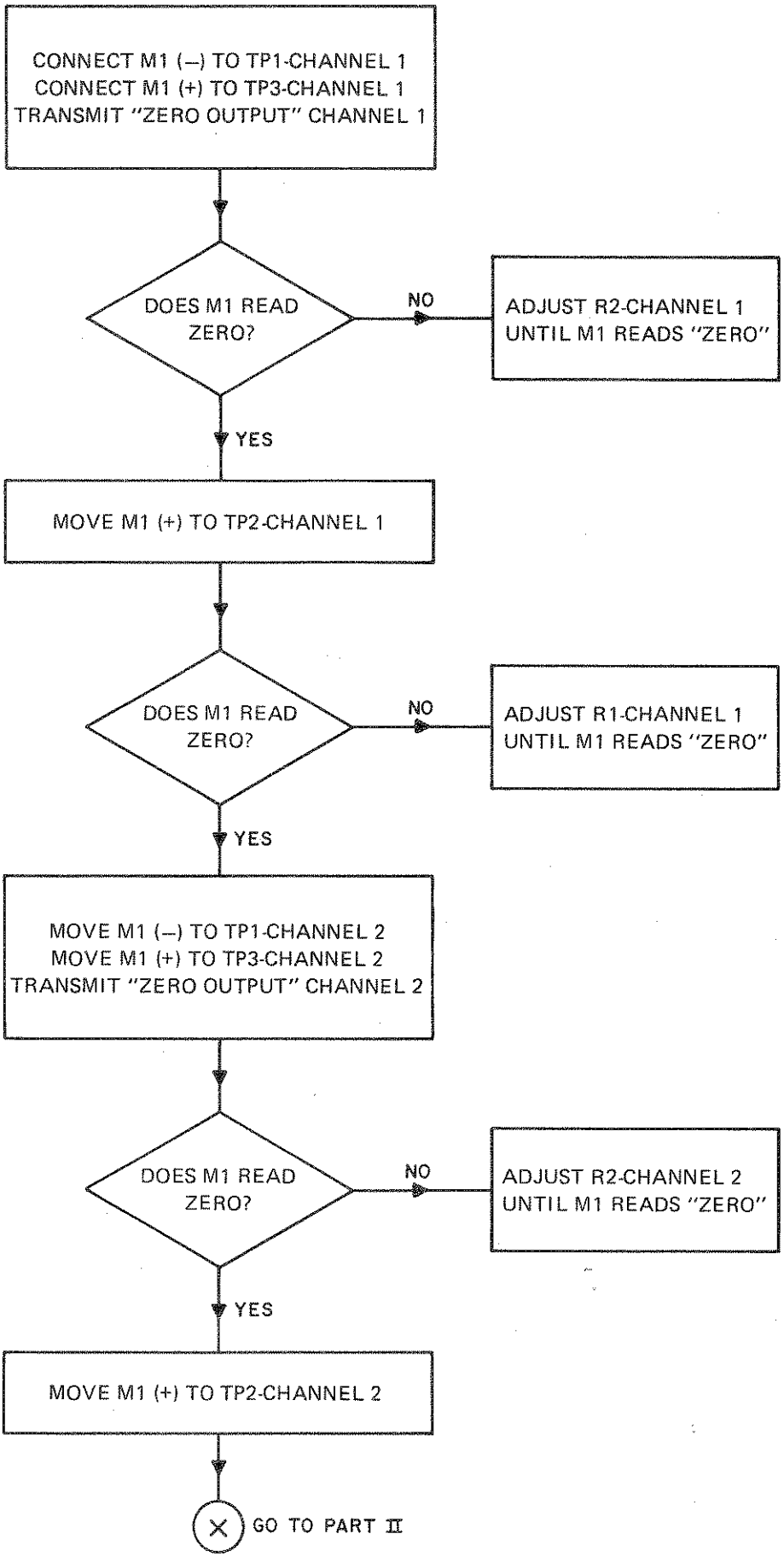


FIG. 3-9 CALIBRATION FLOW-CHART, PART I

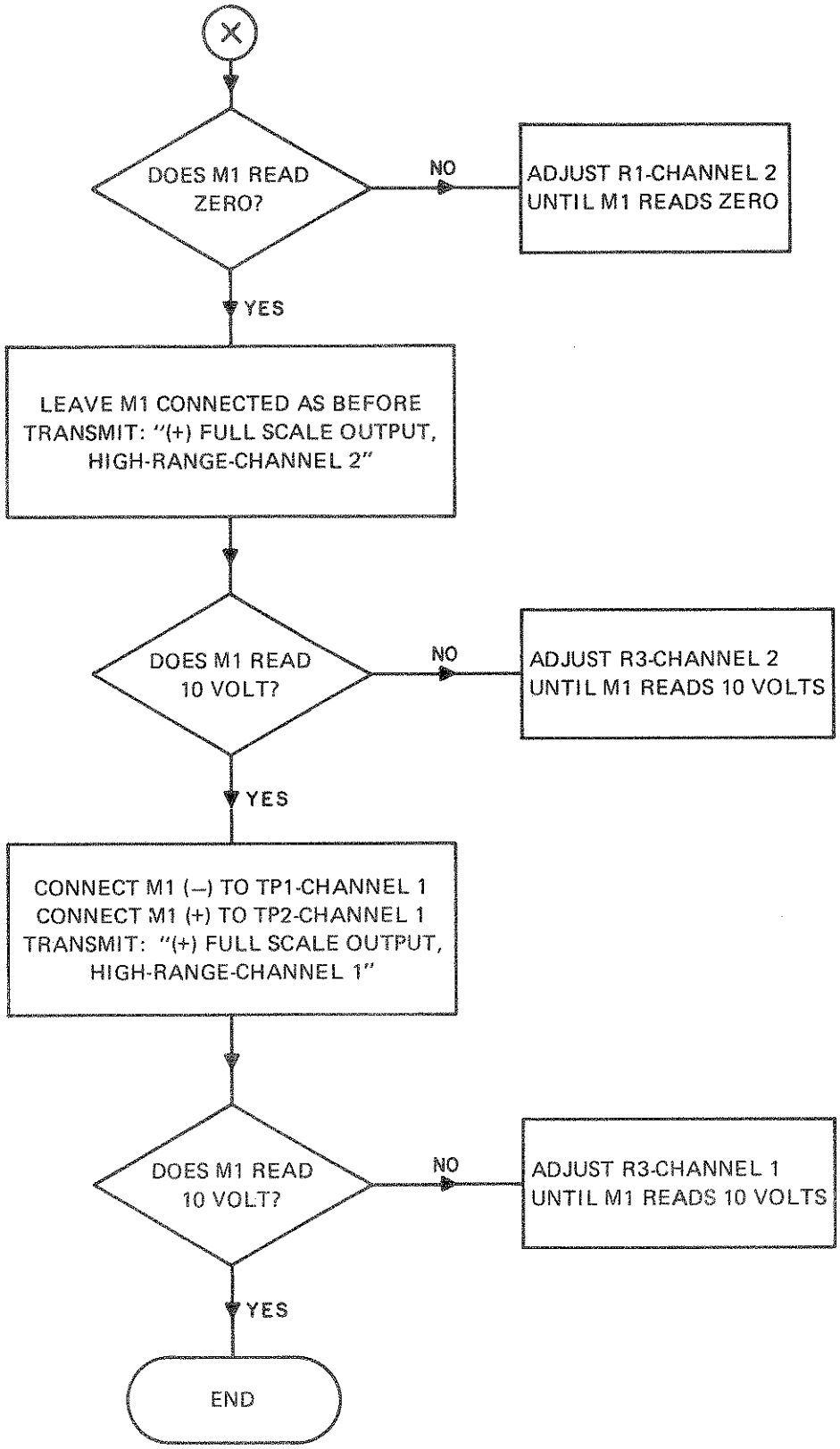


FIG. 3-10 CALIBRATION FLOW-CHART, PART II

SECTION IV – THEORY OF OPERATION

4-1 GENERAL

4-2 The Kepco Series 488 and Series 500 Digital Programmers are self-powered interface devices, operating between a digital controller and a programmable d-c power supply, enabling the latter to change its output in response to digital code from the controller. The difference between the Series 488 and Series 500 Programmers lies in their digital bus interface circuit. While the Series 500 is suitable for data buses using bit-parallel transfer, the Series 488 accepts serial data and is compatible with the General Interface Bus (GPIB, IEEE 488). The digital front end of both, the Series 488 as well as that of the Series 500 Digital Programmers, is isolated from the analog output circuits by an optical isolator providing up to 1000 volts of isolation between the digital input and the analog output circuits.

4-2 DIGITAL FRONT-END, SERIES 488 (REFER TO FIG. 4-1)

4-3 BUS INTERFACE CIRCUITRY. The Kepco Series 488 Digital Programmer is connected to the General Interface Bus (GPIB, IEEE 488) by means of a 16 wire, passive interconnecting cable. The 16 signal lines on the bus are divided into three functional groups as follows:

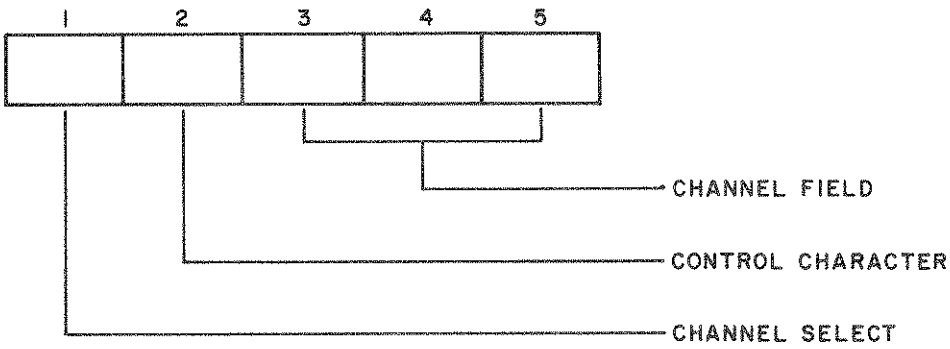
1) Eight DATA lines carry coded messages and/or data in bit-parrallel, byte-serial from a TALKER to one or more LISTENERS. Data flow on the bus is bi-directional and asynchronous, ensuring compatibility among devices with varing response times. Asynchronous transmission is accomplished by means of the DATA BYTE TRANSFER CONTROL LINES, described in Par. 4-3(2). Normally a 7-bit ASCII Code (American Standard Code for Information Interchange) is used for all messages.

2) Three DATA BYTE TRANSFER CONTROL ("Handshake") lines are used to effect the asynchronous transfer of all coded data bytes on the DATA lines.

3) Five GENERAL INTERFACE MANAGEMENT lines are used to control the orderly information flow on the bus. The Kepco Series 488 Programmer, as a LISTENER, is concerned only with the ATN line and the IFC line.

4-4 The BUS INTERFACE CIRCUIT, in the Kepco Series 488 Programmer implements the function of a LISTENER, as defined by the IEEE 488 Standard. The three groups of bus-connected signal lines are shown on the left side of Fig. 4-1, while the outgoing HEX DATA and BYTE COUNT lines are shown leaving the BUS INTERFACE and entering the DIGITAL PROCESSING CIRCUITRY in the center of Fig. 4-1.

4-5 Once the ATN (Attention) line on the GPIB goes true (low), the bus enters the command Mode. The BUS INTERFACE CIRCUIT of the Kepco SN 488 Programmer responds with the "handshake" protocol and receives the first byte of information on the DATA LINES, responding again (as on each of the following bytes) with the "handshake" protocol. If the first byte was the SN 488 Programmer address, as manually preset on the ADDRESS SELECT SWITCHES, the LISTEN MODE Flip-Flop is SET and the BUS INTERFACE CIRCUIT assumes the LADS (Listener Addressed) state. If the ATN (ATTENTION) line on the GPIB goes false (HIGH), the bus enters the data mode and the following (five) data bytes are accepted, by the SN 488 (See Fig. below), converted to HEX data, and deposited in memory (RAM). After the fifth data byte is completed, the NFRD (Not Ready For Data) line is held true (low) until completion of the internal transfer period, after which the "handshake" protocol is completed, indicating to the bus controller that new data can be accepted again. The internal data transfer is described in the following paragraph.



4-6 The DIGITAL DATA TRANSFER CIRCUIT in the Kepco Series 488 Programmer handles the internal data transfer from the BUS INTERFACE CIRCUIT to the ANALOG OUTPUT CIRCUIT. After the count for the five incoming data bytes is completed, the HEX-FF counter starts a 14-bit count, transmitting one bit at a time as follows: The two lower bit content of the second byte (CONTROL CHARACTER) and the four bit content of the following three bytes (12-bit DATA). The first byte (CHANNEL SELECT) is immediately processed in the CHANNEL SELECT Flip-Flop so that the subsequent data bytes are later transmitted to either Channel 1 or, (on Kepco 488 Programmers with dual channels) to Channel 2. After all fourteen data bits have been transfered, the HEX-FF is reset, the NRFD and NDAC lines change states, signaling to the GPIB "ready for new data."

4-7 ANALOG OUTPUT CIRCUIT

4-8 The ANALOG OUTPUT CIRCUIT is identical for both the Kepco 488 Series and the Kepco 500 Series of single channel programmers. On these programmers, the ANALOG OUTPUT CIRCUIT is located together with the BUS INTERFACE and the DIGITAL DATA PROCESSING CIRCUIT on the common printed circuit card. On two-channel programmers, the Channel 2 ANALOG OUTPUT CIRCUIT is located on a separate printed circuit card and carries a separate model designation (see Section I).

4-9 The ANALOG OUTPUT CIRCUIT is isolated from the digital front-end of the digital programmer by means of an OPTICAL ISOLATOR having two sections, one for transfer of the $\overline{\text{STROBE}}$ signal, the other for the serial data bits. Each transmission sequence requires the transfer of 14 bits. The sequence is initiated by the first $\overline{\text{STROBE}}$, following channel selection (see Fig. 4-1) which, transferred by the OPTO ISOLATOR, clears the SERIAL/PARALLEL SHIFT REGISTERS and creates the TRANS A signal via the retriggerable MONOSTABLE. The TRANS A signal initiates a "sample and hold" action at the OUTPUT AMP by placing the previous output state, stored in C_O, at the amplifier input via S2. The OUTPUT AMP, being held (by S3) in a repeater configuration, thus holds the previous state of the output until all 14 bits are transmitted. This action is timed by the time constant of the MONOSTABLE until the completion of transmission of the 14 bits. At this time, the MONOSTABLE changes states, the AMPLIFIER CONTROL PROM commands a new output configuration and the output changes to the new programmed value. While the OUTPUT AMP is held at the previous value, all 14 bits are strobed serially into the SERIAL/PARALLEL SHIFT REGISTERS, and presented in parallel to the AMPLIFIER CONTROL PROM (bits 1 and 2, RANGE, POLARITY) and to the DAC (12 bits for output voltage magnitude). At the completion of the transfer, the OUTPUT AMP is released from the hold mode (S1 closes, S2, S3 open) and is set to a new output magnitude by means of the DAC output AMP CONTROL PROM. The POLARITY and RANGE SELECT NETWORKS contains a network of precision resistors and solid state switches which are set by the AMP CONTROL PROM in response to the RANGE and POLARITY select commands.

4-10 DIGITAL FRONT END, SERIES 500 (REFER TO FIG. 4-2)

4-11 BUS INTERFACE. The Kepco Series 500 Digital Programmer is connected to the digital data bus via its 50 pin rear connector (PC-12). The input/output pin designations have been described in detail in Section III (see Par. 3-3). After the parallel data has been applied to the input of the Series 500 Programmer it must be strobed-in as illustrated in the timing diagram (see Section III, Fig. 3-2). Following the $\overline{\text{STROBE}}$ (2 μsec. minimum) a BUSY signal is presented on PC-12, indicating that the SN 500 Programmer is in the internal data transfer mode and will not yet accept new data. *NOTE, HOWEVER, THAT THE DATA BUS IS FREE, IMMEDIATELY FOLLOWING THE 2 μsec. $\overline{\text{STROBE}}$.*

4-12 DIGITAL DATA TRANSFER CIRCUIT. Once the $\overline{\text{STROBE}}$ has been received, the SHIFT/LOAD line goes high and the data, which has been stored in parallel by the PARALLEL/SERIES SHIFT REGISTERS, is shifted out serially under the control of the 16 BIT TRANSFER COUNTER, synchronized by the CLOCK. Following the transfer of all 16 bits, the COUNTER and all Flip-Flops are reset by the RESET AND POWER-ON Flip-Flop. As a result, the BUSY line goes low, indicating readiness to accept new data from the data bus.

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