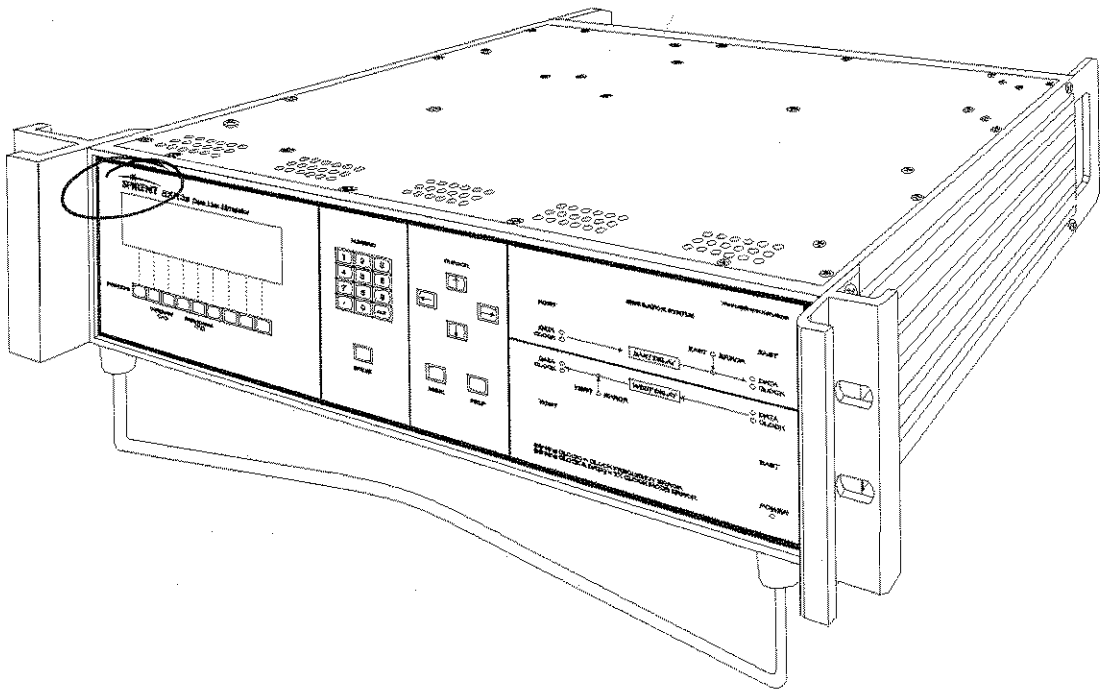
SX/13a
Data Link Simulator



Operating Manual

Adtech or Spirent

PN 340-5038-001 REV A

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See Chapter 8 for technical support information

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About this Manual

The SX/13a Operating Manual describes how to use the SX/13a Data Link Simulator. This manual is a comprehensive guide to installing, setting up, and operating the SX/13a. The manual includes procedures that are specific to each of the nine interfaces and optional modules, and the physical specifications of each.

The SX/13a Operating Manual is for people involved with the day-to-day use of the product. This includes network administrators, system administrators, hardware engineers, software engineers, and quality assurance technicians. In addition, individuals tasked with planning tests for applications and equipment may find the manual useful for understanding what types of test scenarios can be created.

The chapters are:

Chapter 1, Installing the SX/13a, explains how to install and connect the SX/13a chassis, interfaces, and options.

Chapter 2, Setting Up the SX/13a, explains the basic setup when first turning on the unit.

Chapter 3, Setting Up SX/13a Interfaces, explains how to set up the nine data link interfaces.

Chapter 4, Operating the SX/13a, explains how to set up the **MAIN PARAMETERS** screen, including setting delay and errors parameters.

Chapter 5, Creating Programs for the SX/13a, explains how to create programs and program steps, which are more complicated testing situations.

Chapter 6, Using the Error Targeting Options, explains how to use the two error targeting options that extend the functionality of the SX/13a unit. The two options are the SX/13a Error Targeting Option and the Extended T1/E1 Simulation Option.

Chapter 7, Remotely Operating the SX/13a, explains how to set up the two remote control options for operations from a remote control unit.

Chapter 8, Diagnostics and Troubleshooting for the SX/13a, explains how to run the diagnostics and how to contact Technical Support.

Chapter 9, SX/13a Specifications, details the physical characteristics and operating requirements of the unit.

Document Conventions

Front panel function keys as displayed on the liquid crystal display (LCD) screen are set in boldface and are enclosed in angle brackets. For example: Select the **<setup>** function key.

Front panel keys, light emitting diode (LED) descriptions, and labels on the front and back panel are set in boldface, uppercase type. For example: Press **MENU**.

Screen names are boldface, small caps. For example: This displays the **MAIN PARAMETERS** screen.

File names are set in all uppercase lettering. For example: Copy the `SXKEYCAPS.EXE` file to the floppy disk.

DOS commands, coding, and user-entered commands are set in boldface, uppercase type. For example: At the prompt, type **`GOTO`**.

SX/13a Product Overview

The SX/13a is part of the Spirent SX Data Link Simulators product line, which simulates terrestrial and satellite data links for testing internetworking equipment and applications under repeatable and controllable conditions. Utilizing dual-channel, full-duplex operation, these simulators provide bi-directional testing with programmable delays, random bit errors and burst errors. Multiple delay and error events can be programmed into complex sequences to simulate a wide variety of chronic and periodic conditions or events, such as peak traffic and equipment overloads. Three products are included in the SX product line and differ primarily in the speeds supported and extended functionality options available:

- SX/12 — Supports speeds up to 8.448 Mbps and remote operation options
- SX/13a — Supports speeds up to 51.84 Mbps and can be upgraded with error targeting and remote operation options
- SX/14 — Supports speeds up to 155.52 Mbps and can be upgraded with an error targeting interface and remote operation option

The SX products consist of a rack-mountable, portable mainframe coupled with at least one interchangeable interface. The interfaces enable the mainframe to connect to different types of data links. Other options extend the SX/13a's functionality. The unit can be used in lab conditions or for live field testing. The primary method of operation is through the front panel keys and LCD screen. Optional modules enable it to be operated remotely via a PC or other type of terminal. This allows the test set to be placed permanently in a network, if necessary.

Typical simulator applications include testing the operation, performance and reliability of multiplexers, bridges, encrypters, network applications and other communications hardware and software. When used for link simulation, these simulators physically connect directly between two pieces of equipment to replace conventional data links, such as satellite connections, WANs or telephone networks. They can also be used in line with an actual data link to add additional delays or errors, or to simulate the effects of adding an additional link to the system.

Data Link Interfaces

The interfaces and options available for the SX/13a are:

- SONET 51.84 Mbps (STS-1) Interface
- DS3 (T3 44.736 Mbps) Interface
- DS1 (T1 1.544 Mbps) Interface
- G.703 (E3 34.368 Mbps) Interface
- G.703 (E1 2.048 Mbps) Interface
- High Speed Serial Interface (HSSI)
- V.35 Interface
- RS-449 (RS-422-A) Interface
- RS-232-C Interface

Extended Error Targeting Options

The Extended Error Targeting Options for the SX/13a are:

- Extended T1/E1 Simulation Option (installed in an interface slot in the card cage)
- SX/13a Error Targeting Option (installed internally)

Remote Operation Interfaces

The Remote Operation Interfaces available for the SX/13a are:

- IEEE-488 Remote Control Interface (installed in the remote control port on the back panel)
- RS-232-C Remote Control Interface (installed in the remote control port on the back panel)

Chapter 1. Installing the SX/13a

Installing the SX/13a Overview

Installation of the SX/13a unit for local (non-remote) operation includes installing the mainframe, installing interfaces and modules not factory-installed, connecting the power supply cord, and connecting data link equipment to the interfaces. Installation of the SX/13a unit for remote operation includes the additional steps of installing and configuring a PC or other terminal as a remote controller, installing a remote control interface if not factory-installed, and connecting the remote control interface to the remote controller.

Setting up the SX/13a with an external clock source includes the additional step of connecting the external clock source to the external clock input and selecting the clock source when setting up an interface.

The SX/13a can be rack-mounted or not mounted at all. Interfaces and options are factory-installed unless more interfaces and options are ordered than can be installed in the mainframe at one time. Interfaces are installed and removed from the card cage in the rear of the unit. If this is the case, follow the procedure for installing an interface or optional module as necessary. All delivered interfaces and options are compatible with the SX/13a, despite any nomenclature on the hardware to the contrary. No software installation is necessary for local operation of the SX/13a unit.

System Description and Requirements

AC Power Supply

The SX/13a can operate using a 110 or 230 VAC power supply. The fuse is preset by the factory to the shipping destination's line voltage rating, with no additional adjustments necessary. The unit ships with a power supply cord.

Backup Battery

The SX/13a unit includes an internal lithium battery with a 10-year life span. The battery retains the simulator settings, channel parameters, and programming selections in memory when the unit is turned off.

If the battery fails, default parameters are restored when the unit is turned on. If this should occur, contact Technical Support for assistance.

Adequate Ventilation

During operation, a fan located on the unit's rear panel cools the SX/13a. Do not block the fan or obstruct the air vents located on the top cover, bottom cover, or side panels of the unit. Cover all unused interface slots on the rear panel with the cover plates provided. This ensures proper airflow through the unit.

Safety Precautions

Be sure that you understand all directions, warnings, and limitations before using this product. In this document:

NOTES describe limitations on the use of the equipment or procedure.

CAUTIONS reflect conditions that could cause product damage or data loss.

WARNINGS present information or describe conditions that, if not observed, could result in injury.

Unpacking

Before opening the SX/13a carton, examine the carton for damage. If damage is not visible, unpack the carton and check the contents for damage. Save all packing materials. If damage is noted, forward an immediate request to the delivering carrier to perform an inspection, and prepare a damage report. Save the container and packing material until contents are verified.

Concurrently, report the nature and extent of damage to Spirent Communications' Shipping Department so that action can be initiated to repair or replace damaged items, or instructions issued for returning items.

The responsibility of the manufacturer ends with delivery to the first carrier. All claims for loss, damage, or non-delivery must be made against the delivering carrier within 10 calendar days of receipt of shipment.

Preventing Electrostatic Discharge

WARNING! Always unplug the AC power cord before opening the chassis.

CAUTION! Always use a properly grounded anti-static wrist strap when handling the circuit boards and interface modules. Failure to do so can result in permanent damage to the components.

Proper precautions must be taken when installing or removing any SX components to prevent damage from electrostatic discharge (ESD). An ESD wrist strap is available for those who do not have a properly equipped work area. Contact your Spirent sales representative, or call (800) 774-7368 or (818) 676-2300 to obtain a wrist strap.

Installing the Hardware

Mounting the Mainframe

The SX/13a Data Link Simulator can be bench-mounted or rack-mounted in a 19-inch rack. The rack-mounting brackets are part of the mainframe. If bench-mounted, a support bracket located on the bottom unit can be used to elevate the unit to an angle.

Using the SX/13a Rear Panel

Figure 1.1 shows the SX/13a rear panel, which includes:

- If purchased, one remote control interface port for either the IEEE-488 Remote Control Option or RS-232-C Remote Control Option. If not purchased, the faceplate replaces the actual port
- Five interface and option slots in a card cage with either cover plates or installed interfaces
- One fan
- One BNC connector for external clock input connection
- One universal power receptacle for the power supply cord
- One power switch
- One fuse

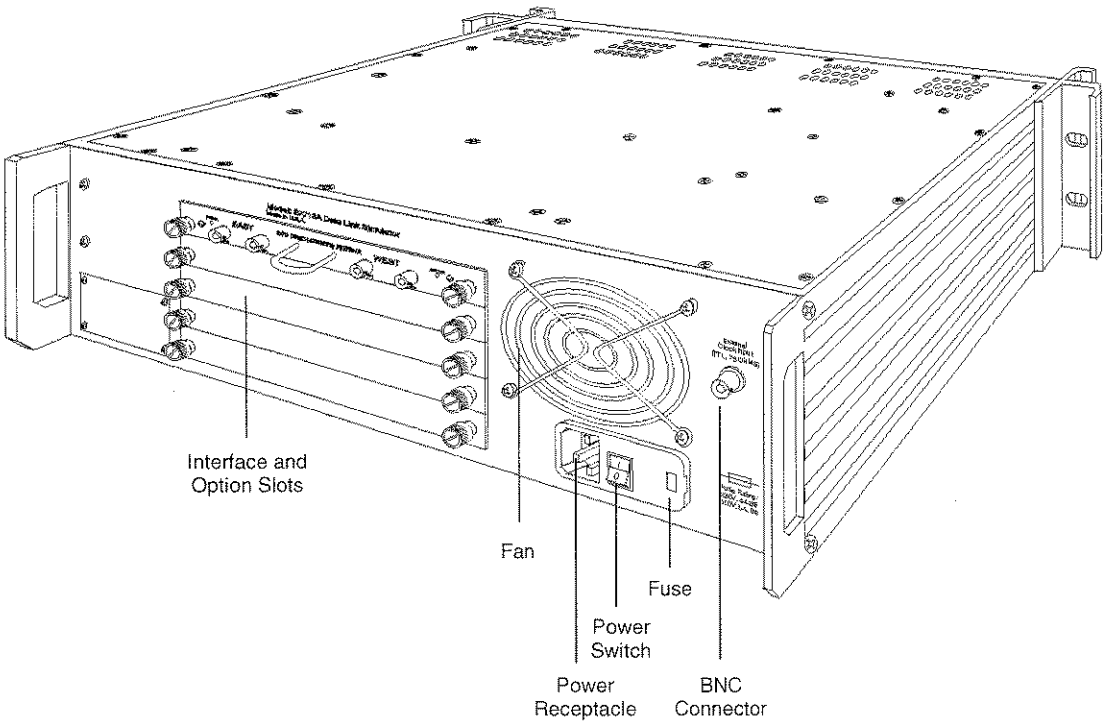

Figure 1.1 SX/13a Rear Panel

Installing an Interface or Option

There are nine interfaces and one option that can be installed. Chapter 3, Setting Up the SX/13a Interfaces, includes each interface's faceplate diagram. The interfaces and option are:

- SONET 51.84 Mbps (STS-1) Interface
- DS3 (T3 44.736 Mbps) Interface
- DS1 (T1 1.544 Mbps) Interface
- G.703 (E3 34.368 Mbps) Interface
- G.703 (E1 2.048 Mbps) Interface
- High Speed Serial Interface (HSSI)
- V.35 Interface
- RS-449 (RS-422-A) Interface
- RS-232-C Interface
- Extended T1/E1 Simulation Option

Tools Needed for Interface Installation

Gather the following tools to install an interface:

- Anti-static grounding wrist strap
- Grounded, anti-static mat
- Slotted screwdriver for installing an interface module or option
- Philips-head screwdriver for installing a remote control interface

The steps to install an interface or optional module are:

1. Individual must be properly grounded.
2. Turn off the SX/13a using the power switch on the rear of the unit.

   CAUTION! You might cause permanent damage to the SX/13a if you attempt to install or remove an interface while the mainframe unit is on.

3. Some interfaces have configurable jumpers. Configure the jumpers before installing the interface. Chapter 3, Setting Up the SX/13a Interfaces, contains the jumper-setting procedure.
4. Locate an unused card cage slot and remove the cover plate, or remove an existing interface or option module by unscrewing the two thumbscrews and pulling the interface out from the chassis.
5. Insert the new interface into the chassis so that the name of the interface on the panel reads right side up. The components face down. Slide the outer edges of the circuit board into the two white nylon card guides on both sides of the card cage. While pressing on the handle of the module panel, push the module all the way in until it is seated firmly in the connector in the back of the card cage. Once fully seated, tighten the two thumbscrews to secure the module.

6. Connect the power supply cord.

   NOTE: Be sure to cover all unused interface slots on the rear panel with the blank cover plates provided. This will ensure proper airflow through the unit.

On power-up, the SX/13a lists all installed interfaces and options, then displays the **SETUP** screen. If an interface or option that was installed does not appear in this list, turn off the unit, and check that it was installed properly. If a problem persists, contact Technical Support.

For interfaces that have a **POWER** LED, the green LED is illuminated when the interface is receiving power. The amber **ACTIVE** LED is illuminated when the interface is selected as the active interface.

Connecting to Other Equipment

The method of connecting to other equipment depends on the installed interfaces. A typical procedure to connect to other equipment is:

1. Select the appropriate data cable.
2. Attach one end of the cable to the appropriate SX/13a interface.
3. Attach the other end to the device under test (DUT).
4. Turn on power to the SX/13a unit and the DUT.
5. On power-up, view the SX/13a LCD to ensure that the interface is listed as an installed interface.
6. Enable an active interface as necessary.

Installing a Remote Control Interface

The two remote control interfaces are:

- IEEE-488 Remote Control Interface
- RS-232-C Remote Control Interface

Installing a remote control interface includes installing the interface, loading and configuring the controller software, and connecting the controller to the SX/13a unit. The port for a remote interface is located in the lower left-hand corner of the rear panel of the SX/13a.

To install a remote control interface:

1. Individual must be properly grounded.
2. Turn off power to the SX/13a simulator and unplug the AC power cord from the chassis.
3. Facing the front panel of the SX/13a simulator, remove the top four screws (along the right edge of the chassis) that secure the side panel.
4. Remove the bottom four screws (along the edge of the chassis) that secure the side panel.
5. Remove the two screws that secure the rack-mount handle to the side panel.
6. Remove the four screws that secure the side panel to the chassis.
7. Remove the four screws that secure the blank Remote Control Interface panel to the rear panel of the chassis.
8. Locate the 20-pin remote ribbon cable inside the chassis, and cut and remove the tie straps that secure it to the chassis.

9. Carefully insert the Remote Control Interface (components facing up) through the chassis rear panel opening.
10. Carefully insert the two plastic standoff posts into the mounting holes on the Remote Control Interface.

    NOTE: Do not remove the coated paper from the bottom of the standoff posts.

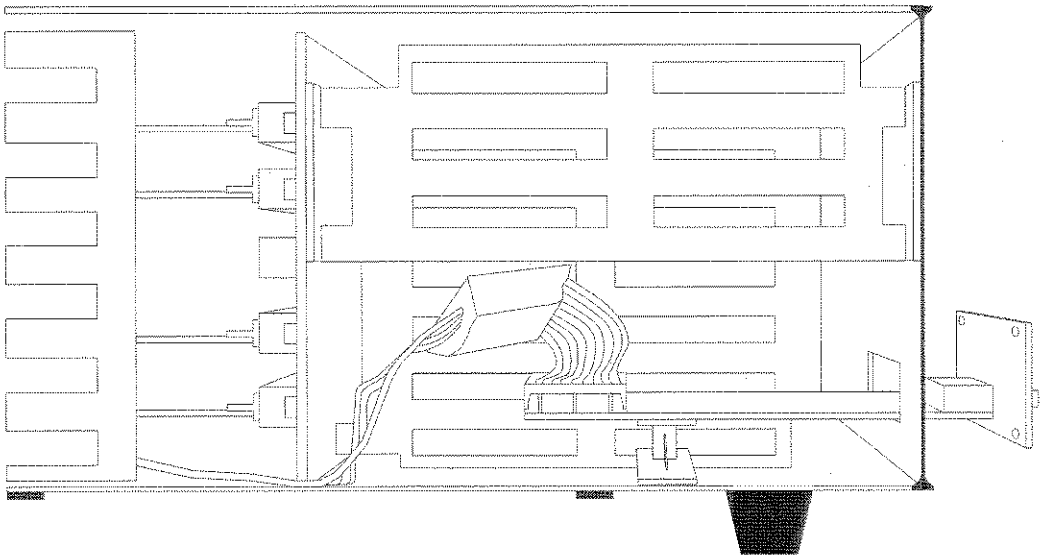

Figure 1.2 View of SX/13a with Side Panel Removed

11. Plug the 20-pin ribbon cable connector to the Remote Control Interface.

    CAUTION! Make sure the red line on the 20-pin ribbon cable is on the same side as Pin 1 of the interface's 20-pin connector. Improper installation will cause the SX/13a simulator to malfunction.

12. Replace and tighten the four screws that hold the Remote Control Interface to the chassis rear panel.
13. Replace the side panel and the four screws that secure the side panel to the chassis.
14. Replace the rack-mount handle and the two screws that secure the rack-mount handle to the chassis.
15. Replace and tighten the top four screws that secure the side panel to the chassis.
16. Replace and tighten the bottom four screws that secure the side panel to the chassis.
17. Plug in the AC power cord to the chassis and turn on power to the SX/13a simulator.

On power-up, the SX/13a lists all installed interfaces and options and then displays the **SETUP** screen. If a module that was installed does not appear in this list, turn off the unit, and check that the interfaces are installed properly. If a problem persists, contact Technical Support. Chapter 7, Remotely Operating the SX/13a, provides more detail for remote operation.

Setting Up the Remote Interface and Controller

The remote interface port is located on the rear panel of the SX/13a in the lower left-hand corner. The remote is factory-installed, if the option was ordered at the same time as the unit. The IEEE-488 ships with the IEEE-488 Controller Software, which works with the IOtech IEEE-488 card interface. The disk also includes sample code in BASIC for programmers who write their own programs for the IEEE-488 remote.

Setting Up the IEEE-488

1. Install the option.
2. Install the software provided on the IEEE-488 Controller Software diskette on the PC controller.
3. Connect the SX/13a to the controller.

Connecting the IEEE-488

To connect the SX/13a to a PC or workstation:

1. Connect one end of an IEEE-488 cable to one end of the SX/13a's remote port, and the other end to the controlling equipment.
2. Tighten the retaining screws.

On power-up, the SX/13a displays the message "IEEE-488 Remote Control Rev. (x.x)" and lists the installed modules. If this message does not appear, turn off the power, make sure the IEEE-488 is correctly installed and the cable is connected firmly, and turn on power again. If a problem persists, contact Technical Support.

Installing the IEEE-488 Controller

1. Run the install batch file on the included IEEE-488 Controller Software diskette.
2. Assign an IEEE-488 address. Both the controller and the SX/13a are configured. Use the same address number for both settings. Since address "00" is usually reserved for the bus master, avoid using "00" for an address. Choose an address between 1 and 31.

To ensure that the remote device displays the SX/13a screens as accurately as possible, the controller should support ANSI commands. ANSI commands permit the controller screen to display the SX/13a screen in a fixed position at all times. Without ANSI, any SX/13a screen displayed scrolls upward as new commands are entered.

These addresses and screen parameters are retained in the SX/13a's battery-backed memory when power is removed.

Setting Up the RS-232-C Remote Interface and Terminal

The remote interface port is located on the rear panel of the SX/13a in the lower left-hand corner. The remote is factory-installed, if it was ordered with the unit. If the option is not installed, follow the instructions for installing a remote control interface.

Connecting the RS-232-C

To connect the SX/13a to a VT-100 compliant terminal, PC, or workstation:

1. Using an RS-232-C cable with a DB-25 connector, connect one end to the SX/13a's remote port and the other end to the terminal or computer equipment. For RS-232-C cables, do not use a null modem.
2. Tighten the retaining screws.
3. Turn on the unit.
4. The message "RS-232-C Remote Control Rev. (x.x)" and a list of any other installed modules are displayed.

If this message does not appear, turn off the power, make sure the RS-232-C is installed correctly and the cable is connected firmly, and turn on the power again. If a problem persists, contact Technical Support.

A PC software package, such as Procomm or HyperTerminal, can be used to save and reload SX/13a settings on the controller.

Setting Up the RS-232-C Remote Controller

The terminal or computer to be connected to the SX/13a should be configured:

- For half-duplex operation
- Not to automatically generate a line feed for each carriage return
- To support ANSI commands (this is preferable, but not required)

Installing the SX/13a Error Targeting Option

The SX/13a Error Targeting Option is a circuit board that must be installed internally in the SX/13a mainframe either by Spirent Communications or a designated distributor. This option allows the user to inject errors of various programmable types into random or specific places within formatted or unformatted data streams.

Contact Spirent Communications or a designated distributor to arrange the purchase and installation of the SX/13a Error Targeting Option.

Connecting an External Clock Source

The BNC connector for an external clock source is located on the rear panel. It is labeled **EXTERNAL CLOCK INPUT**. Any 75-ohm coaxial cable may be used to connect the SX/13a to an external clock source.

Starting the System

Using the SX/13a Front Panel

The front panel is the user interface for operation of the SX/13a unit, unless a remote control option is installed. The front panel consists of four sections (see Figure 1.3).

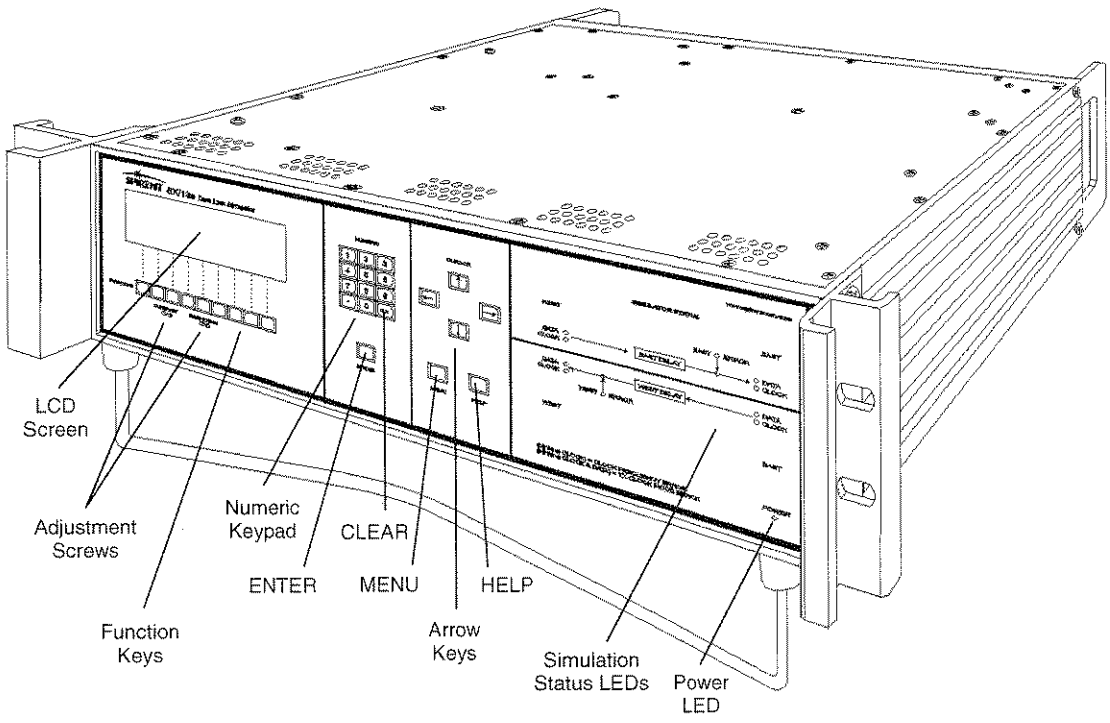

Figure 1.3 SX/13a Front Panel

From left to right, the sections of the front panel include:

- An LCD screen, nine function keys, a contrast adjustment screw, and a brightness adjustment screw
- A 12-key numeric keypad and **ENTER** button. The numeric keypad includes the numerals 0–9; a period (.); and a clear button (**CLR**).
- A four-key cursor keypad that consists of directional arrows for moving the LCD cursor, a blue **MENU** key, and a red **HELP** key
- **SIMULATION STATUS** LEDs and a **POWER** LED

LCD Screen and Function Keys

The LCD screen consists of eight lines of 40 characters on each line. The screens display the operating information for the unit. The nine function keys, also known as soft keys, correspond to screen selections. The values of the function keys change for each screen and are displayed onscreen. White dotted lines are displayed to connect the onscreen key labels to their corresponding function keys.

The top line of the screen displays the screen name. For example, Figure 1.4 shows the **SETUP** screen. The middle lines of the LCD screen display the information specific to the screen. The two bottom lines display the values for the function keys.

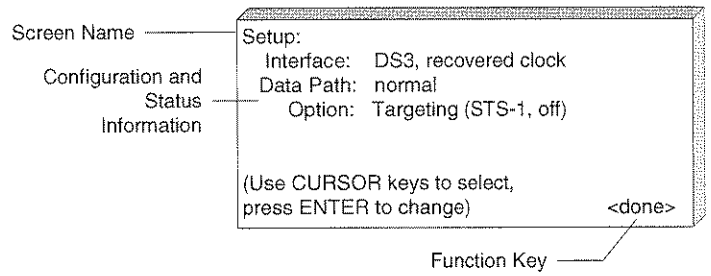

Figure 1.4 Typical LCD Screen

Adjusting the Contrast and Brightness of the LCD Screen

The **CONTRAST** and **BRIGHTNESS** adjustments are located below the LCD and functions keys on the front panel. Use a small, flat-blade screwdriver to turn the controls. Turn the **CONTRAST** adjustment to the right to increase the contrast. Turn it to the left to decrease the contrast. Turn the **BRIGHTNESS** adjustment to the right to increase the brightness of the display. Turn it to the left to decrease the brightness.

Numeric Keypad and ENTER Key

Use the numeric keypad to enter numeric values, such as data rates and delays. The keypad includes a period (.) for entering decimal values and a **CLR** key to erase values by backspacing.

The **ENTER** key can complete an entry, make a menu selection, or display a sub-screen.

Cursor Keys, MENU Key, and HELP Key

The cursor keys relocate the cursor or highlight fields on the LCD. The arrow keys correspond to which direction the cursor moves. The cursor is a reverse-video display that creates a highlight to indicate a location or selection.

Pressing the blue **MENU** key displays the main **MENU** screen. The **MENU** screen is the highest level of the menu hierarchy. It shows the name and version of the unit. This screen includes function keys that display the major screens used in setting up parameters, creating programs, viewing statistics, and so on.

The **HELP** key displays the help topic associated with the screen or the highlighted entry field.

Simulation Status and Power LED Indicators

The right-most section of the front panel is titled **SIMULATION STATUS** and includes LEDs that indicate the statuses for the East and West channels. For each channel, an LED indicates the data, clock, and error statuses for the current data link settings. An illuminated LED indicates a signal presence. An unilluminated LED indicates an absence of a signal. A blinking **CLOCK** LED indicates that the clock signal does not match the data rate setting. **CLOCK** and **DATA** LEDs blinking simultaneously indicate a clock slip.

The LEDs are:

- **DATA** (four) — Flash green to indicate data flow; one each to represent the West receive, West transmit, East receive, and East transmit
- **CLOCK** (four) — Light steady amber to indicate correct timing; blink amber to indicate that the clock signal measured at that point does not match the set data rate; do not illuminate to indicate no signal presence
- **EAST ERROR** (one) — Flashes red with every error injected into the Eastbound data
- **WEST ERROR** (one) — Flashes red with every error injected into the Westbound data

When a transition occurs on the data or clock signal, the corresponding indicator is illuminated. When a signal is absent, the indicator is not illuminated.

The green **POWER** LED on the lower right-hand side of the front panel illuminates when the unit is turned on.

Understanding the Menu System

The **MENU** key on the front panel can be pressed while viewing any screen to display the top-level screen in the menu hierarchy — the **MENU** screen. The **MENU** screen and the **MENU (CONT.)** screen constitute the root of the menu tree. Pressing the **<more>** function key on the **MENU** screen displays the **MENU (CONT.)** screen. Figure 1.5 shows several levels of the SX/13a menu tree.

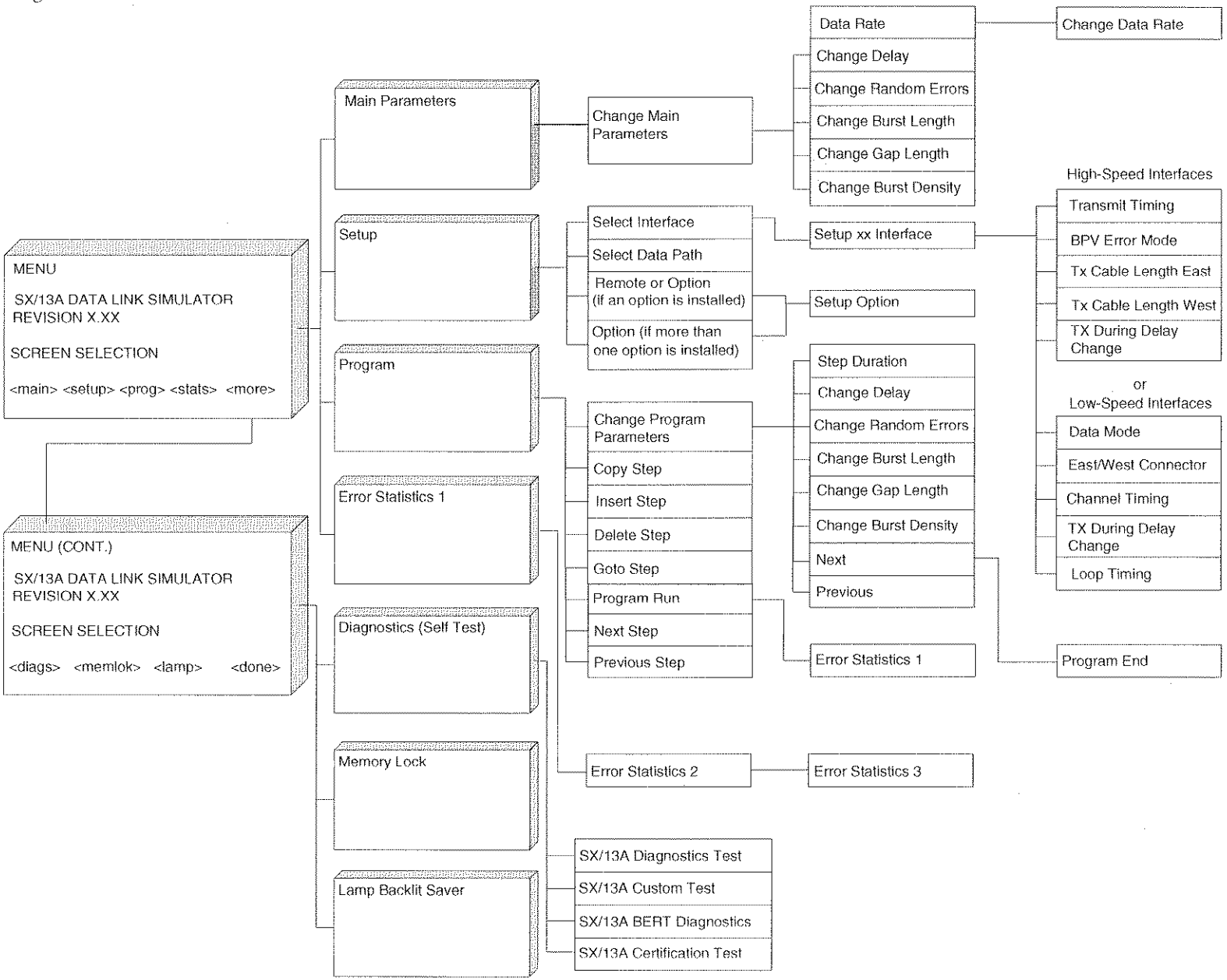

Figure 1.5 SX/13a Menu Hierarchy

The available function keys on the **MENU** screen are:

<main> — Displays the **MAIN PARAMETERS** screen. This screen sets the data rate, delay parameters, random error parameters, and manually triggered burst errors.

<setup> — Displays the **SETUP** screen. This is the default screen displayed after turning on the unit. It shows the active interface and clock mode, the selected data path, and installed options.

<prog> — Displays the **PROGRAM** screen. A program can consist of up to 99 steps. Each step includes delay and error parameter settings, like those configured with the **MAIN PARAMETERS** screen.

<stats> — Displays the **ERROR STATISTICS 1** screen. This screen and two additional error statistics screens display the number of errors injected in each channel and the number of errored seconds, burst errored seconds, and severely errored seconds. Burst errors can be triggered from this screen.

<more> — Displays the **MENU (CONT.)** screen.

The available function keys on the **MENU (CONT.)** screen are:

<diags> — Displays the **SX/13A DIAGNOSTICS (SELF TEST)** screen. This screen runs the initial diagnostics, customized diagnostics, and a bit error rate test (BERT).

<memlok> — Displays the **MEMORY LOCK** screen. Locking the memory prevents accidental changes from being made to the current settings. A user can continue to trigger burst errors, run (but not change) programs, and access other functions that do not modify the system's settings even when memory lock is turned on. To turn Memory Lock on or off:

1. Press the **MENU** key.
2. Press the **<more>** function key.
3. Press the **<memlok>** function key.
4. Press **<on>** to lock in the current settings.
5. Press **<off>** to unlock the current settings.

<lamp> — Displays the **LAMP BACKLIT SAVER** screen. Sets a duration of front panel inactivity in minutes after which the LCD lamp is turned off. The screen saver function does not affect the settings of the unit. Delays, errors, and program settings continue to function. The **<off>** function key turns off the timer. Pressing any front panel key reactivates the lamp.

<done> — Displays the **MENU** screen.

Additional function keys are displayed on the **MENU** screen depending on the installed options and interfaces, and on the settings.

Running the Initial Diagnostics

The SX/13a features two levels of diagnostic testing. First, on power-up, the SX/13a runs an internal self-test, which performs an abbreviated check of the internal circuitry and each installed option. The second level of diagnostics includes a set of user-controlled routines that perform detailed internal circuitry tests. The error targeting options have an additional set of diagnostics accessed through the specific error targeting option diagnostics screen.

The SX/13a has been thoroughly tested at the factory prior to shipping. However, to verify that the unit was not damaged during shipping, run the diagnostics once on initial power-up.

The internal system test includes six diagnostic routines. These test the keyboard, memory, delay, clock generator, error generator, and data path.

There are two test modes:

- In single test mode, the routine stops after completing the entire set of tests.
- In continuous test mode, the test sequence restarts after the last test but omits the keyboard test on all subsequent passes. In this mode, the SX/13a displays the number of times the test sequence has passed. The test sequence restarts from 0 when the system reaches a count value of 65535.

Chapter 2. Setting Up the SX/13a

Getting Started with the Setup Screen

The **SETUP** screen is displayed after turning on the unit. The screen sets the active interface and transmit timing source, data path, and displays, sets, and enables remote control interfaces and optional modules. Pin assignments, connector types, signal levels, and setting options for each interface are specified in Chapter 3, Setting Up the SX/13a Interfaces.

The basic steps are:

1. Select and configure an active interface.
2. Select the transmit timing mode.
3. Select a data path.
4. Set the main operating parameters.

Selecting the Active Interface

Up to five interfaces can be installed in the card cage. Only one interface can be active at a time. Each interface provides the physical line connection for the various data channels that the SX/13a simulates. The active interface determines the default data rate.

Options (not interfaces) can be active at the same time as an interface. These include one of two remote control options, and the SX/13a Error Targeting Option or the Extended T1/E1 Simulation Option.

NOTE: All interfaces and options supplied for the SX/13a are compatible, despite any contrary nomenclature on the hardware. Although several interfaces are labeled "SX/13" on the front panel, they are fully compatible with the SX/13a.

Displaying the **SETUP** screen:

1. Press **MENU**.
2. Press the **<setup>** function key.
3. The active interface and the transmit timing mode is shown. Each interface has a setup screen with its specific parameters.

The **SETUP** screen can also be displayed from the **MAIN PARAMETERS** screen with the **<setup>** function key. To select an interface or to change settings for the current interface:

1. Highlight the active interface with the cursor keys.
2. Press **ENTER**.
3. The **SELECT INTERFACE** screen is displayed if more than one interface is installed. The **SELECT INTERFACE** screen lists the installed interfaces. The interface-specific setup screen is displayed if only one interface is installed.
4. Select an interface to make active.
5. Press **ENTER**. The setup screen for the specific interface is displayed. The amber **ACTIVE** LED is illuminated on the active interface. Only one interface can be active at a time.

NOTE: If the interface name is not displayed, the interface may not be installed. To install an interface, turn off the SX/13a and follow the procedures in Chapter 3.

Figure 2.1 shows the DS3 (T3) Interface as the active interface. Settings for each configured interface are stored in memory when the interface is deactivated. These settings are restored when the interface is reactivated.

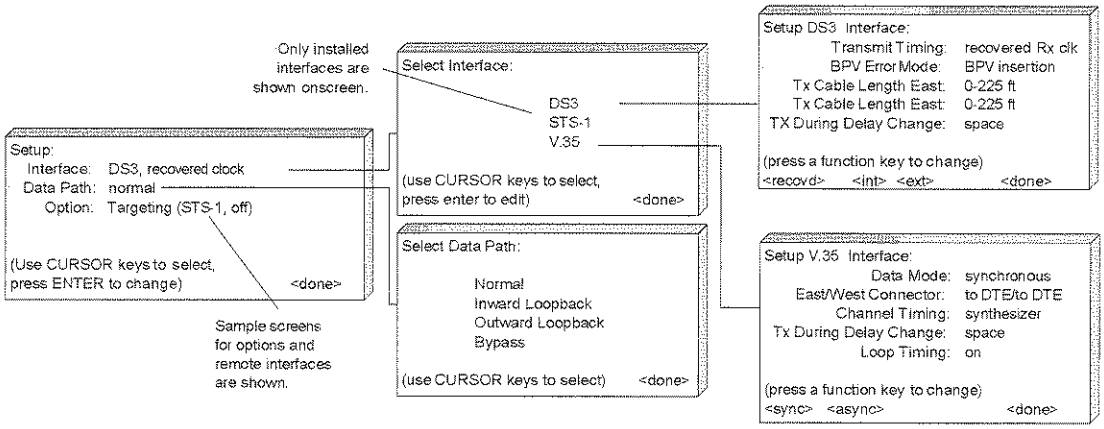

Figure 2.1 Typical Setup Screens

Selecting the Transmit Timing Mode

This section provides a brief overview of the transmit timing for the SX/13a unit. The transmit timing mode settings are unique to each interface. The specific options for each interface are detailed in Chapter 3, Setting Up the SX/13a Interfaces.

Understanding Clocking Requirements

Before testing the simulated link, it is important to consider the data link clocking requirements for different modes of operation. The data link clocking requirements of a particular simulation vary according to the type of interface, the device under test, and the data path mode.

Understanding Transmit Timing

The three basic timing sources for transmitting data through the SX/13a are: recover received clock, internal clock, or external clock. The clock source is set for each interface.

Recover Received Clock (Loop Timing)

The master network timing source is received from equipment connected to the SX/13a. The unit recovers the timing from the received data and uses this recovered clock to transmit data through itself and out the end of the other channel. The received clock is either recovered from the data or on a separate line, depending on the interface.

Internal Clock

The SX/13a provides the master network clock. Internal clocking is provided in one of two ways: by using the internal frequency synthesizer, or by using fixed-frequency crystal oscillators located on the interfaces. Only the high-speed interfaces have an onboard oscillator. The range of the internal frequency synthesizer is 100 Hz through 52 MHz, with resolution in 1 Hz increments. The internal clock frequency synthesizer provides greater granularity than the oscillators. The data rate setting for each interface automatically determines whether the synthesizer or the oscillator is used, with the exception of the HSSI interface which is user selectable. The oscillators for each interface are located on the interface card, except for RS-422, RS-232, and V.35. The range for each oscillator is specific to each interface.

Other equipment in the network is set to recover received timing (i.e., loop timing), if the SX/13a unit provides the network timing.

The interfaces with onboard oscillators are:

- SONET 51.84 Mbps (STS-1) Interface
- High Speed Serial Interface (HSSI)
- DS3 (T3 44.736 Mbps) Interface
- G.703 (E3 34.368 Mbps) Interface
- DS1 (T1 1.544 Mbps) Interface
- G.703 (E1 2.048 Mbps) Interface

The interfaces without onboard oscillators are:

- V.35 Interface
- RS-449 (RS-422-A) Interface
- RS-232-C Interface

External Clock

While the SX/13a is the master network clock, the timing source is an external clock that regulates the timing of the transmitted data. The timing source is connected to the SX/13a either through the rear panel's TTL External Clock Input connector or the terminal timing signal of a synchronous interface such as the RS-422-A. Other equipment in the network are set to recover received or loop timing.

External clock mode can be used to test the receive interface and clock recovery circuits of the equipment being tested when jitter and wander are introduced by the external clock.

Internal and external clock mode can be used to test the receive interface and clock recovery circuits of the equipment being tested by matching a frequency error. Setting the clock faster or slower than the actual data rate for the interface creates a frequency error. The data rate is set on the **CHANGE DATA RATE** screen. However, in other situations, setting the data rate incorrectly can lead to incorrect operation.

The High Speed Serial Interface (HSSI) operates in internal or external clock mode, and in gapped or continuous clock mode with internal or external timing.

Asynchronous and Synchronous Data Modes

Operating in asynchronous mode enables the SX/13a to be used with low-speed asynchronous data (i.e., data with no accompanying clock). This mode is valid only for interfaces with separate clock and data lines. The RS-232-C, RS-449 (RS-422-A), and V.35 interfaces can operate in synchronous or asynchronous mode.

Selecting a Data Path

The SX/13a simulates a full-duplex data link consisting of two data channels:

- East channel (Eastbound data)
- West channel (Westbound data)

Eastbound data enter via the West interface receive (RX) connector, pass through the unit, and exit via the East interface transmit (TX) connector. Eastbound data are affected by the East channel parameters.

Westbound data enter via the East interface receive connector, pass through the unit, and exit via the West interface transmit connector. Westbound data are affected by the West channel parameters. Different data paths can be selected to implement various testing scenarios.

The four data paths in the SX/13a are:

- Normal: simulates a full-duplex data channel
- Bypass: skirts the error and delay generators
- Outward Loopback: simulates a local loopback condition
- Inward Loopback: simulates a remote loopback condition

Normal Data Path

The normal data path simulates a full-duplex data channel where error and delay characteristics are injected into data streams (see Figure 2.2). Westbound data enter the East receive connector, pass through the West delay and error generators, and exit via the West transmit connector. Eastbound data enter the West receive connector, pass through the East delay and error generators, and exit via the East transmit connector.

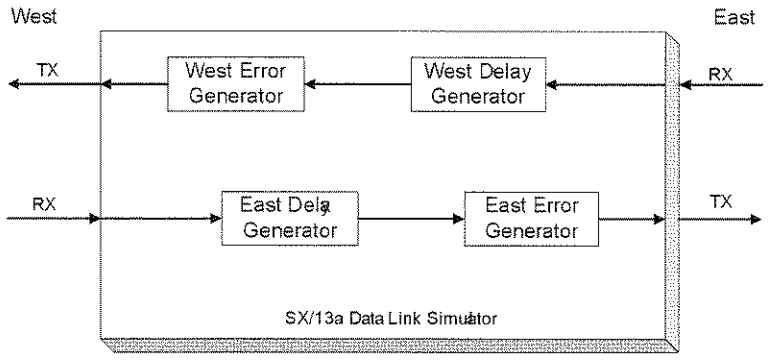

Figure 2.2 Normal Data Path

Bypass Data Path

The bypass data path simulates a back-to-back connection and is useful for testing cabling or for checking equipment performance without introducing additional delays and errors. Westbound data enter the East receive connector, bypass the delay and error generators, and exit via the West transmit connector. Eastbound data enter the West receive connector, bypass the delay and error generators, and exit via the East connector. All data and clock signals pass through the SX/13a, but without additional injected delay and errors. The signal is subject only to the propagation delay of the interface.

*NOTE: The green **DATA** LED indicators on the front panel are not illuminated when the data path is set to bypass mode.*

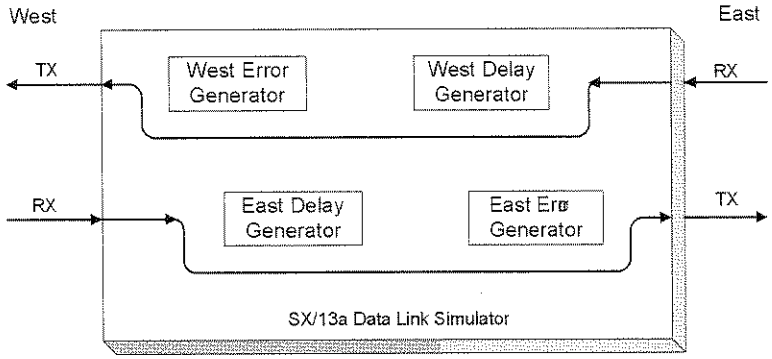

Figure 2.3 Bypass Data Path Mode

Outward Loopback Data Path

The outward loopback data path simulates a local loopback condition on both channels simultaneously. Westbound data enter the East receive connector and exit via the East transmit connector. Eastbound data enter the West receive connector and exit via the West transmit connector. Data bypass the error and delay generators of the unit and are subject only to the propagation delay of the interface (see Figure 2.4).

*NOTE: The green **DATA** LED indicators on the front panel are not illuminated while the data path is set to outward loopback mode.*

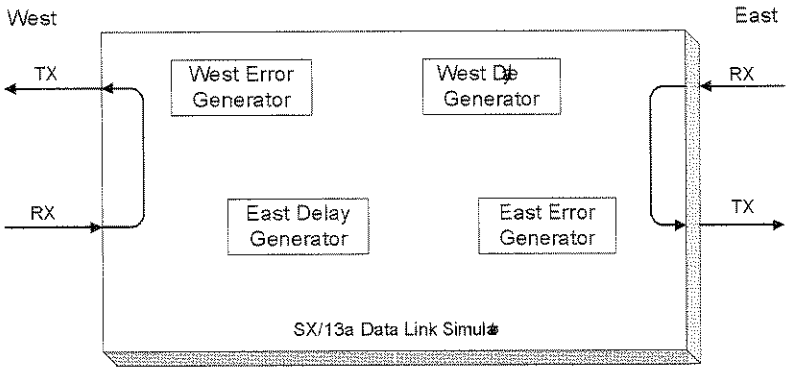

Figure 2.4 Outward Loopback Data Path Mode

Inward Loopback Data Path

The inward loopback data path simulates a remote loopback condition for both channels simultaneously. Westbound data enter the East receive connector, pass through the East delay and error generators, and exit via the East transmit connector. This is juxtaposed to normal mode in which the Westbound data pass through the West delay and error generators. Eastbound data enter the West receive connector, pass through the West delay and error generators, and exit via the West transmit connector. This is juxtaposed to normal mode in which the Eastbound data pass through the East delay and error generators.

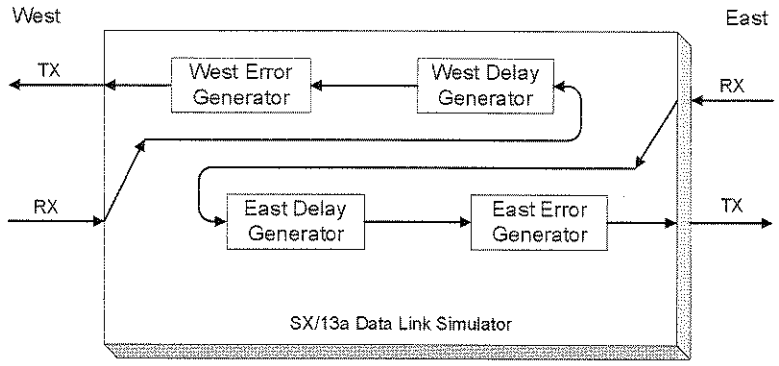

Figure 2.5 Inward Loopback Data Path Mode

Changing the Data Path

The **SETUP** screen displays the SX/13a data path. The data path is changed on the **SELECT DATA PATH** screen.

1. Press the **MENU** key, then the **<setup>** function key. The **SETUP** screen is displayed showing the active interface.
2. Press **ENTER**. The **SELECT INTERFACE** screen is displayed with the active interface highlighted. Press **ENTER** again or select a different interface and press **ENTER**. The setup screen for the interface is displayed.
3. Select the current data path and press **ENTER** to display the **SELECT DATA PATH** screen.
4. From the **SELECT DATA PATH** screen, select a new type of data path and press either **ENTER** or **<done>**. This activates the new data path and displays the **SETUP** screen, which shows new data path.

*NOTE: The **MAIN PARAMETERS** screen displays the data path setting when a path other than Normal is selected.*

Chapter 3. Setting Up the SX/13a Interfaces

The setup and specifications for the following nine data link interfaces are discussed in this chapter:

- SONET 51.84 Mbps (STS-1)
- DS3 (T3 44.736 Mbps)
- DS1 (T1 1.544 Mbps)
- G.703 (E3 34.368 Mbps)
- G.703 (E1 2.048 Mbps)
- HSSI
- V.35
- RS-449 (RS-422-A)
- RS-232-C

Each one of these interfaces can be installed in any card cage slot on the rear panel. The two error targeting options and two remote controller options are detailed in Chapter 6, Using the Error Targeting Options, and Chapter 7, Remotely Operating the SX/13a.

NOTE: All interfaces and options supplied for the SX/13a are compatible, despite any contrary nomenclature on the hardware. Although several interfaces are labeled "SX/13" on the front panel, they are fully compatible with the SX/13a.

The details provided for each interface include:

- A brief description, line drawing, features, and characteristics
- Step-by-step instructions for the initial set up of the interface
- Signalling leads and connector pin assignments, as relevant

SONET 51.84 Mbps (STS-1) Interface

The SONET 51.84 Mbps (STS-1) interface provides signal conversion between the SX/13a's internal format and signals complying with specifications for the 51.84 Mbps SONET STS-1 format (see Figure 3.1).

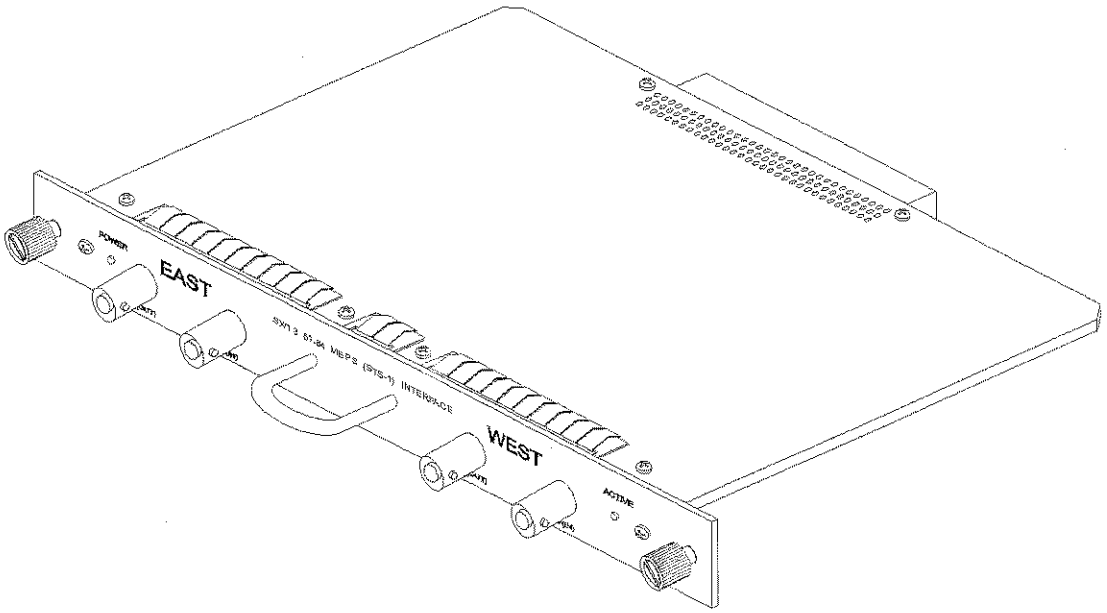

Figure 3.1 SONET 51.84 Mbps (STS-1) Interface

The features and capabilities of the SONET 51.84 Mbps (STS-1) interface are:

- 51.84 MHz data rate
- Accepts and generates B3ZS line coding
- Four BNC connectors: East receive, East transmit, West receive, West transmit
- Programmable output amplitude: Select transmit cable length on **SETUP STS1 INTERFACE** screen: low for cable lengths of 0–225 feet or high is for cable lengths greater than 225 feet. The East and West channels are independently selectable.
- Receiver sensitivity: 550 mV–1.1 V
- Input impedance: 75 ohms

Setting Up the SONET STS-1 Interface

Use the **SETUP STS1 INTERFACE** screen to select the:

- Transmit timing mode
- BPV error mode
- Transmit level (setting based on cable length)
- Data type to transmit during a delay change

To display the **SETUP STS1 INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **STS1** and press **ENTER**. The **SETUP STS1 INTERFACE** screen is displayed (see Figure 3.2).

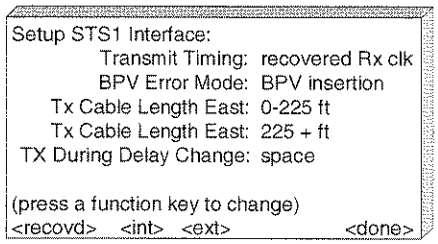

Figure 3.2 Setup STS-1 Interface Screen

Selecting a Transmit Timing Mode

1. Display the **SETUP STS1 INTERFACE** screen.
2. Press one of the following function keys to select a transmit timing mode:

   <recovd> — Recover received clock (i.e., loop): Network clock source does not originate with SX/13a; timing is based on the data received.

   <int> — Internal clock: SX/13a provides the network clock source based on the internal clock synthesizer or a fixed-frequency oscillator.

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

NOTE: Regardless of which transmit timing source is selected, the data rate must be set to the nominal rate that data flow through the SX/13a. For STS-1 simulations, this rate is usually 51.84 Mbps.

Selecting a BPV Error Mode

1. Display the **SETUP STS1 INTERFACE** screen.
2. Move the cursor to the BPV Error Mode field.
3. Press one of the following function keys to select a BPV error mode:

   <BpvIns> — BPV Insertion: If the data stream does not have a pulse, a pulse is injected. If a pulse is present, it is removed. If a pulse is inserted, the polarity of the inserted pulse is the same as the previous pulse, which produces improper bipolar encoding.

   <PulsRv> — Pulse Reversal: Reverses the polarity of a bipolar pulse. This polarity reversal occurs only on the second of two consecutive pulses to minimize the possibility of the reversal creating a zero-substitution pattern.

   <B3ZSds> — B3ZS Disable: Turns off the B3ZS encoding for a single substitution event. No zero-substitution occurs and the three zeros are transmitted unencoded.

   <BadSub> — Wrong Substitution: Inserts the wrong zero-substitution pattern at the next zero-substitution opportunity. Instead of alternating the zero-substitution patterns, the same pattern is incorrectly used for two successive substitutions.

Selecting a Transmit Level

1. Display the **SETUP STS1 INTERFACE** screen.
2. The transmit levels for each channel are set at the TX Cable Length East and TX Cable Length West fields. Press one of the following function keys for each field to select a cable length:

   <0-225> — Low setting for a cable length of up to 225 feet

   <225+> — High setting for a cable length of 225 feet and greater

DS3 (T3 44.736 Mbps) Interface

The DS3 (T3 44.736 Mbps) interface provides signal conversion between the SX/13a's internal format and signals complying with specifications for the 44.736 Mbps DS3 (T3) format (see Figure 3.3).

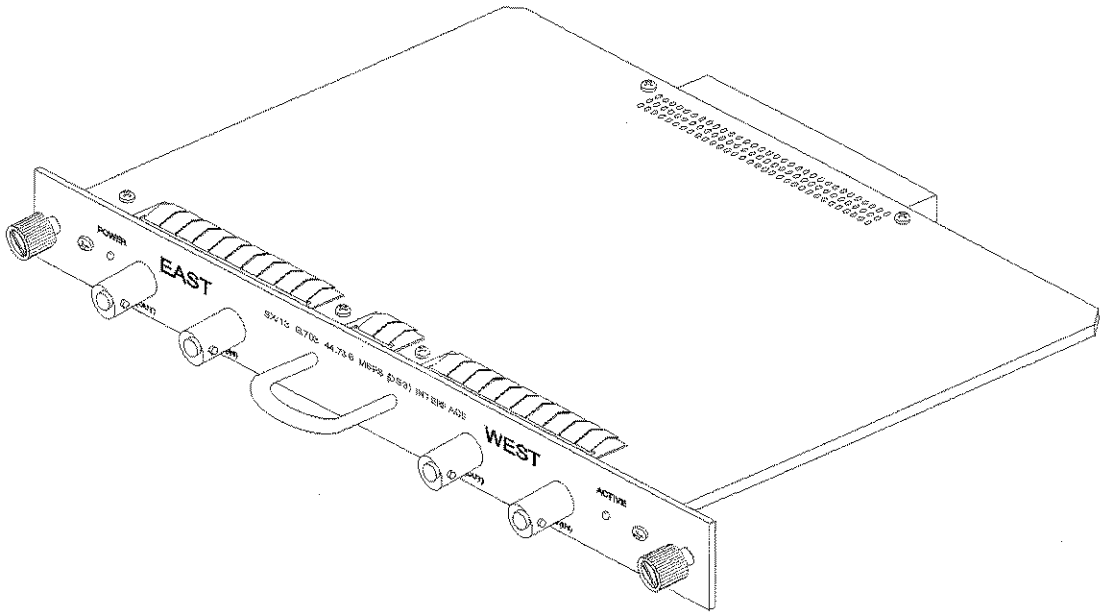

Figure 3.3 DS3 (T3 44.736 Mbps) Interface

The features and capabilities of the DS3 (T3 44.736 Mbps) interface are:

- 44.736 MHz data rate
- Accepts and generates B3ZS line coding
- Complies with the ANSI T1.102-1993 pulse shape specifications for DS3 44.736 Mbps signals
- Four BNC connectors: East receive, East transmit, West receive, West transmit
- Programmable output amplitude: Select transmit cable length on **SETUP DS3 INTERFACE** screen: low for cable lengths of 0–225 feet, or high for cable lengths of 225 feet and greater. The East and West channels are independently selectable.
- Receiver sensitivity: 550 mV–1.1 V
- Input impedance: 75 ohms

Setting Up the DS3 Interface

Use the **SETUP DS3 INTERFACE** screen to select the:

- Transmit timing mode
- BPV error mode
- Transmit level (setting based on cable length)
- Data type to transmit during a delay change

To display the **SETUP DS3 INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **DS3** and press **ENTER** to display the **SETUP DS3 INTERFACE** screen (see Figure 3.4).

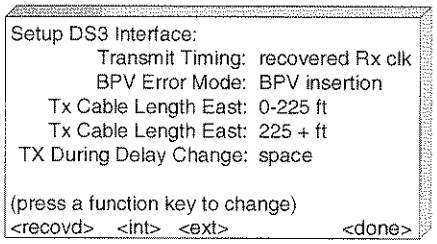

Figure 3.4 Setup DS3 Interface Screen

Selecting a Transmit Timing Mode

1. Display the **SETUP DS3 INTERFACE** screen.
2. Press one of the following function keys to select a transmit timing mode:

   <recovd> — Recover received clock (i.e., loop): Network clock source does not originate with SX/13a; timing is based on the data received.

   <int> — Internal clock: SX/13a provides the network clock source based on the internal clock synthesizer or a fixed-frequency oscillator.

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

NOTE: Regardless of which transmit timing source is selected, set the data rate to the nominal rate that data flow through the SX/13a. For DS3 simulations, this rate is usually 44.736 Mbps.

Selecting a BPV Error Mode

BPV error types are selected via the **SETUP DS3 INTERFACE** screen. The choice between logic and BPV error mode is made via the **CHANGE RANDOM ERRORS** screen. Logic errors encode B3ZS properly, but the data itself is incorrect. BPV errors create errors in the B3ZS encoding.

1. Display the **SETUP DS3 INTERFACE** screen.
2. Move the cursor to the BPV Error Mode field.
3. Press one of the following function keys to select a BPV error type:

   <BpvIns> — BPV Insertion: If the data stream does not have a pulse, a pulse is injected. If a pulse is present, it is removed. If a pulse is inserted, the polarity of the inserted pulse is the same as the previous pulse, which produces improper bipolar encoding.

   <PulsRv> — Pulse Reversal: Reverses the polarity of a bipolar pulse. This polarity reversal occurs only on the second of two consecutive pulses to minimize the possibility of the reversal creating a zero-substitution pattern.

   <B3ZSds> — B3ZS Disable: Turns off the B3ZS encoding for a single substitution event. No zero-substitution occurs and the three zeros are transmitted unencoded.

   <BadSub> — Wrong Substitution: Inserts the wrong zero-substitution pattern at the next zero-substitution opportunity. Instead of alternating the zero-substitution patterns, the same pattern is incorrectly used for two successive substitutions.

Selecting a Transmit Level

1. Display the **SETUP DS3 INTERFACE** screen.
2. Move the cursor to the TX Cable Length East field or the TX Cable Length West field. Press one of the following function keys for each field to select a cable length:

   <0-225> — Low setting for a cable length up to 225 feet

   <225+> — High setting for cable lengths of 225 feet and greater

DS1 (T1 1.544 Mbps) Interface

The DS1 (T1 1.544 Mbps) interface provides signal conversion between the SX/13a's internal format and signals complying with ITU-T specifications for the DS1 1.544 Mbps (T1) format (see Figure 3.5).

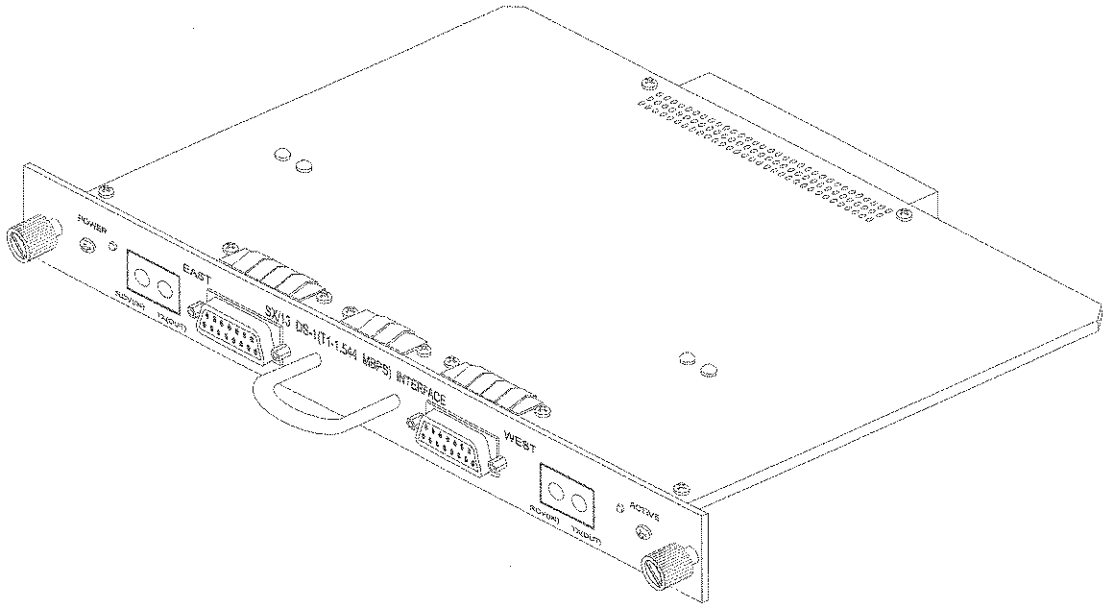

Figure 3.5 DS1 (T1 1.544 Mbps) Interface

The features and capabilities of the DS1 (T1 1.544 Mbps) interface are:

- 1.544 MHz data rate
- Accepts and generates AMI or B8ZS line coding
- Complies with the ITU-T specifications for the DS1 1.544 Mbps (T1) format
- Two dual-bantam connectors: East receive, East transmit, West receive, West transmit; two 15-pin, D-type female connectors
- Programmable output amplitude: Select transmit cable length on the **SETUP DS1 INTERFACE** screen: Five line build-outs for up to 655 feet (2.4 V–3.6 V) (3.0 V)
- Receiver sensitivity: –10 dB below DSX-1
- Input impedance: 100 ohms

Setting Up the DS1 Interface

Use the **SETUP DS1 INTERFACE** screen to select the:

- Transmit timing mode
- BPV error mode
- Line coding and transmit level (setting based on cable length)
- Data type to transmit during a delay change

To display the **SETUP DS1 INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **DS1(T1)** and press **ENTER**. The **SETUP DS1 INTERFACE** screen is displayed (see Figure 3.6).

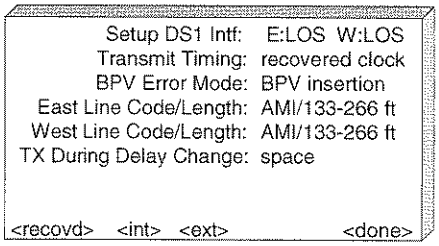

Figure 3.6 Setup DS1 Interface Screen

Selecting a Transmit Timing Mode

1. Display the **SETUP DS1 INTERFACE** screen.
2. Press one of the following function keys to select a transmit timing mode:

   <recovd> — Recover received clock (i.e., loop): Network clock source does not originate with SX/13a; timing is based on the data received.

   <int> — Internal clock: SX/13a provides the network clock source based on the internal clock synthesizer or a fixed-frequency oscillator.

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

NOTE: Regardless of which transmit timing source is selected, set the data rate to the nominal rate that data flow through the SX/13a. For DS1 simulations, this rate is usually 1.544 Mbps.

Selecting a BPV Error Mode

BPV error modes types are selected via the **SETUP DS1 INTERFACE** screen. The choice between logic and BPV error types is made via the **CHANGE RANDOM ERRORS** screen. Logic errors encode B8ZS properly, but the data itself is incorrect. BPV errors create errors in the B8ZS encoding.

1. Display the **SETUP DS1 INTERFACE** screen.
2. Move the cursor to the BPV Error Mode field.
3. Press one of the following function keys to select a BPV error mode:

   <BpvIns> — BPV Insertion: If the data stream does not have a pulse, a pulse is injected. If a pulse is present, it is removed. If a pulse is inserted, the polarity of the inserted pulse is the same as the previous pulse, which produces improper bipolar encoding.

   <PulsRv> — Pulse Reversal: Reverses the polarity of a bipolar pulse. This polarity reversal occurs only on the second of two consecutive pulses to minimize the possibility of the reversal creating a zero-substitution pattern.

   <B8ZSds> — B8ZS Disable: Turns off the B8ZS encoding for a single substitution event. No zero-substitution occurs and eight zeros are transmitted unencoded. This BPV error type has no effect on AMI encoding.

Selecting a Line Coding

1. Display the **SETUP DS1 INTERFACE** screen.
2. Move the cursor to the TX Cable Length East or TX Cable Length West field. Both the line coding selections and the transmit levels are set in these fields.
3. Press one of the following function keys to select a line coding:

   <B8ZS> — Bipolar with 8-zero substitution

   <AMI> — Alternate mark inversion
4. Use the right arrow cursor key to select a transmit level.

Selecting a Transmit Level

For T1 DSX-1 applications, East and West cable lengths can be set ranging from 0 to 655 feet, as measured from the transmitter to the DSX-1 cross-connect.

1. Display the **SETUP DS1 INTERFACE** screen.
2. Move the cursor to the TX Cable Length East or TX Cable Length West field. Both the line coding selections and the transmit levels are set in these fields.
3. Use the right arrow cursor key to select one of the following transmit levels:

   <0-133> — For a cable length of 0 to 133 feet

   <to 266> — For a cable length of 134 to 266 feet

   <to 399> — For a cable length of 267 to 399 feet

   <to 533> — For a cable length of 400 to 533 feet

   <to 655> — For a cable length of 534 to 655 feet

Connector Pin Assignments

The network connector for the DS1 interface is a 15-pin, D-type, female connector (see Table 3.1).

Table 3.1 DS1 Connector Pin Assignments

Pin	Signal
1	Send to network tip
9	Send to network ring
2	Chassis ground
3	Receive from network tip
11	Receive from network ring
4	Chassis ground

G.703 (E3 34.368 Mbps) Interface

The G.703 (E3 34.368 Mbps) interface provides signal conversion between the SX/13a's internal format and signals complying with specifications for the 34.368 Mbps G.703 (E3) format (see Figure 3.7).

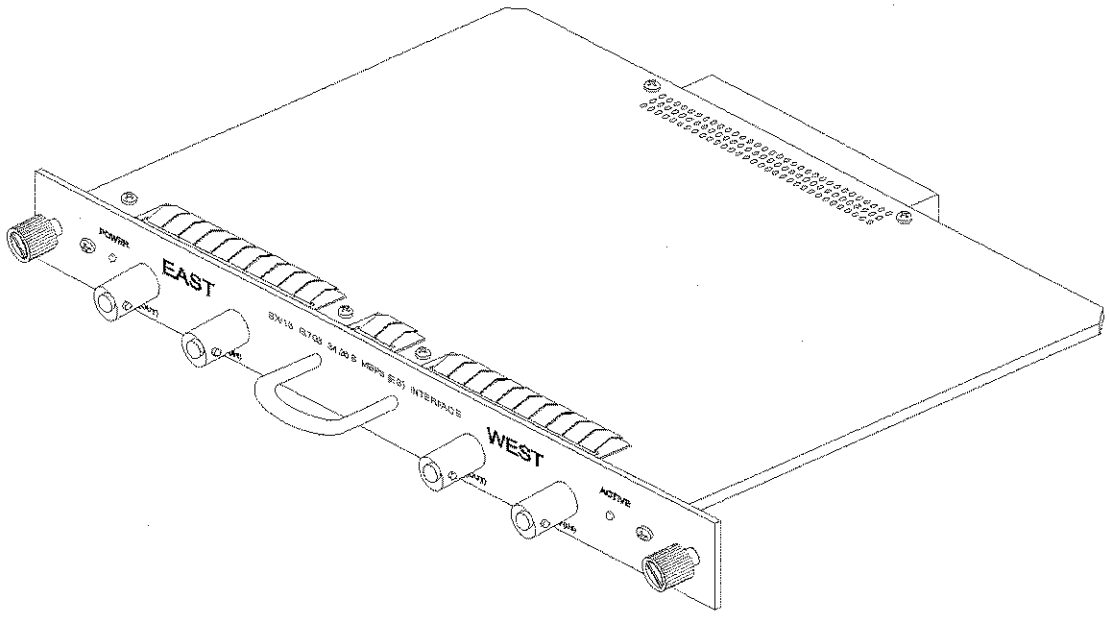

Figure 3.7 G.703 (E3 34.368 Mbps) Interface

The features and capabilities of the G.703 (E3 34.368 Mbps) interface are:

- 34.368 MHz data rate
- Accepts and generates HDB3 line coding
- Complies with the ITU-T Recommendation G.703 Physical/Electrical Characteristics of Hierarchical Digital Interfaces
- Four BNC connectors: East receive, East transmit, West receive, West transmit
- Receiver sensitivity: 550 mV–1.1 V
- Input impedance: 75 ohms

Setting Up the G.703 (E3) Interface

Use the **SETUP E3 INTERFACE** screen to select the:

- Transmit timing mode
- BPV error mode
- Transmit level
- Data type to transmit during a delay change

To display the **SETUP E3 INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **E3** and press **ENTER** to display the **SETUP E3 INTERFACE** screen (see Figure 3.8).

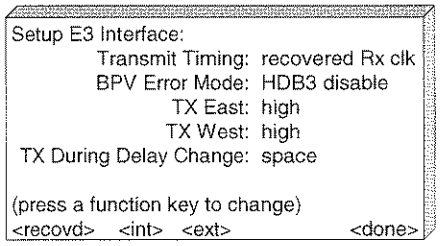

Figure 3.8 Setup E3 Interface Screen

Selecting a Transmit Timing Mode

1. Display the **SETUP E3 INTERFACE** screen.
2. Press one of the following function keys to select a transmit timing mode:

   <recovd> — Recover received clock (i.e., loop): Network clock source does not originate with SX/13a; timing is based on the data received.

   <int> — Internal clock: SX/13a provides the network clock source based on the internal clock synthesizer or a fixed-frequency oscillator.

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

NOTE: Regardless of which transmit timing source is selected, set the data rate to the nominal rate that data flow through the SX/13a. For E3 simulations, this rate is usually 34.368 Mbps.

Selecting a BPV Error Mode

BPV error types are selected via the **SETUP E3 INTERFACE** screen. The choice between logic and BPV error mode is made via the **CHANGE RANDOM ERRORS** screen. Logic errors encode HDB3 properly, but the data itself is incorrect. BPV errors create errors in the HDB3 encoding.

1. Display the **SETUP E3 INTERFACE** screen.
2. Move the cursor to the BPV Error Mode field.

3. Press one of the following function keys to select a BPV error mode:

   <BpvIns> — BPV Insertion: If the data stream does not have a pulse, a pulse is injected. If a pulse is present, it is removed. If a pulse is inserted, the polarity of the inserted pulse is the same as the previous pulse, which produces improper bipolar encoding.

   <PulsRv> — Pulse Reversal: Reverses the polarity of a bipolar pulse. This polarity reversal occurs only on the second of two consecutive pulses to minimize the possibility of the reversal creating a zero-substitution pattern.

   <HDB3ds> — HDB3 Disable: Turns off the HDB3 encoding for a single substitution event. No zero-substitution occurs, and the four zeros are transmitted unencoded.

   <BadSub> — Wrong Substitution: Inserts the wrong zero-substitution pattern at the next zero-substitution opportunity. Instead of alternating the zero-substitution patterns, the same pattern is incorrectly used for two successive substitutions.

Selecting a Transmit Level

1. Display the **SETUP E3 INTERFACE** screen.
2. The transmit levels for each channel are set in the TX Level East and TX Level West fields. Press one of the following function keys for each to select a transmit level:

   <Low> — Low setting. For special applications.

   <High> — High setting. This level meets the G.703 pulse mask requirements.

G.703 (E1 2.048 Mbps) Interface

The G.703 (E1 2.048 Mbps) interface provides TTL conversion between the SX/13a's internal format and signals complying with ITU-T specifications for the 2.048 Mbps G.703 (E1) format (see Figure 3.9).

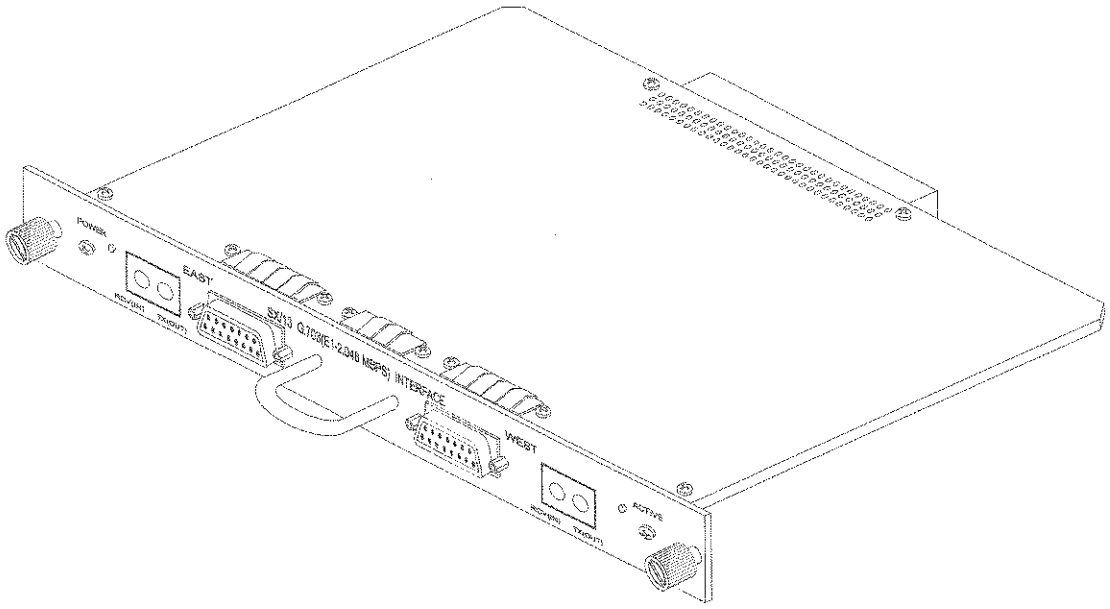

Figure 3.9 G.703 (E1 2.048 Mbps) Interface

The features and capabilities of the G.703 (E1 2.048 Mbps) interface are:

- 2.048 MHz data rate
- Accepts and generates HDB3 line coding
- Complies with the ITU-T Recommendation G.703 Physical/Electrical Characteristics of Hierarchical Digital Interfaces
- Two dual-bantam connectors: East receive, East transmit, West receive, West transmit; two 15-pin, D-type female connectors
- Output amplitude: 2.37 V (75-ohm coaxial cable setting) or 3.0 V (120-ohm twisted pair setting)
- Receiver sensitivity: –12 dB (1.5 Vpp)
- Input impedance: 75 ohms (coaxial cable) or 120 ohms (twisted pair cable)

Setting Up the G.703 (E1) Interface

Use the **SETUP G.703 (E1) INTERFACE** screen to set the:

- Transmit timing mode
- BPV error mode
- Receiver impedance
- Data type to transmit during a delay change

To display the **SETUP G.703 (E1) INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select G.703 (E1) and press enter to display the **SETUP G.703 (E1) INTERFACE** screen (see Figure 3.10).

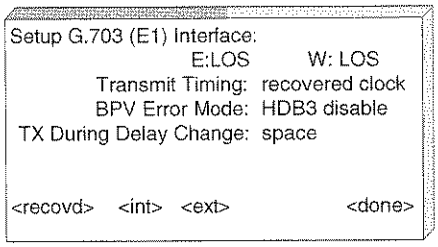

Figure 3.10 Setup G.703 (E1) Interface Screen

Selecting a Transmit Timing Mode

1. Display the **SETUP G.703 (E1) INTERFACE** screen.
2. Press one of the following function keys to select a transmit timing mode:

   <recovd> — Recover received clock (i.e., loop): Network clock source does not originate with SX/13a; timing is based on the data received.

   <int> — Internal clock: SX/13a provides the network clock source based on the internal clock synthesizer or a fixed-frequency oscillator.

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

*CAUTION! The data rate **must** be set to 2.048 MHz for proper operation with the E1 interface, regardless of which transmit timing source is selected.*

Selecting a BPV Error Mode

BPV error types are selected via the **SETUP G.703 (E1) INTERFACE** screen. The choice between logic and BPV error mode is made via the **CHANGE RANDOM ERRORS** screen. Logic errors encode HDB3 properly, but the data itself is incorrect. BPV errors create errors in the HDB3 encoding.

1. Display the **SETUP G.703 (E1) INTERFACE** screen.
2. Move the cursor to the BPV Error Mode field.
3. Press one of the following function keys to select a BPV error mode:

   <BpvIns> — BPV Insertion: If the data stream does not have a pulse, a pulse is injected. If a pulse is present, it is removed. If a pulse is inserted, the polarity of the inserted pulse is the same as the previous pulse, which produces improper bipolar encoding.

   <PulsRv> — Pulse Reversal: Reverses the polarity of a bipolar pulse. This polarity reversal occurs only on the second of two consecutive pulses to minimize the possibility of the reversal creating a zero-substitution pattern.

   <HDB3ds> — HDB3 Disable: Turns off the HDB3 encoding for a single substitution event. No zero-substitution occurs, and the four zeros are transmitted unencoded.

   <BadSub> — Wrong Substitution: Inserts the wrong zero-substitution pattern at the next zero-substitution opportunity. Normally, the HDB3 zero-substitution encoding scheme has an odd number of pulses between violations. When a wrong substitution BPV is inserted, an even number of pulses occurs between violations.

Selecting a Receiver Impedance

The receiver impedance for East and West channels for the G.703 (E1 2.048 Mbps) interface is changed by removing the jumper pin covers on the jumper pins and replacing them to connect a different set of jumper pins. Both sets of jumper pins are located on the interface (see Figure 3.11). The two input impedance values are:

- 75 ohms for coaxial cable
- 120 ohms for twisted pair cable

The default input impedance is 120 ohms. The jumpers consist of two sets of jumpers: one for the West channel, and one for the East channel. Each set of jumpers includes four jumpers with three pins each. Two of the three pins for each jumper should be set. Each setting — 75 and 120 — is indicated on the interface, as shown in Figure 3.12 and Figure 3.13, respectively.

To select a receiver impedance:

1. Follow the instructions for preventing electrostatic discharge on page 1-2.
2. Turn off the SX/13a.
3. Remove the E1 interface. The jumpers are located on the component side of the board.
4. Remove the plastic jumper pin covers from each jumper that needs to be set.
5. Replace the jumper pin covers over the pins according to the diagram.

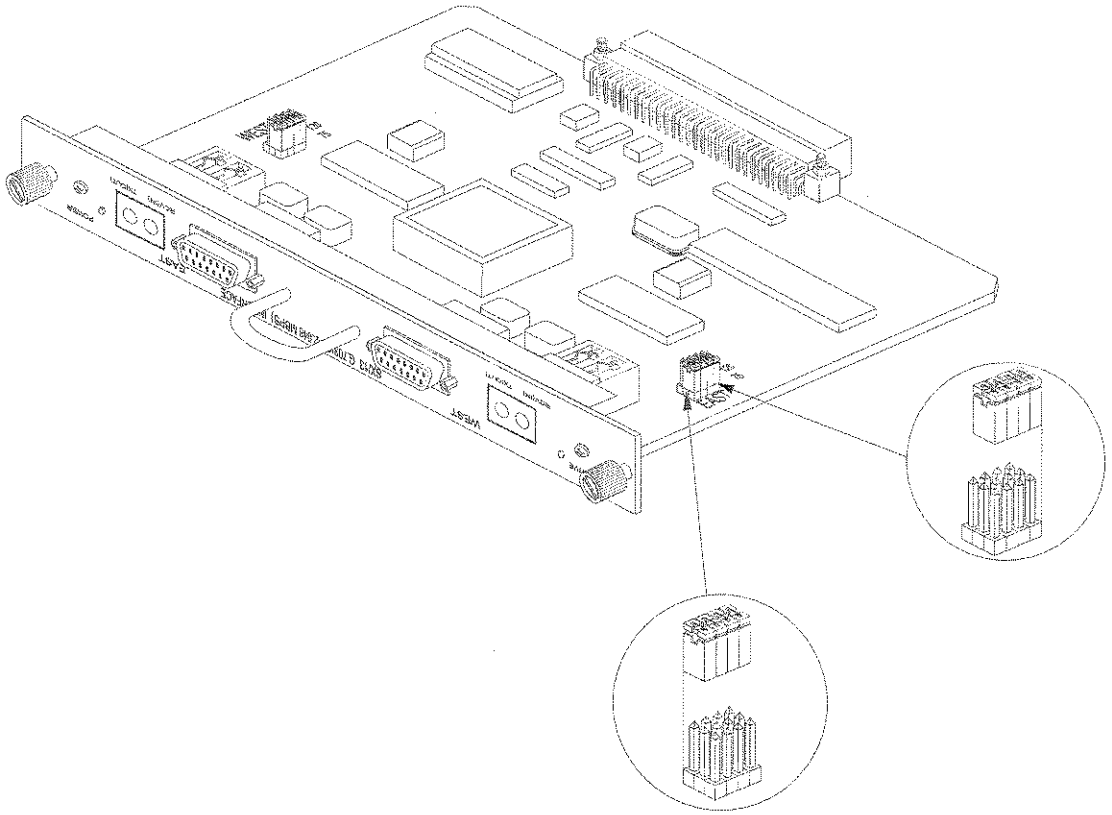

Figure 3.11 G.703 (E1 2.048 Mbps) Interface Jumper Locations

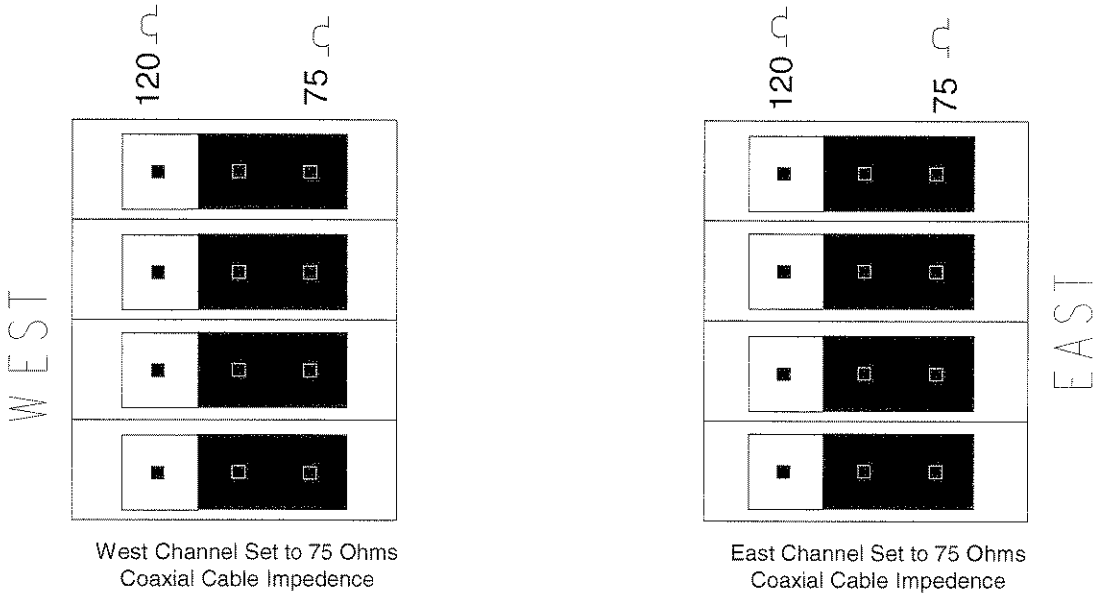

Figure 3.12 E1 75-ohm Jumper Setting

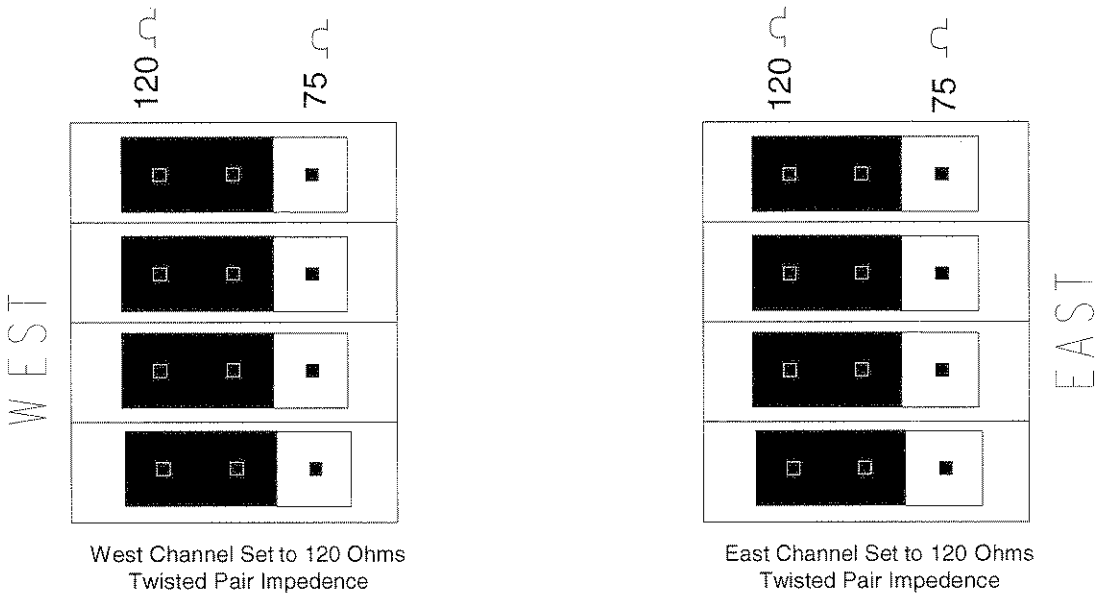

Figure 3.13 E1 12-ohm Jumper Setting (Default)

High Speed Serial Interface (HSSI)

The HSSI interface converts TTL signals used within the SX/13a and signals complying with the industry standard HSSI interface specification created by Cisco Systems and T3 Plus Networking. (Revision 2.11-3). The interface features East and West HSSI 50-pin female connectors for connecting two pieces of data terminal equipment (DTE).

The HSSI interface permits the SX/13a to simulate the link as well as the data service units (DSUs) that would be present in an actual system (see Figure 3.14).

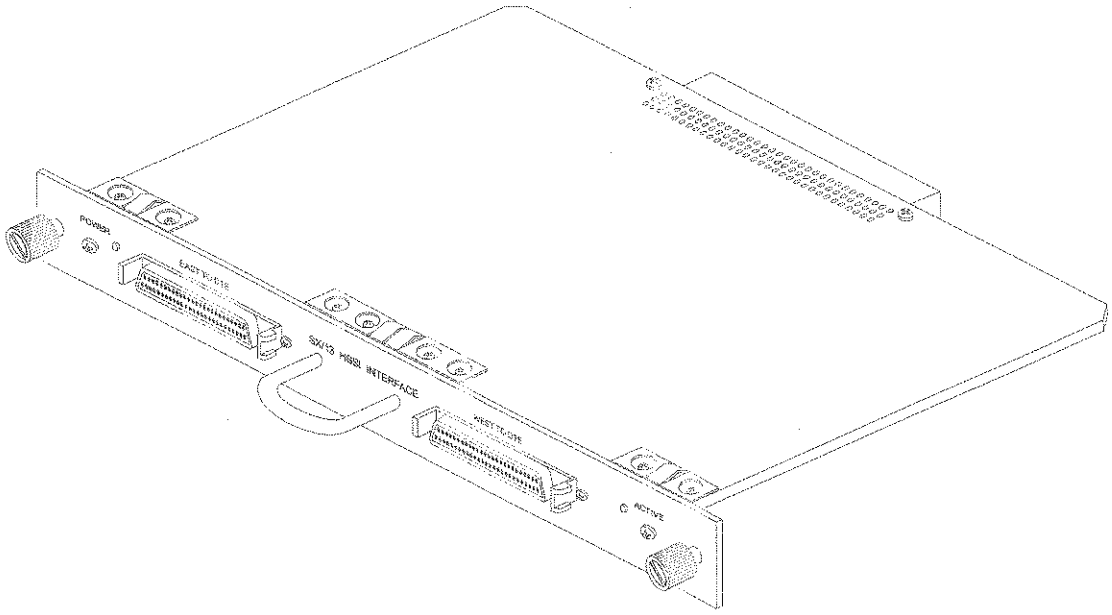

Figure 3.14 HSSI Interface

The features and capabilities of the HSSI interface are:

- 51.84 MHz data rate
- Complies with the Cisco Systems and T3 Plus Networking Revision 2.11-3 HSSI interface specifications
- Two 50-pin HSSI connectors
- Input impedance: 110 ohms

Setting Up the HSSI Interface

Use the **SETUP HSSI INTERFACE** screen to select the:

- Line type
- Transmit timing source and mode
- Line rate and payload ratio, if manually entering a line type
- Data type to transmit during a delay change

To display the **SETUP HSSI INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **HSSI** and press **ENTER** to display the **SETUP HSSI INTERFACE** screen (see Figure 3.15).

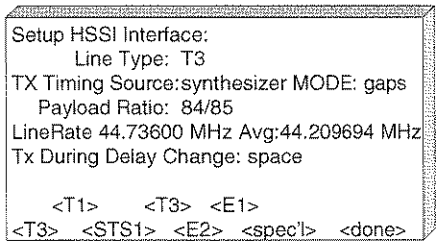

Figure 3.15 Setup HSSI Interface Screen

Selecting a Line Type

Selecting a standard line type automatically sets the correct payload ratio and corresponding line rate. Selecting a special line type requires manually entering a line rate and payload ratio.

1. Display the **SETUP HSSI INTERFACE** screen.
2. Choose a line type. Table 3.2 lists the line types and corresponding payload ratios, line rates, and clock rate average.

Table 3.2 HSSI Line Types, Payload Ratios, Line Rates, and Clock Rate Averages

Line Type	Payload Ratio	Line Rate (MHz)	Average (MHz)
T3	84/85	44.736000	44.209694
T1	192/193	1.544000	1.536000
STS-1	696/720	51.840000	50.112000
E3	1512/1536	34.368000	33.831000
E2	824/848	8.448000	8.208905
E1	248/256	2.048000	1.984000
spec'l	Manually entered if gapped clock	Manually entered	

Setting a Transmit Timing Source and Mode

The HSSI interface can operate in internal or external clock mode. Both of these can be set to continuous or gapped. A gapped clock has pulses missing periodically to simulate the effect of a DSU, which may remove clock pulses to insert line format framing bits, such as for T3 circuits. The payload is the number of data bits per frame. The payload ratio is the number of data bits divided by the frame length. Gaps are dependent on the payload ratio. The more overhead bits, the less payload bits. Thus, as overhead increases, the payload ratio decreases.

Setting the Transmit Timing Source for Any Line Type

1. Display the **SETUP HSSI INTERFACE** screen.
2. Move the cursor to the TX Timing Source field.
3. Press one of the following function keys to select a timing source:

   <ext> — External clock: Network clock is provided by the SX/13a, but the timing source is from the clock connected via the external clock input.

   <synth> — Internal clock: The SX/13a's internal frequency synthesizer provides the transmit timing for clock rates up to 51.84 MHz, which is the maximum speed of the synthesizer.

   <osc> (only available for a line type of "special") — Internal clock: Two oscillators on the HSSI interface provide the timing source. The 44.736000 MHz oscillator provides an 84/85 gapped clock with an average rate of 44.209694 MHz. This is a clock type that some T3 DSUs provide to the DTE. The 44.209694 MHz oscillator provides a continuous clock of the same average frequency as the gapped 44.736000 MHz oscillator. Some T3 DSUs provide this type of continuous clock instead of a gapped clock.

NOTE: These oscillators can be replaced to support other pairs of gapped and continuous frequencies. Contact Spirent Communications for more information about this option.

Setting the Timing Source Mode

1. Display the **SETUP HSSI INTERFACE** screen.
2. Move the cursor to the Mode field.
3. Press one of the following function keys to select a timing source mode:

   <gaps> — Gapped clock

   <cont> — Continuous clock

Defining the Payload Ratio

Defining a payload ratio is only necessary when a line type of "special" is set to gapped clock mode.

1. Select **<spec'l>** to choose a non-standard line type and **<gaps>** to choose gapped clock mode.
2. Move the cursor to the Payload Ratio field and press **ENTER. THE HSSI INTERFACE – SET PAYLOAD RATIO** screen is displayed.
3. Enter a bit value for the payload. This represents the non-overhead portion of the frame, which includes data bits, but not framing bits.
4. Enter a bit value for the frame length. This represents the entire value of the frame, which includes data bits and framing bits.

HSSI Payload Ratio Example

The T1 frame consists of 24 time slots, each with 8 bits of information for a total of 192 bits (24 x 8 = 192). A 193rd bit is added to mark the end of one frame and the beginning of the next. The T1 payload ratio is 192/193, which means there are 192 payload bits, 193 total bits, and 1 overhead bit.

Setting the Line Rate

The line rate is automatically set for the standard line types. Manually set a line rate for a line type of "special." The line rate is set to the value of the average clock rate as displayed on the **SETUP HSSI INTERFACE** screen.

The line rate is displayed on the **MAIN PARAMETERS** screen, but cannot be changed via the **CHANGE DATA RATE** screen as the line rate for other interfaces. Attempts to change the data rate for the HSSI interface from the **MAIN PARAMETERS** screen result in an error message.

NOTE: When operating above 34.368 MHz on external clock, it is recommended that the HSSI interface be the only high-speed interface plugged in to the SX/13a's rear panel. If other high-speed interfaces are installed at the same time, the duty cycle requirements of the HSSI clock cannot be guaranteed above this frequency and unexpected errors may result.

Connector Pin Assignments

Table 3.3 HSSI East and West Connector Pin Assignments

Pin	Circuit	Signal	Lead Status
1,26	SG	Signal ground	Signal ground reference
2,27	RT (+,-)	Receive timing	Output: receive clock to DTE
3,28	CA	DCE available	Output: always asserted by SX/13a
4,29	RD (+,-)	Receive data	Output: receive data to DTE
5,30	LC (+,-)	Loopback circuit C	Output: not asserted by SX/13a
6,31	ST (+,-)	Send timing	Output: transmit timing to DTE
7,32	SG	Signal ground	Signal ground reference
8,33	TA (+,-)	DTE available	Input: ignored by SX/13a
9,34	TT (+,-)	Terminal timing	Input: transmit timing from DTE
10,35	LA (+,-)	Loopback circuit A	Input: loopback command A to SX/13a
11,36	SD (+,-)	Send data	Input: transmit data from DTE
12,37	LB (+,-)	Loopback circuit B	Input: loopback command B to SX/13a
13,38	SG	Signal ground	Signal ground reference
19,44	SG	Signal ground	Signal ground reference
25,50	SG	Signal ground	Signal ground reference

Data and Timing Leads

Table 3.4 HSSI Data and Timing Leads

Circuit	Signal	Lead Status
RT	Receive timing	A gapped or continuous clock at a maximum bit rate of 51.84 Mbps. Provides receive timing information for receive data (RD).
RD	Receive data	Data output to the DTE from the SX/13a's simulated channel.
ST	Send timing	A gapped or continuous clock at a maximum bit rate of 51.84 Mbps. Provides transmit data timing information to the DTE.
TT	Terminal timing	Provides transmit data timing information back to the SX/13a (the DCE). Terminal timing (TT) is send timing (ST) echoed back to the SX/13a by the DTE.
SD	Send data	Data received from the DTE equipment that will be transmitted to the SX/13a's simulated channel. Send data (SD) is synchronous to terminal timing (TT).

Signalling Leads

Table 3.5 HSSI Signalling Leads

Circuit	Signal	Lead Status
TA	Data terminal equipment available	Provided by the DTE to the SX/13a to indicate that the DTE is prepared to send and receive data.
CA	Data communications equipment available	Provided by the SX/13a to the DTE to indicate that the SX/13a is prepared to send and receive data.

Loopback Leads

Table 3.6 HSSI Loopback Leads

Circuit	Signal	Lead Status
LA, LB	Loopback circuits A and B	Request for loopback by the DTE is coded as follows: LB=0, LA=0: No loopback LB=1, LA=1: Local DTE loopback (SX/13a does outward loopback) LB=0, LA=1: Local line loopback (SX/13a does outward loopback) LB=1, LA=0: Remote line loopback (SX/13a does inward loopback) A request for loopback from either DTE interface will cause loopback to occur on both interfaces.
LC	Loopback circuit C	DTE loopback signal used to request that the DTE loopback its ST to TT, and RD to SD for testing purposes. The SX/13a does not assert this signal.

V.35 Interface

The V.35 interface provides signal conversion between the SX/13a's internal format and signals complying with ITU-T Recommendation V.35. This interface features East and West 34-pin Winchester MRA-34-P-JTC6-H8 (female) connectors (see Figure 3.16).

The V.35 interface can be used to connect data terminal equipment (DTE) in a DTE-to-DTE configuration, and DTE to data communications equipment (DCE) in a DTE-to-DCE configuration. The East connector is always a DTE connection. The West connector can connect to DTE or DCE.

The V.35 interface uses high-speed, balanced V.35-type clock drivers, data drivers, and receivers. All signalling drivers and receivers are unbalanced RS-232-C type.

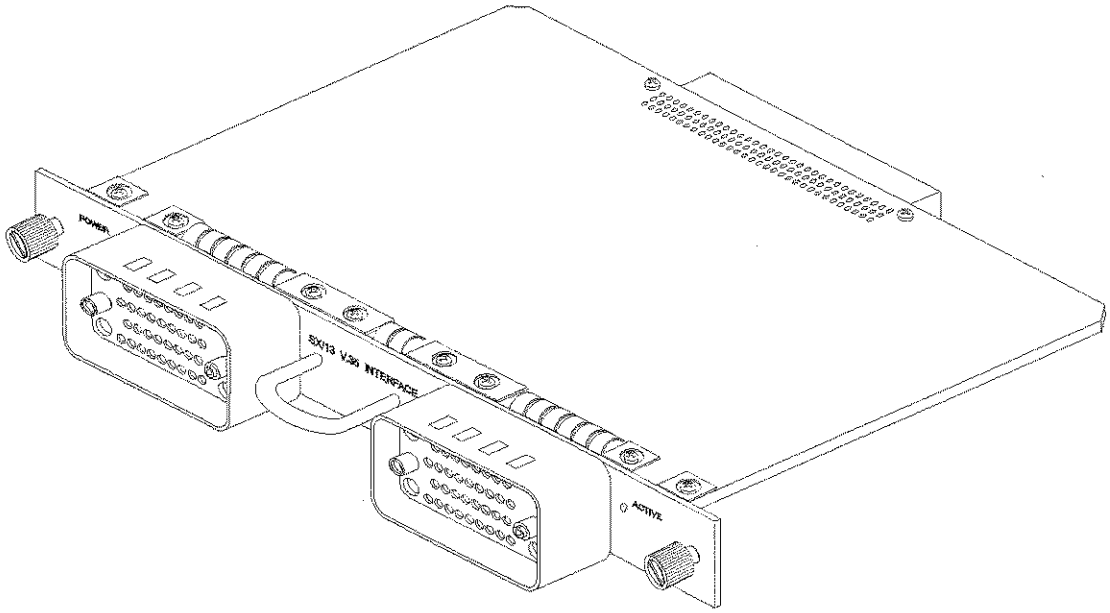

Figure 3.16 V.35 Interface

The features and capabilities of the V.35 interface are:

- Complies with the ITU-T recommendation for V.35
- Two 34-pin V.35 connectors (Winchester MRA-34-P-JTC6-H8)
- Input impedance for clock and data lines: 100 ohms
- Input impedance for signalling lines: 3,000–7,000 ohms
- Output amplitude for clock and data lines: +/– 1.10 Vpp
- Output amplitude for signalling lines: +/– 10 V

Setting Up the V.35 Interface

Use the SETUP V.35 INTERFACE screen to select the:

- Data mode
- East/West connector type
- Channel timing
- Data type to transmit during delay change
- Loop timing setting

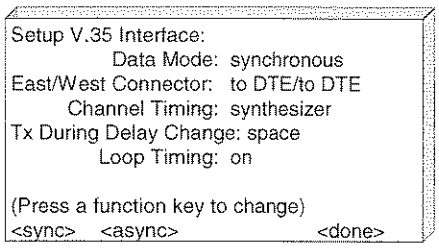

Figure 3.17 Setup V.35 Interface Screen

Setting the Data Mode

The asynchronous mode allows the SX/13a to be used with low-speed asynchronous data (data with no accompanying clock). This is accomplished by operating the SX/13a in its internal clock mode and at a rate that is 10 times the baud rate of the data. Each data bit is sampled approximately 10 times and appears at the output of the SX/13a channel as the original data bit with a small sampling error due to the asynchronous sampling by the internal clock. Jitter caused by the 10-times over-sampling will be at worst 10 percent of the data bit. The SX/13a data rate in this mode is measured in baud (Bd). In the synchronous mode, the unit is hertz (Hz).

For example, if the data rate parameter is set to 9600 baud, the internal clock of the SX/13a will automatically be adjusted to 96,000 Hz.

Errors injected in the asynchronous mode have slightly different characteristics from synchronous errors. Synchronous mode error events are 1 or more bits wide in increments of a bit. Asynchronous errors are 1/10th of a bit wide and occur 10 times more frequently due to the over-sampling. The net result is the correct error rate but with a finer distribution of the error events. When analyzing the SX/13a's error statistics in asynchronous mode, keep in mind that the error counts are counting 1/10th of a bit error events, so there will be 10 times as many of them as expected.

From the SETUP V.35 INTERFACE screen:

1. Move cursor to the Data Mode field.
2. Use the function keys to select **<sync>** for synchronous or **<async>** for asynchronous.

Selecting a Connector

The East channel is always set to DTE; the West channel can be set to DCE or DTE.

1. Display the **SETUP V.35 INTERFACE** screen.
2. Move the cursor to the East/West Connector field. The West connector is highlighted.
3. Press one of the following function keys to select an equipment type:

   <DTE> — DTE-to-DTE: In this mode, both the East and West connectors are connected to DTEs.

   <DCE> — DTE-to-DCE: In this mode, the East connector is connected to a DTE and the West connector is connected to a DCE.

Selecting Channel Timing

The channel timing for the V.35 interface depends on the data mode selection (synchronous or asynchronous) and data equipment simulation (DTE-to-DTE or DTE-to-DCE). Channel timing can only be set for synchronous operations. If asynchronous data mode is selected, the channel timing is automatically set to sampling. Once the data mode is set to synchronous, the East/West connectors, channel timing, and loop on or off can be selected.

In synchronous DTE-to-DTE, the internal clock synthesizer, external clock source, or the connected DTE can provide timing. Further, when using the internal clock synthesizer or external clock mode, loop timing can be set to on or off. The loop off setting provides the DTE with transmit and receive clocks. With the loop on setting, the SX/13a (either the internal clock synthesizer or an external clock source connected to the unit) provides the DTE with the receive clocks and the DTEs use the SX/13a clock as a transmit clock source.

In synchronous DTE-to-DCE configuration, timing can be provided from the DCE, or from the DTE and the DCE.

Refer to Table 3.7 for the correlation among hardware configurations, onscreen selections, and the diagrams that illustrate the internal functioning of the received and transmit paths for data and clock for each mode.

Table 3.7 V.35 Channel Timing Configuration

Configuration	Selections Onscreen	Description	Figure
Synchronous DTE-to-DTE without loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <off>	The internal frequency synthesizer or external clock source connected to the SX/13a provides the DTE with transmit and receive clocks.	Figure 3.18
Synchronous DTE-to-DTE with loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <on>	The internal frequency synthesizer or external clock source connected to the SX/13a provide the DTE with the receive clock. The SX/13a clock provides the transmit clock source for the DTE.	Figure 3.19
Synchronous DTE-to-DTE with DTE timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: <DTE>	The DTEs provide their own transmit clock timing to the SX/13a.	Figure 3.20
Synchronous DTE-to-DCE with DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DCE> (from DCE)	The DCE provides both transmit and receive clocks for the East and West connectors.	Figure 3.21
Synchronous DTE-to-DCE with DTE & DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DTE> (from DTE & DCE)	The DTE and DCE provide their own transmit clocks.	Figure 3.22

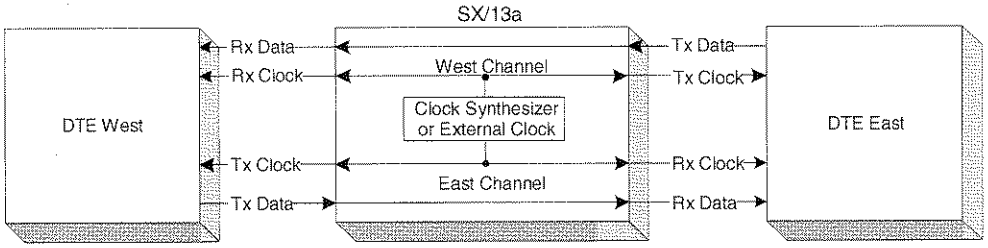

Figure 3.18 DTE-to-DTE Synthesizer or External Clock Mode with Loop Timing Off

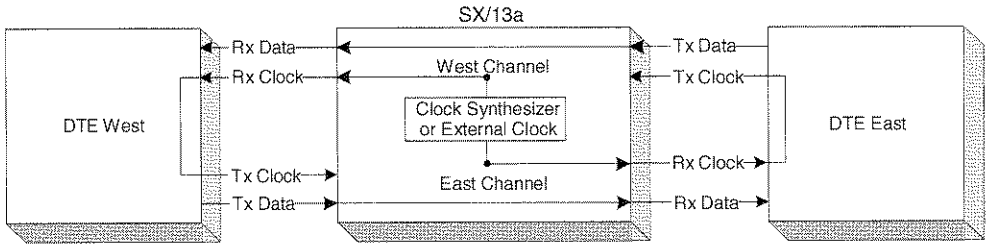

Figure 3.19 DTE-to-DTE Synthesizer or External Clock Mode with Loop Timing On

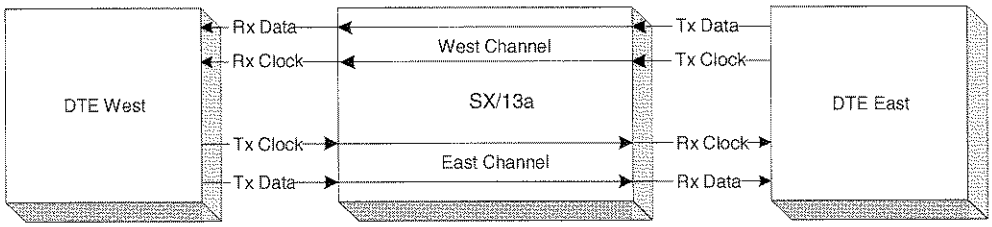

Figure 3.20 DTE-to-DTE Channel Timing from DTEs

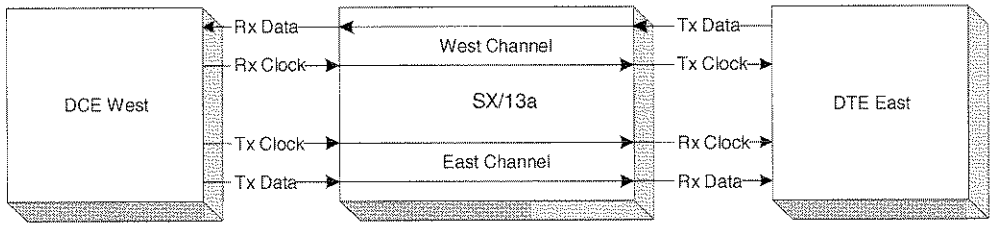

Figure 3.21 DTE-to-DCE Channel Timing from DCE

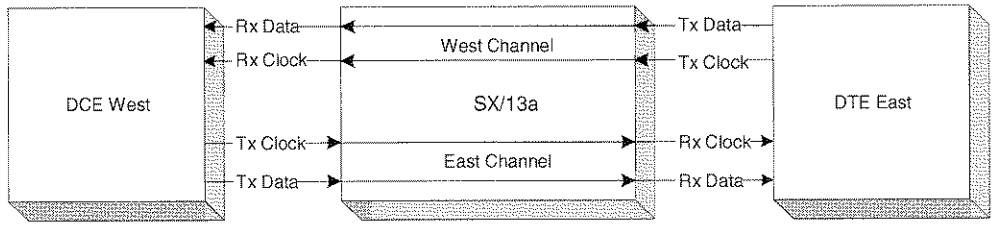

Figure 3.22 DTE-to-DCE Channel Timing from DTE & DCE

Setting the Channel Timing for Synchronous DTE-to-DTE

The channel timing and loop timing options are unique to synchronous DTE-to-DTE.

1. From the **SETUP V.35 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to DTE. The East connector is not selectable. Selecting synchronous DTE-to-DTE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DTE channel timing:

   <synth> (loop timing off) — Synthesizer: The internal frequency synthesizer provides the DTEs with transmit and receive clocks.

   <synth> (loop timing on) — Synthesizer: The internal frequency synthesizer provides the DTEs with receive clocks. The DTEs use the clock from the SX/13a as a transmit clock source.

   <ext> (loop timing off) — External clock: This mode is the same as the Synthesizer (loop timing off) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <ext> (loop timing on) — External clock: This mode is the same as the Synthesizer (loop timing on) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <DTE> — From DTE: The DTEs provide their own transmit clocks to the SX/13a.

Synthesizer or external clock mode enables loop timing. The loop "off" setting provides the DTE with transmit and receive clocks. The loop "on" setting provides the DTE with the receive clocks, and the DTEs use the SX/13a clock as a transmit clock source.

Setting the Channel Timing for Synchronous DTE-to-DCE

The channel timing options are unique to synchronous DTE-to-DCE.

1. From the **SETUP V.35 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to DCE. The East connector is not selectable. Selecting synchronous DTE-to-DCE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DCE channel timing:

   <DCE> — From DCE: The DCE provides both the transmit and receive clocks for the East and West connectors.

   <DTE> — From DTE & DCE: The DTE and DCE provide their own transmit clocks.

Connector Pin Assignments

Table 3.8 through Table 3.10 show the connector pin assignments for the East and West connectors to DTE, and the West connector to DCE. The V.35 connectors are 37-pin, D-type female connectors.

Table 3.8 V.35 East Connector to DTE

Pin	Circuit	Signal	Lead Status
A	AA	Protective ground	Strapped to interface panel
B	AB	Signal ground	Internally connected to circuit ground
C	CA	Request to send	Input
D	CB	Clear to send	Output
E	CC	Data set ready	Output
F	CF	Received line signal detector	Output (internally forced on)
H		Data terminal ready	Input
P, S	SD (A, B)	Send data	West channel data input
R, T	RD (A, B)	Received data	East channel data output
U, W	SCTE (A, B)	Serial clock transmit external	Input
V,X	SCR (A,B)	Serial clock receive	Output
Y,a	SCT (A,B)	Serial clock transmit	Output

Table 3.9 V.35 West Connector to DTE

Pin	Circuit	Signal	Lead Status
A	AA	Protective ground	Strapped to interface panel
B	AB	Signal ground	Internally connected to circuit ground
C	CA	Request to send	Input (internally looped to CTS)
D	CB	Clear to send	Output (internally looped to RTS)
E	CC	Data set ready	Output (internally forced on)
F	CF	Received line signal detector	Output (internally forced on)
H		Data terminal ready	No connection
P, S	SD (A, B)	Send data	East channel data inputs
R, T	RD (A, B)	Received data	West channel data output
U, W	SCTE (A, B)	Serial clock transmit external	Input
V, X	SCR (A, B)	Serial clock receive	Output
Y,a	SCT (A, B)	Serial clock transmit	Output

Table 3.10 V.35 West Connector to DCE

Pin	Circuit	Signal	Lead Status
A	AA	Protective ground	Strapped to interface panel
B	AB	Signal ground	Internally connected to circuit ground
C	CA	Request to send	Output
D	CB	Clear to send	Input
E	CC	Data set ready	Input
F	CF	Received line signal detector	Input (not used)
H		Data terminal ready	Output
P, S	SD (A, B)	Send data	West channel data output
R, T	RD (A, B)	Received data	East channel data input
U, W	SCTE (A, B)	Serial clock transmit external	Output
V, X	SCR (A, B)	Serial clock receive	Input
Y, a	SCT (A, B)	Serial clock transmit	Input

Signalling Leads

In the DTE-to-DTE configuration for the East/West connector, the clear to send (CTS) and request to send (RTS) are connected, and data set ready (DSR) and data carrier detect (DCD) are held on at each connector.

In the DTE-to-DCE configuration, when the delay is greater than "0" for the East connector, the CTS and RTS are connected, and DSR and DCD are held on. For the West connector, the RTS is held on.

In the DTE to-DCE when the delay is equal to "0", the following conditions apply for the East/West connector:

- CTS (East) connected to CTS (West)
- RTS (East) connected to RTS (West)
- DSR (East) connected to DSR (West)
- DTR (East) connected to DTR (West)

RS-449 (RS-422-A) Interface

The RS-449 (RS-422-A) interface provides signal conversion between the SX/13a's internal TTL format and signals complying with EIA standard RS-422-A. The interface features East and West 37-pin female, D-type connectors for connecting DTEs in a DTE-to-DTE configuration, and for connecting DTEs to a data connecting equipment (DCE) configuration. A 37-pin, D-type adapter with male connectors on each end may be required for connecting equipment in a DTE-to-DCE configuration.

The East connector is *always* a DTE connection. The West connector can be either a DTE or DCE connection (see Figure 3.23).

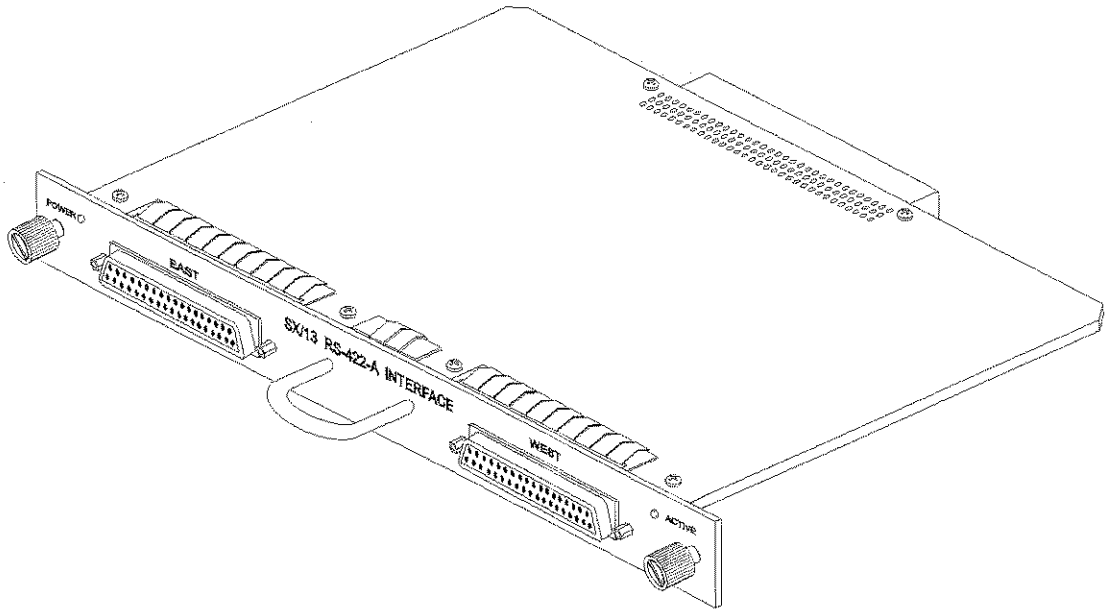

Figure 3.23 RS-449 (RS-422-A) Interface

The features and capabilities of the RS-449 (RS-422-A) interface are:

- 10 Mbps data rate
- Complies with EIA standard RS-422-A
- Two 37-pin female, D-type connectors: East is DTE; West may be either DTE or DCE
- Input impedance: 100 ohms

Setting Up the RS-449 (RS-422-A) Interface

Use the **SETUP RS-422 INTERFACE** screen to select the:

- Data mode
- East/West connector type
- Channel timing
- Data type to transmit during a delay change
- Loop timing setting

To display the **SETUP RS-422 INTERFACE** screen:

1. Press **MENU**.
2. Selet **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **RS-422** and press **ENTER** to display the **SETUP RS-422 INTERFACE** screen (see Figure 3.24).

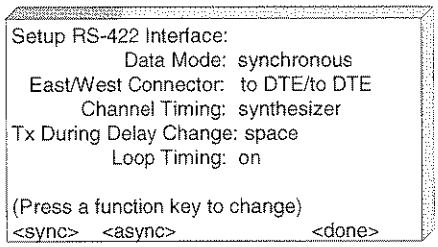

Figure 3.24 Setup RS-422 Interface Screen

Selecting a Data Mode

The asynchronous mode allows the SX/13a to be used with low-speed asynchronous data (data with no accompanying clock). This is accomplished by operating the SX/13a in internal clock mode and at a rate that is 10 times the baud rate of the data. Each data bit is sampled approximately 10 times and appears at the output of the SX/13a channel as the original data bit with a small sampling error due to the asynchronous sampling by the internal clock. Jitter caused by the 10-times over-sampling will be at worst 10 percent of the data bit. The SX/13a data rate in this mode is measured in baud (Bd). In synchronous mode, the unit is hertz (Hz).

For example, if the data rate parameter is set to 9600 baud, the internal clock of the SX/13a will automatically be adjusted to 96,000 Hz.

Errors injected in the asynchronous mode have slightly different characteristics from synchronous errors. Synchronous mode error events are 1 or more bits wide in increments of a bit. Asynchronous errors are 1/10th of a bit wide and occur 10 times more frequently due to the over-sampling. The net result is the correct error rate but with a finer distribution of the error events. When analyzing the SX/13a's error statistics in asynchronous mode, keep in mind that the error counts are counting 1/10th of a bit error events, so there will be 10 times as many of them as expected.

Changing the Data Mode

1. Display the **SETUP RS-422 INTERFACE** screen.
2. Select **<sync>** for synchronous operation; select **<async>** for asynchronous operation.

Selecting a Connector

The East channel is always set to DTE; the West channel can be set to DCE or DTE.

1. Display the **SETUP RS-422 INTERFACE** screen.
2. Move the cursor to the East/West Connector field. The West connector is highlighted.
3. Press one of the following function keys to select an equipment type:

   <DTE> — DTE-to-DTE: In this mode, both the East and West connectors are connected to DTEs.

   <DCE> — DTE-to-DCE: In this mode, the East connector is connected to a DTE and the West connector is connected to a DCE.

Selecting Channel Timing

The channel timing for the RS-449 (RS-422-A) interface depends on the data mode selection (synchronous or asynchronous) and data equipment simulation (DTE-to-DTE or DTE-to-DCE). Channel timing can only be set for synchronous operations. If asynchronous data mode is selected, the channel timing is automatically set to sampling. Once the data mode is set to synchronous, the East/West connectors, channel timing, and loop on or off can be selected.

In synchronous DTE-to-DTE, the internal clock synthesizer, external clock source, or the connected DTE can provide timing. Further, when using the internal clock synthesizer or external clock mode, loop timing can be set to on or off. The loop off setting provides the DTE with transmit and receive clocks. With the loop on setting, the SX/13a (either the internal clock synthesizer or an external clock source connected to the unit) provides the DTE with the receive clocks and the DTEs use the SX/13a clock as a transmit clock source.

In synchronous DTE-to-DCE configuration, timing can be provided from the DCE, or from the DTE and the DCE.

Refer to Table 3.11 for the correlation among hardware configurations, onscreen selections, and the diagrams that illustrate the internal functioning of the received and transmit paths for data and clock for each mode.

Table 3.11 RS-422-A Channel Timing Configuration

Configuration	Selections Onscreen	Description	Figure
Synchronous DTE-to-DTE without loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <off>	The internal frequency synthesizer or external clock source connected to the SX/13a provides the DTE with transmit and receive clocks.	Figure 3.25
Synchronous DTE-to-DTE with loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <on>	The internal frequency synthesizer or external clock source connected to the SX/13a provide the DTE with the receive clock. The SX/13a clock provides the transmit clock source for the DTE.	Figure 3.26
Synchronous DTE-to-DTE with DTE timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: <DTE>	The DTEs provide their own transmit clock timing to the SX/13a.	Figure 3.27
Synchronous DTE-to-DCE with DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DCE> (from DCE)	The DCE provides both transmit and receive clocks for the East and West connectors.	Figure 3.28
Synchronous DTE-to-DCE with DTE & DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DTE> (from DTE & DCE)	The DTE and DCE provide their own transmit clocks.	Figure 3.29

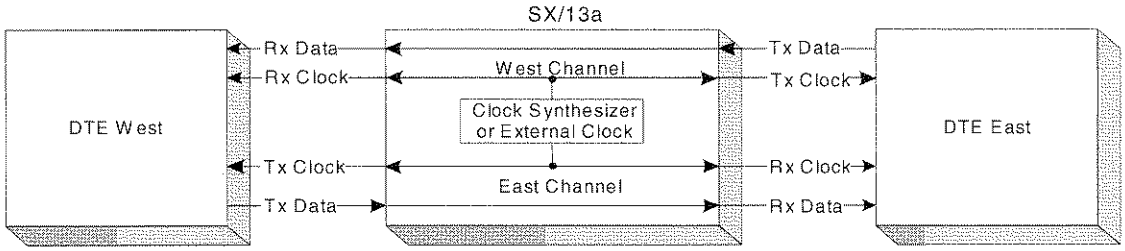

Figure 3.25 RS-422-A DTE-to-DTE Synthesizer or External Clock Mode with Loop Timing Off

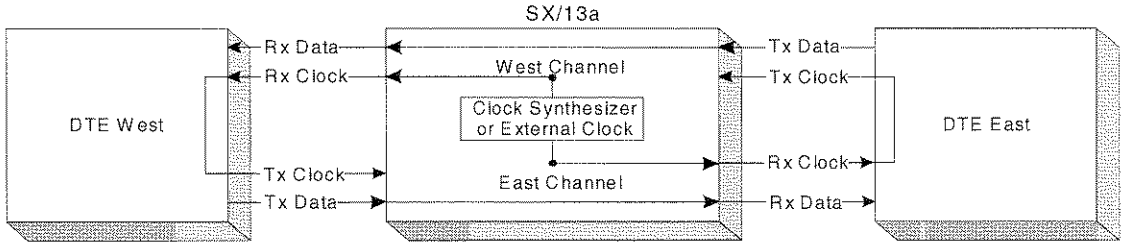

Figure 3.26 RS-422-A DTE-to-DTE Synthesizer or External Clock Mode with Loop Timing On

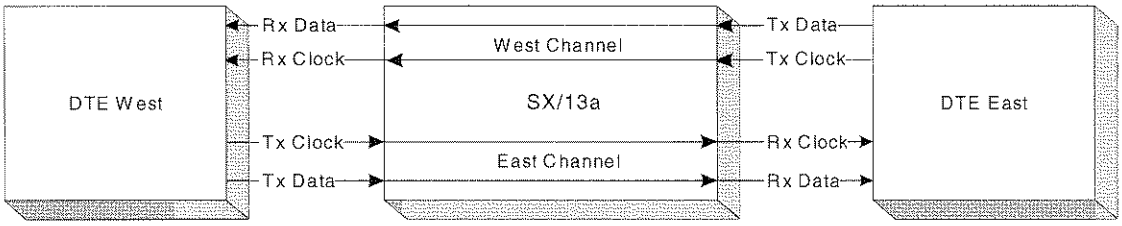

Figure 3.27 RS-422-A DTE-to-DTE Channel Timing from DTEs

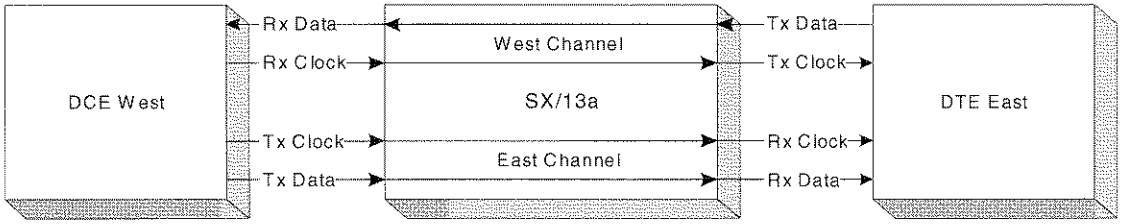

Figure 3.28 RS-422-A DTE-to-DCE Channel Timing from DCE

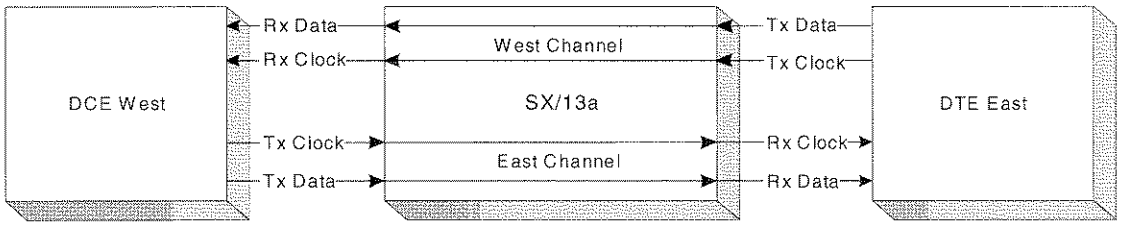

Figure 3.29 RS-422-A DTE-to-DCE Channel Timing from DTE & DCE

Setting the Channel Timing for Synchronous DTE-to-DTE

The channel timing and loop timing options are unique to synchronous DTE-to-DTE.

1. From the **SETUP RS-422 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to **DTE**. The East connector is not selectable. Selecting synchronous DTE-to-DTE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DTE channel timing:

   <synth> (loop timing off) — Synthesizer: The internal frequency synthesizer provides the DTEs with transmit and receive clocks.

   <synth> (loop timing on) — Synthesizer: The internal frequency synthesizer provides the DTEs with receive clocks. The DTEs use the clock from the SX/13a as a transmit clock source.

   <ext> (loop timing off) — External clock: This mode is the same as the Synthesizer (loop timing off) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <ext> (loop timing on) — External clock: This mode is the same as the Synthesizer (loop timing on) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <DTE> — From DTE: The DTEs provide their own transmit clocks to the SX/13a.

Synthesizer or external clock mode enables loop timing. The loop "off" setting provides the DTE with transmit and receive clocks. The loop "on" setting provides the DTE with the receive clocks, and the DTEs use the SX/13a clock as a transmit clock source.

Setting the Channel Timing for Synchronous DTE-to-DCE

The channel timing options are unique to synchronous DTE-to-DCE.

1. From the **SETUP RS-422 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to **DCE**. The East connector is not selectable. Selecting synchronous DTE to DCE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DCE channel timing:

   <DCE> — From DCE: The DCE provides both the transmit and receive clocks for the East and West connectors.

   <DTE> — From DTE & DCE: The DTE and DCE provide their own transmit clocks.

Selecting the Transmit During Delay Change

The SX/13a recalculates and sets the delay buffer each time the delay setting or the data rate is changed. During this time, the SX/13a transmits either all 1s (marks) or all 0s (spaces) in place of the data that normally flows through the SX/13a.

1. Display the **SETUP RS-422 INTERFACE** screen.
2. Move the cursor to the Tx During Delay Change field.

3. Press one of the following function keys to select a transmit during delay change:

   <mark> — 1s are inserted during delay changes.

   <space> — 0s are inserted during delay changes.

Connector Pin Assignments

Table 3.12 through Table 3.14 show the connector pin assignments for the East channel in To DTE channel timing, the West channel in To DTE channel timing, and the West channel in To DCE channel timing. The connectors for the RS-449 (RS-422-A) interface are 37-pin, D-type female connectors.

Table 3.12 RS-449 (RS-422-A) East Connector Pin Assignments in To DTE Channel Timing

Pin	Circuit	Signal	Lead Status
1	Shield	Protective ground	Strapped to interface panel
2	SI	Signalling rate indicator	Output (internally forced on)
4,22	SD (A, B)	Send data	West channel data input
5,23	ST (A, B)	Send timing	Output
6,24	RD (A, B)	Receive data	East channel data output
7,25	RS (A, B)	Request to send	Input
8,26	RT (A, B)	Receive timing	Output
9,27	CS (A, B)	Clear to send	Output
11,29	DM (A, B)	Data mode	Output
12,30	TR (A, B)	Terminal ready	Input
13,31	RR (A, B)	Receiver ready	Output
15	IC	Incoming call	Output (internally forced off)
17,35	TT (A, B)	Terminal timing	Input
18	TM	Test mode	Output (internally forced off)
19	SG	Signal ground	Internally connected to circuit ground
20	RC	Receive common	Internally connected to circuit ground
33	SQ	Signal quality	Output (internally forced on)
36	SB	Standby indicator	Output (internally forced off)
37	SC	Send common	Internally connected to circuit ground

Table 3.13 RS-449 (RS-422-A) West Connector Pin Assignments in To DTE Channel Timing

Pin	Circuit	Signal	Lead Status
1	Shield	Protective ground	Strapped to interface panel
2	SI	Signalling rate indicator	Output (internally forced on)
4,22	SD (A, B)	Send data	East channel data input
5,23	ST (A, B)	Send timing	Output
6,24	RD (A, B)	Receive data	West channel data output
7,25	RS (A, B)	Request to send	Input (internally looped to CS)
8,26	RT (A, B)	Receive timing	Output
9,27	CS (A, B)	Clear to send	Output (internally looped to RS)
11,29	DM (A, B)	Data mode	Output (internally forced on)
12,30	TR (A, B)	Terminal ready	Input
13,31	RR (A, B)	Receiver ready	Output (internally forced on)
15	IC	Incoming call	Output (internally forced off)
17,35	TT (A, B)	Terminal timing	Input
18	TM	Test mode	Output (internally forced off)
19	SG	Signal ground	Internally connected to circuit ground
20	RC	Receive common	Internally connected to circuit ground
33	SQ	Signal quality	Output (internally forced on)
36	SB	Standby indicator	Output (internally forced off)
37	SC	Send common	Internally connected to circuit ground

Table 3.14 RS-449 (RS-422-A) West Connector Pin Assignments in To DCE Channel Timing

Pin	Circuit	Signal	Lead Status
1	Shield	Protective ground	Strapped to interface panel
2	SI	Signalling rate indicator	Open
4,22	SD (A, B)	Send data	West channel data output
5,23	ST (A, B)	Send timing	Input
6,24	RD (A, B)	Receive data	East channel data input
7,25	RS (A, B)	Request to send	Output
8,26	RT (A, B)	Receive timing	Input
9,27	CS (A, B)	Clear to send	Input
10	LL	Local loopback	Output (internally forced off)
11,29	DM (A, B)	Data mode	Input
12,30	TR (A, B)	Terminal ready	Output
13,31	RR (A, B)	Receiver ready	Open
14	RL	Remote Loopback	Output (internally forced off)
15	IC	Incoming call	Open
16	SF/SR	Select frequency/ Signalling rate indicator	Output (internally forced on)
17,35	TT (A, B)	Terminal timing	Output
18	TM	Test mode	Open
19	SG	Signal ground	Internally connected to circuit ground
20	RC	Receive common	Internally connected to circuit ground
28	IS	Terminal in service	Output (internally forced on)
32	SS	Select standby	Output (internally forced off)
33	SQ	Signal quality	Open
34	NS	New signal	Output (internally forced off)
36	SB	Standby indicator	Open
37	SC	Send common	Internally connected to circuit ground

Signalling Leads

In the DTE-to-DTE configuration, the clear to send (CTS) and the request to send (RTS) are connected, and the data mode (DM) and receiver ready (RR) are held on at each connector. In the DTE-to-DCE configuration, when the delay is set to greater than 0, CTS and RTS are connected, and DM and RR are held on for the East connector. In the DTE-to-DCE configuration, when the delay is set to greater than 0, the RTS and terminal ready (TR) are held on for the West connector.

In the DTE-to-DCE configuration, when there is no delay set, the conditions are:

- CTS (East) connected to CTS (West)
- RTS (East) connected to RTS (West)
- DSR (East) connected to DSR (West)
- DTR (East) connected to DTR (West)

RS-232-C Interface

The RS-232-C interface provides signal conversion between the SX/13a's internal TTL format and signals complying with EIA standard RS-232-C. The interface features East and West 25-pin, female D-type connectors for connecting a DTE-to-DTE configuration, and for connecting a DTE-to-DCE configuration. A 25-pin, D-type adapter with male connectors on each end may be required for connecting equipment in a DTE-to-DCE configuration.

The East connector is *always* a DTE connection. The West connector can be either a DTE or DCE connection (see Figure 3.30).

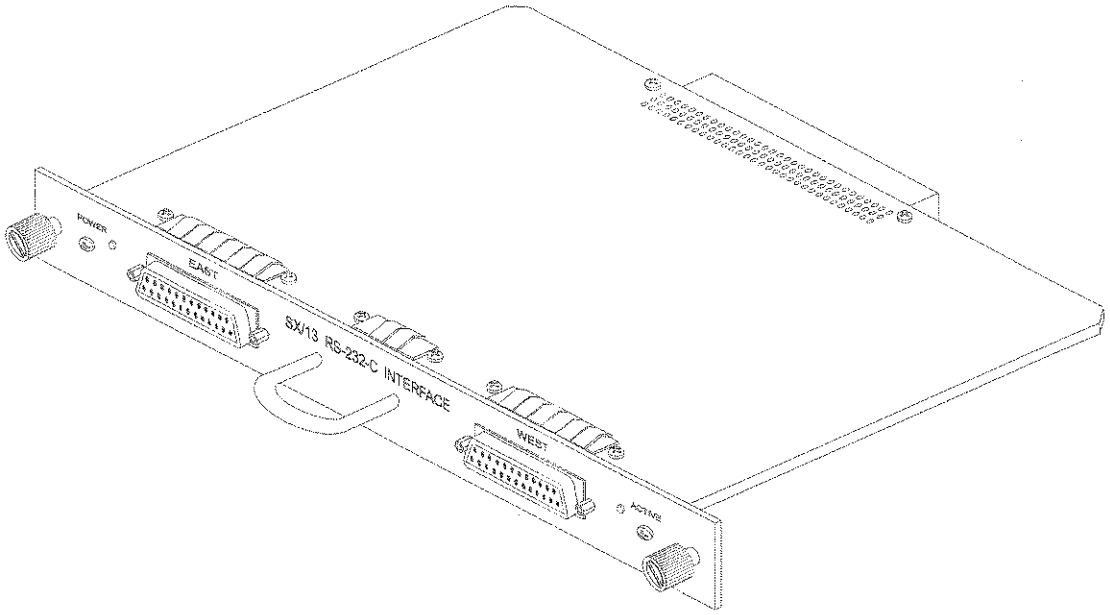

Figure 3.30 RS-232-C Interface

The features and capabilities of the RS-232-C interface are:

- 20 kbps data rate
- Complies with EIA standard RS-232-C
- Two 25-pin female, D-type connectors: East is DTE; West may be either DTE or DCE
- Input impedance: 3,000–7,000 ohms
- Output amplitude: as great as +/– 10 V

Setting Up the RS-232-C Interface

Use the **SETUP RS-232 INTERFACE** screen to select the:

- Data mode
- East/West connector setting
- Channel timing
- Data type to transmit during a delay change
- Loop timing setting

To display the **SETUP RS-232 INTERFACE** screen:

1. Press **MENU**.
2. Select **<setup>**.
3. Press **ENTER** to display the **SELECT INTERFACE** screen.
4. Select **RS-232** and press **ENTER** to display the **SETUP RS-232 INTERFACE** screen (see Figure 3.31).

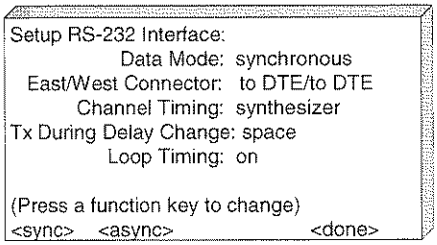

Figure 3.31 Setup RS-232 Interface Screen

Selecting a Data Mode

Asynchronous mode allows the SX/13a to be used with low-speed asynchronous data (data with no accompanying clock). This is accomplished by operating the SX/13a in its internal clock mode and at a rate that is 10 times the baud rate of the data. Each data bit is sampled approximately 10 times and appears at the output of the SX/13a channel as the original data bit with a small sampling error due to the asynchronous sampling by the internal clock. Jitter caused by the 10-times over-sampling will be at worst 10 percent of the data bit. The SX/13a data rate in this mode is measured in baud (Bd). In the synchronous mode, the unit is hertz (Hz).

For example, if the data rate parameter is set to 9600 baud, the internal clock of the SX/13a will automatically be adjusted to 96,000 Hz.

Errors injected in the asynchronous mode have slightly different characteristics from synchronous errors. Synchronous mode error events are 1 or more bits wide in increments of a bit. Asynchronous errors are 1/10th of a bit wide and occur 10 times more frequently due to the over-sampling. The net result is the correct error rate but with a finer distribution of the error events. When analyzing the SX/13a's error statistics in the asynchronous mode, keep in mind that the error counts are counting 1/10th of a bit error events, so there will be 10 times as many of them as expected.

Changing the Data Mode

1. Display the **SETUP RS-232 INTERFACE** screen.
2. Select the **<sync>** function key for synchronous operation; select the **<async>** function key for asynchronous operation.

Selecting a Connector

The East channel is always set to DTE; the West channel can be set to DCE or DTE.

1. Display the **SETUP RS-232 INTERFACE** screen.
2. Move the cursor to the East/West Connector field. The West connector is highlighted.
3. Press one of the following function keys to select an equipment type:

   <DTE> — DTE-to-DTE: In this mode, both the East and West connectors are connected to DTEs.

   <DCE> — DTE-to-DCE: In this mode, the East connector is connected to a DTE and the West connector is connected to a DCE.

Selecting Channel Timing

The channel timing for the RS-232-C interface depends on the data mode selection (synchronous or asynchronous) and data equipment simulation (DTE-to-DTE or DTE-to-DCE). Channel timing can only be set for synchronous operation. If asynchronous data mode is selected, the channel timing is automatically set to sampling. Once the data mode is set to synchronous, the East/West connectors, channel timing, and loop on or off can be selected.

In synchronous DTE-to-DTE, the internal clock synthesizer, external clock source, or the connected DTE can provide timing. Further, when using the internal clock synthesizer or external clock mode, loop timing can be set to on or off. The loop "off" setting provides the DTE with transmit and receive clocks. With the loop "on" setting, the SX/13a (either the internal clock synthesizer or an external clock source connected to the unit) provides the DTE with the receive clocks and the DTEs use the SX/13a clock as a transmit clock source.

In a synchronous DTE-to-DCE configuration, timing can be provided from the DCE, or from the DTE and the DCE.

Refer to Table 3.15 for the correlation among hardware configurations, onscreen selections, and the diagrams that illustrate the internal functioning of the received and transmit paths for data and clock for each mode.

Table 3.15 RS-232-C Channel Timing Configuration

Configuration	Selections Onscreen	Description	Figure
Synchronous DTE-to-DTE without loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <off>	The internal frequency synthesizer or external clock source connected to the SX/13a provides the DTE with transmit and receive clocks.	Figure 3.32
Synchronous DTE-to-DTE with loop timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: Either <synth> or <ext> (Either the internal clock synthesizer or external clock mode) Loop Timing: <on>	The internal frequency synthesizer or external clock source connected to the SX/13a provide the DTE with the receive clock. The SX/13a clock provides the transmit clock source for the DTE.	Figure 3.33
Synchronous DTE-to-DTE with DTE timing	Data Mode: <sync> (synchronous) East/West Connector: <DTE> (to DTE/to DTE) Channel Timing: <DTE>	The DTEs provide their own transmit clock timing to the SX/13a.	Figure 3.34
Synchronous DTE-to-DCE with DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DCE> (from DCE)	The DCE provides both transmit and receive clocks for the East and West connectors.	Figure 3.35
Synchronous DTE-to-DCE with DTE & DCE channel timing	Data Mode: <sync> (synchronous) East/West Connector: <DCE> (to DTE/to DCE) Channel Timing: <DTE> (from DTE & DCE)	The DTE and DCE provide their own transmit clocks.	Figure 3.36

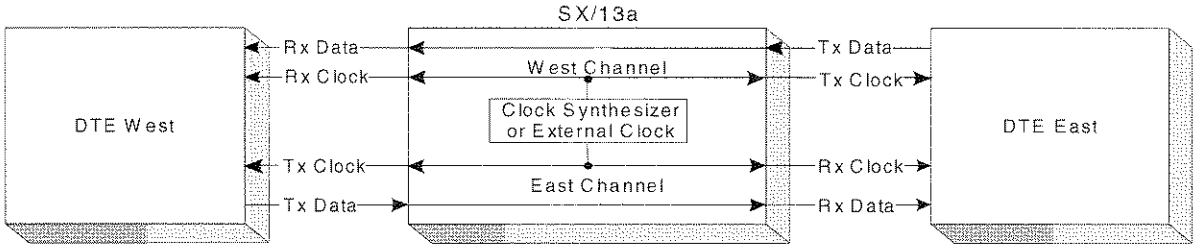

Figure 3.32 RS-232-C DTE-to-DTE Synthesizer or External Clock Mode with Loop Timing Off

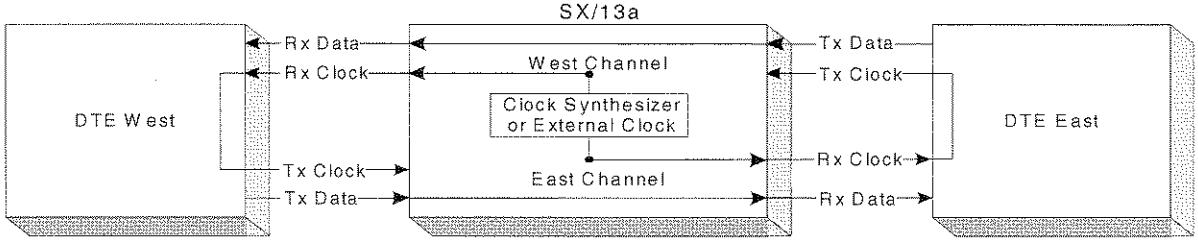

Figure 3.33 RS-232-C DTE-to-DTE Synthesizer External Clock Mode with Loop Timing On

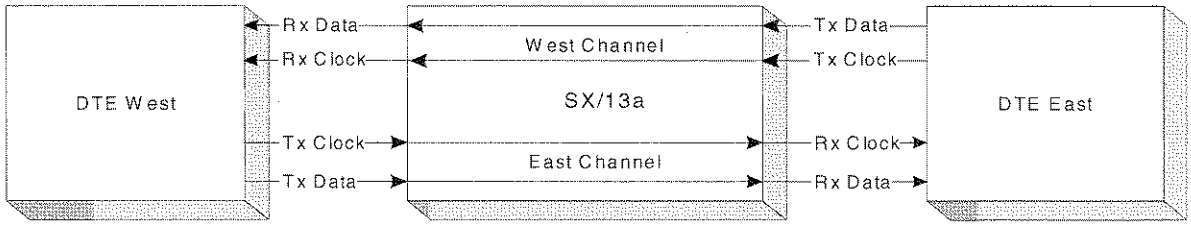

Figure 3.34 RS-232-C DTE-to-DTE Synthesizer or Internal Channel Timing from DTEs

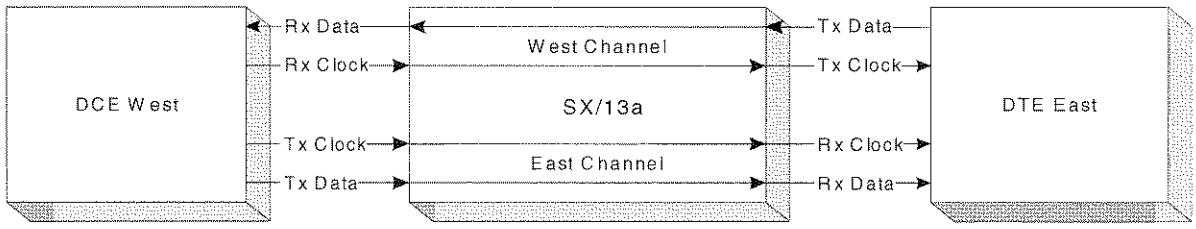

Figure 3.35 RS-232-C DTE-to-DCE Channel Timing from DCE

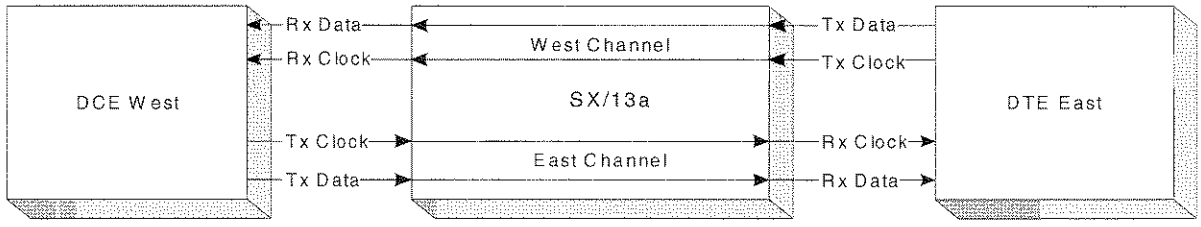

Figure 3.36 RS-232-C DTE-to-DCE Channel Timing from DTE & DCE

Setting the Channel Timing for Synchronous DTE-to-DTE

The channel timing and loop timing options are unique to synchronous DTE-to-DTE.

1. From the **SETUP RS-232 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to **DTE**. The East connector is not selectable. Selecting synchronous DTE-to-DTE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DTE channel timing:

   <synth> (loop timing off) — Synthesizer: The internal frequency synthesizer provides the DTEs with transmit and receive clocks.

   <synth> (loop timing on) — Synthesizer: The internal frequency synthesizer provides the DTEs with receive clocks. The DTEs use the clock from the SX/13a as a transmit clock source.

   <ext> (loop timing off) — External clock: This mode is the same as the Synthesizer (loop timing off) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <ext> (loop timing on) — External clock: This mode is the same as the Synthesizer (loop timing on) mode, except that the SX/13a's timing source is the external clock input, not the frequency synthesizer.

   <DTE> — From DTE: The DTEs provide their own transmit clocks to the SX/13a.

Synthesizer or external clock mode enables loop timing. The loop "off" setting provides the DTE with the transmit and receive clocks. The loop "on" setting provides the DTE with the receive clocks and the DTEs use the SX/13a clock as a transmit clock source. Figure 3.32 through Figure 3.36 illustrate the channel timing modes.

Setting the Channel Timing for Synchronous DTE-to-DCE

The channel timing options are unique to synchronous DTE-to-DCE. Figure 3.35 and Figure 3.36 illustrate the channel timings for DTE-to-DCE.

1. From the **SETUP RS-232 INTERFACE** screen, Data Mode field, select **<sync>** to set the data mode to synchronous.
2. From the East/West Connector field, set the West connector to **DCE**. The East connector is not selectable. Selecting synchronous DTE-to-DCE enables the Channel Timing field.
3. Press one of the following function keys to select a DTE-to-DCE channel timing:

   <DCE> — From DCE: The DCE provides both the transmit and receive clocks for the East and West connectors.

   <DTE> — From DTE & DCE: The DTE and DCE provide their own transmit clocks.

Selecting the Transmit During Delay Change

The SX/13a recalculates and sets the delay buffer each time the delay setting or the data rate is changed. During this time, the SX/13a transmits either all 1s (marks) or all 0s (spaces) in place of the data that normally flow through the SX/13a.

1. Display the **SETUP RS-232 INTERFACE** screen.
2. Move the cursor to the Tx During Delay Change field.

3. Press one of the following function keys to select a transmit during delay change:

   <mark> — 1s are inserted during delay changes.

   <space> — 0s are inserted during delay changes.

Connector Pin Assignments

Table 3.16 through Table 3.18 show the connector pin assignments for the East channel in To DTE channel timing, the West channel in To DTE channel timing, and the West channel in To DCE channel timing. The connector pin assignments are for the 25-pin, D-type female connectors for the RS-232-C interface.

Table 3.16 RS-232 East Connector Pin Assignments in To DTE

Pin	Circuit	Signal	Lead Status
1	AA	Protective ground	Strapped to interface panel
2	BA	Transmitted data	West channel data input
3	BB	Received data	East channel data output
4	CA	Request to send	Input
5	CB	Clear to send	Output
6	CC	Data set ready	Output
7	AB	Signal ground	Internally connected to circuit ground
8	CF	Received line signal detector	Output (internally forced on)
15	DB	Transmit signal element timing (DCE source)	Output
17	DD	Receive signal element timing (DCE source)	Output
20	CD	Data terminal ready	Input
24	DA	Transmit signal element timing (DTE source)	Input

Table 3.17 RS-232 West Connector Pin Assignments in To DTE

Pin	Circuit	Signal	Lead Status
1	AA	Protective ground	Strapped to interface panel
2	BA	Transmitted data	East channel data input
3	BB	Received data	West channel data output
4	CA	Request to send	Input (internally strapped to CTS)
5	CB	Clear to send	Output (internally strapped to RTS)
6	CC	Data set ready	Output (internally forced on)
7	AB	Signal ground	Internally connected to circuit ground
8	CF	Received line signal detector	Output (internally forced on)
15	DB	Transmit signal element timing (DCE source)	Output
17	DD	Receive signal element timing (DCE source)	Output
20	CD	Data terminal ready	Input
24	DA	Transmit signal element timing (DTE source)	Input

Table 3.18 RS-232 West Connector Pin Assignments in To DCE

Pin	Circuit	Signal	Lead Status
1	AA	Protective ground	Strapped to interface panel
2	BA	Transmitted data	West channel data output
3	BB	Received data	East channel data input
4	CA	Request to send	Output
5	CB	Clear to send	Input
6	CC	Data set ready	Input
7	AB	Signal ground	Internally connected to circuit ground
8	CF	Received line signal detector	Input (not connected)
15	DB	Transmit signal element timing source (DCE source)	Input
17	DD	Receive signal element timing (DCE source)	Input
20	CD	Data terminal ready	Output
24	DA	Transmit signal element timing (DTE source)	Output

Signalling Leads

In the DTE-to-DTE configuration for the East/West connector, the clear to send (CTS) and the request to send (RTS) are connected, and the data set ready (DSR) and data carrier detect (DCD) are held on at each connector.

In the DTE-to-DCE configuration, when the delay is greater than "0" for the East connector, the clear to send (CTS) and request to send (RTS) are connected, and data set ready (DSR) and data carrier detect (DCD) are held on. The West connector request to send (RTS) and data terminal ready (DTR) are held on.

In the DTE-to-DCE configuration when delay is equal to "0" for the East/West connector, the following conditions occur:

- CTS (East) connected to CTS (West)
- RTS (East) connected to RTS (West)
- DSR (East) connected to DSR (West)
- DTR (East) connected to DTR (West)

Chapter 4. Operating the SX/13a

Setting the Main Parameters

After turning on the unit, running the initial diagnostics, and configuring the initial setup and interfaces, select settings for the **MAIN PARAMETERS** screen.

To display the **MAIN PARAMETERS** screen:

1. Press **MENU**.
2. Select **<main>** to display the **MAIN PARAMETERS** screen.

The **MAIN PARAMETERS** screen shows the current operating settings. This screen is used to change the settings for delays, random errors, and burst errors. Random errors can be toggled on and off. The **SETUP** screen can be displayed. The delay and error generator settings are not enabled if the data path is set to bypass or outward loopback mode because the generators are bypassed. The data path mode is shown on this screen if any mode other than normal is set. If either error-targeting interface is installed and enabled, the **MAIN PARAMETERS** screen can be used to select targeting settings (e.g., frame type and bits selected for errors). If burst errors are set for either channel, function keys are available for triggering them. Figure 4.1 through Figure 4.3 show the **MAIN PARAMETERS** screens and the menu hierarchy. The clock source displayed in the **CHANGE DATA RATE** screen will vary according to the type of interface used.

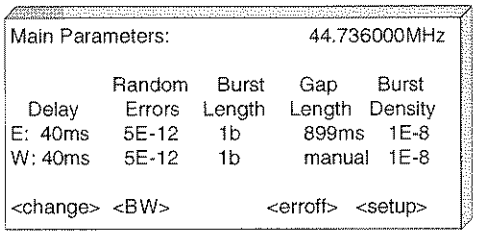

Figure 4.1 Typical Main Parameters Screen

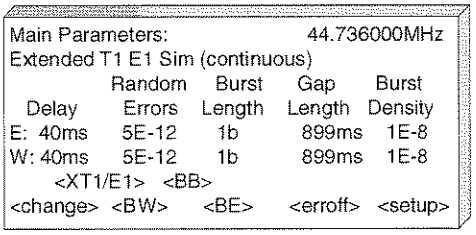

Figure 4.2 Loaded Main Parameters Screen

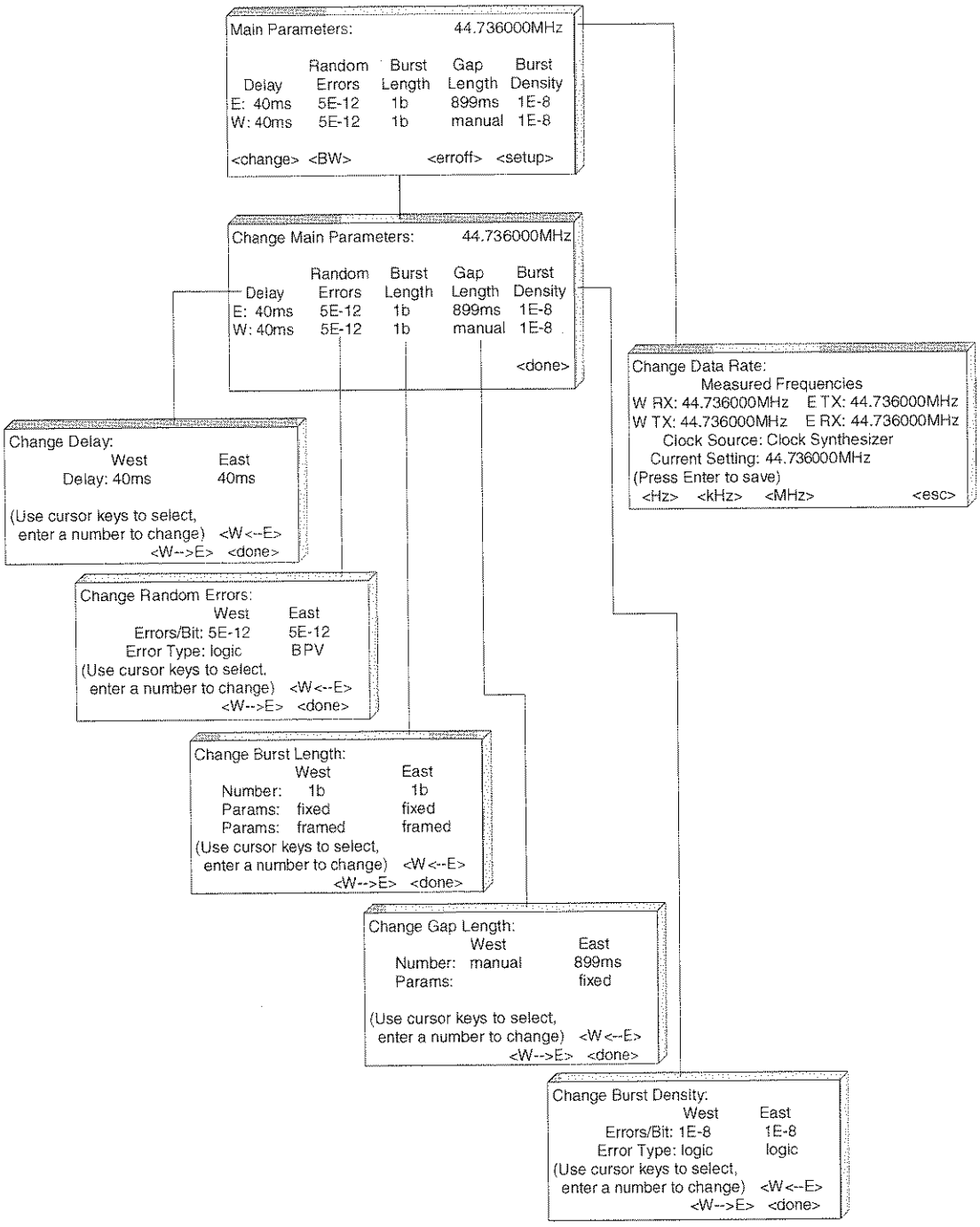

Figure 4.3 Main Parameters Screen Hierarchy

The main operating parameters are:

- The data rate — This is initially set by interface selection to match the default speed of the interface for fixed-frequency interfaces and set to 100 Hz for synchronous interfaces. To display the **CHANGE DATA RATE** screen: **<change>** ▶ Up arrow key ▶ **ENTER** or any number key.

- The delay length for the East and West channels — The delay parameters determine the delay for the East and West directions of the simulated channel. The channel settings are independently selectable, but they are typically set the same for most test applications. The delay range and resolution depend on the data rate, so ensure the data rate setting is correct before setting delays. To display the **CHANGE DELAY** screen: **<change>** (cursor defaults to Delay field) ▶ **ENTER** or any number key.

- The random error rate for the East and West channels — The random error parameters are rate (errors per bit count) and type. The error rate and error type for each channel are independently selectable. To display the **CHANGE RANDOM ERROR** screen: **<change>** ▶ Right arrow key ▶ **ENTER** or any number key.

- The burst error length for the East and West channels — Burst length sets the duration for the burst density. To display the **CHANGE BURST LENGTH** screen: **<change>** ▶ Right arrow key ▶ Right arrow key ▶ **ENTER** or any number key.

- The burst error gap length for the East and West channels — Gap length sets the duration between bursts and the duration that the random error rate is active. To display the **CHANGE GAP LENGTH** screen: **<change>** ▶ Right arrow key ▶ Right arrow key ▶ Right arrow key ▶ **ENTER** or any number key.

- The burst error density for the East and West channels — Burst density sets the rate that burst errors are inserted into a channel during a burst. To display the **CHANGE BURST DENSITY** screen: **<change>** ▶ Right arrow key ▶ Right arrow key ▶ Right arrow key ▶ Right arrow key ▶ **ENTER** or any number key; or **<change>** ▶ Left arrow key ▶ **ENTER** or any number key.

To perform a typical change to a **MAIN PARAMETERS** screen setting:

1. Select **<change>** to display the **CHANGE PARAMETERS** screen. The cursor is initially located on East delay.
2. Position the cursor key in the field to be changed.
3. Press **ENTER** or begin to enter a value using the numeric keypad. The screen to set the parameter is displayed.
4. Set the parameter.
5. Select **<done>** to save the settings and display the **CHANGE PARAMETERS** screen. Select **<esc>** to discard the changes and restore the previous settings. The **CHANGE PARAMETERS** screen is only displayed for 30 seconds. If no activity is detected for 30 seconds, the **MAIN PARAMETERS** screen is automatically displayed.

Setting the Data Rate

Understanding Data Rates

The data rate determines the speed of the simulated channel. The current rate setting is displayed in the upper right-hand corner of the **MAIN PARAMETERS** screen. The SX/13a uses this setting to calculate the length of the first-in, first-out (FIFO) delay buffers for both channels and to set the internal (clock) frequency synthesizer. Table 4.1 shows the default data rates for each SX/13a interface.

Table 4.1 Default Data Rates by Interface

Interface	Default Data Rate
SONET 51.84 Mbps (STS-1) Interface	51.84 MHz
DS3 (T3 44.736 Mbps) Interface	44.736 MHz
DS1 (T1 1.544 Mbps) Interface	1.544 MHz
G.703 (E3 34.368 Mbps) Interface	34.368 MHz
G.703 (E1 2.048 Mbps) Interface	2.048 MHz
HSSI Interface	44.209694 MHz
V.35 Interface	100 Hz
RS-232-C Interface	100 Hz
RS-449 (RS-422-A) Interface	100 Hz

To display the **CHANGE DATA RATE** screen:

1. Display the **MAIN PARAMETERS** screen (**MENU** key ► **<main>** function key).
2. Select **<change>** to display the **CHANGE PARAMETERS** screen.
3. Locate the cursor on the Data Rate field in the upper right-hand corner.
4. Press **ENTER** or begin to enter a value with the numeric keypad. The **CHANGE DATA RATE** screen is displayed and the cursor is at the Current Setting field (see Figure 4.4).

NOTE: The HSSI interface is an exception. The data rate is set from the Setup HSSI interface screen rather than the Main Parameters screen.

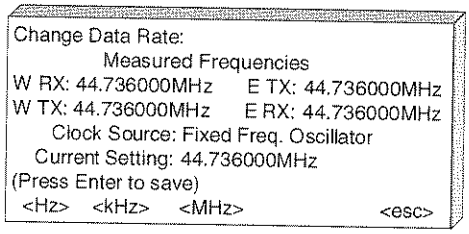

Figure 4.4 Change Data Rate Screen

The **CHANGE DATA RATE** screen shows:

- Measured frequencies — Real-time frequencies for the West receive, West transmit, East transmit, and East receive channels. The measured clock rates can be used to help isolate setup problems and to set the data rate.
- Clock source — Shows the source of the network clock: recover received (loop), internal (fixed frequency oscillator), or external. The clock source is set in the Transmit Timing field via the setup screen for the active interface.
- Current setting — Shows the current data rate.

Changing the Data Rate

The data rate can be changed either by entering a number or by copying a current measured frequency from one of the channels. Perform one of the following:

- Enter the new rate in the Current Setting field. The rate function keys are displayed. Choose one of the following:
  - **<Hz>, <KHz>, <MHz>** — for synchronous applications (SONET (OC-3, STS-3, STS-1), G.703 (E3), G.703 (E1), HSSI, DS1 (T1), DS3 (T3))
  - **<Bd>, <KBd>** — for asynchronous applications (V.35, RS-232-C, RS-422-A)

  NOTE: Since the setting defaults to Hz, be sure to select the proper unit of measurement.

Or:

- Use the function key corresponding to a clock rate measured at one of the four channel connectors, which are:
  - **<W-RX>** — West receive
  - **<W-TX>** — West transmit
  - **<E-RX>** — East receive
  - **<E-TX>** — East transmit

The selected channel rate becomes the current data rate.

NOTE: One or more blinking amber clock LEDs indicates an incorrect data rate. If this occurs, the <change> button on the Main Parameters screen automatically displays the Change Incorrect Data Rate? screen.

The resolution of these measured data rates are:

- 20 Hz for rates below 5 MHz
- 200 Hz for rates of 5 MHz and above

The data rate parameter *must* be set to the rate that flows through the SX/13a. If a discrepancy is detected between the data rate parameter setting and any clock entering or leaving the SX/13a, the appropriate clock LEDs on the unit's front panel will blink.

The data rate depends on the active interface line speed. Table 4.1 shows the data rate for each interface. Note the following:

- Synchronous interfaces, such as V.35 and RS-422-A, normally use the SX/13a's on-board frequency synthesizer to provide clock. The range of this frequency synthesizer is 100 Hz through 52 MHz, with 1 Hz resolution.
- Fixed-frequency interfaces, such as T1, E1, T3, E3, and STS-1, have onboard crystal oscillators to provide network clock. If the data rate of a fixed-frequency interface is set to a rate other than its normal frequency, the SX/13a uses the frequency synthesizer in place of the fixed-frequency oscillator.

Setting Data Rate Examples

Example 1

If the data rate for a T1 interface is set to 1,544,010 Hz, the frequency synthesizer creates this non-standard frequency. If the data rate is set to 1,544,000 Hz, the crystal oscillator on the T1 interface provides this frequency.

Example 2

If a T1 interface is installed and the SX/13a is the source of network clock (i.e., internal clock mode) but nothing is connected to the East receive connector on the T1 interface, the amber LED associated with the East receive blinks.

Setting a Delay

Understanding Delays

All real links add delay to a data stream. This delay is the result of both the propagation time of the physical transmission and the node delays created through cross-connects associated with the routing of the circuit through the switching offices along its path. The total delay time can be significant, even for relatively short links, with delays as high as 70 milliseconds or more for terrestrial links. When satellites are used, the delay can grow considerably longer, adding approximately another 250 milliseconds of delay to transit times in each direction.

The SX/13a can simulate delays from 0 to 324 milliseconds. Delays of up to 9,999 milliseconds are possible at low data rates. Delays of such magnitude are used to simulate the sum of two delay components: the link delay and the delay introduced by a computer system response (which is created in a heavily loaded local area network (LAN), a distributed client/server application, or a remote database system).

The SX/13a uses variable-length, FIFO delay buffers to create the delays. There is one buffer for each channel: East and West. The delay and data rate parameters determine the length of this buffer. When either one of these parameters is changed, the buffer length is recalculated and reset. Channel delays can be entered in microseconds (μs), milliseconds (ms), bytes (B), or words (wd). For finer resolution, the delay can be entered in 8-bit or 16-bit increments, depending on the data rate. Data rates between 100 bps and 8.448 Mbps have 8-bit resolution; rates between 8.448 and 52 Mbps have 16-bit resolution. The delay buffer size for data rates below 8.448 Mbps is 8,388,600 bits. The delay buffer size for data rates between 8.448 Mbps and 52 Mbps is 16,777,200 bits. These can be used to calculate the maximum delay for a data rate.

The input data rate resolution is 8 bits for 8.448 Mbps and below; the input data rate resolution is 16 bits for 8.448 Mbps.

When the delay parameter is set to 0, the data link will still experience a small amount of delay. This inherent delay varies from 16 to 184 bits, depending on interface type, data rate, and data path (the faster the data, the smaller the maximum number of delay bits). The effect of the minimum delay and the delay increment size is apparent only at low data rates (i.e., the minimum delay at a rate of 9,600 Hz is 4 ms with increments of 2.5 ms). The minimum delay and granularity have minimal effect at higher data rates, and the minimum delay changes with different data rates.

Delay settings for the East and West channels are independent. Although the delay would normally be the same for the two channels, there are situations where each channel delay is set to different values.

The delay parameters determine how long it takes data to pass through each channel. For example, if both delay parameters are set to 1,000 ms, the Eastbound data would take 1 second to pass through the East channel, and the Westbound data would take 1 second to pass through the West channel. Table 4.2 shows common data rates and the corresponding maximum delays.

Table 4.2 Common Data Rates and Corresponding Maximum Delays

Data Rate	Relevance	Maximum Delay Rate
100 bps	minimum	9999 ms
1 kbps		9999 ms
64 kbps	(DS0)	9999 ms
100 kbps		9999 ms
1544 kbps	(T1)	5433 ms
2048 kbps	(E1)	4096 ms
6312 kbps	(T2)	2658 ms
8448 kbps	(E2)	1986 ms
34.368 Mbps	(E3)	488 ms
44.736 Mbps	(T3)	375 ms
51.84 Mbps	(STS-1)	324 ms

Changing the Delay Settings

Although the East and West channels can have independent delays, the data rate for both channels must be nominally the same for proper operation. The delay range and resolution depend on the data rate. Ensure the data rate is correct before entering a delay value.

If a delay longer than the maximum delay rate is entered, the following error message is displayed: "Warning! Entry set to upper limit." The unit resets the entered delay to the maximum allowed. If the data rate is changed, then the delay is changed to the new maximum allowed.

If a delay shorter than the minimum rate is entered, the following error message is displayed: "Warning! Entry set to lower limit." In this case, th e unit resets the entered delay to the minimum allowed.

1. Display the **MAIN PARAMETERS** screen.
2. Press **<change>** to display the **CHANGE MAIN PARAMETERS** screen. The cursor defaults to the Delay field.
3. Press any number key on the numeric keypad or press **ENTER** to display the **CHANGE DELAY** screen (see Figure 4.5).

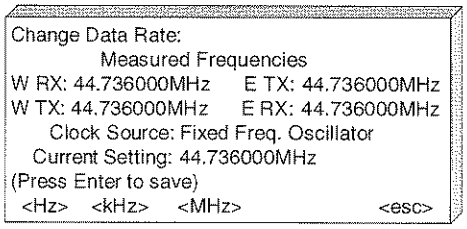

Figure 4.5 Change Delay Screen

4. Enter the delay for both the East and West channel, or enter a delay for one channel and copy the setting to the other channel. Pressing any number key displays the units in which the delay can be measured:

   <µs> — Microseconds

   <ms> — Milliseconds

   <word>/<bytes> — Bytes for data rates below 8.448 MHz, or words for data rates between 8.448 MHz and 52 MHz

5. Press **ENTER** to activate the new delay. The SX/13a reconfigures the delay memory when a delay setting is changed. No data pass through the channel during this time. Instead, the SX/13a transmits either all 1s (marks) or all 0s (spaces). Set the TX During Delay Change setting via the setup screen of the active interface.

Copying a Delay

1. Enter a delay for either the East or West channel.
2. Select **<W→E>** to copy the setting from the West channel to the East channel, or select **<W←E>** to copy from the East channel to the West channel.

The SX/13a automatically sets the delay to the nearest possible delay setting if the delay entered is either out of range or at too fine a resolution.

Creating a Delay without Errors

1. Display the **MAIN PARAMETERS** screen and press the **<erroff.>** function key. Or, turn off random errors by setting the random error rate parameter's mantissa (the decimal part of a logarithm) to 0 for both East and West channels; and turn off burst errors by setting the burst length setting to 0 for both East and West channels.
2. Set the data rate and delay.

The data passing through the SX/13a now will be subject to delay, with no errors added.

Disabling Delays

A delay setting of 0 indicates that the delay generator is turned off. However, data flowing through the SX/13a still experience small propagation delays. On the **MAIN PARAMETERS** screen, the Delay field displays "off" when a delay parameter is set to 0.

Creating Errors

The SX/13a includes an East and a West error generator. These error generators are identical in capability and characteristics. Each channel's error generator includes two types of error generators: the random error generator and the burst error generator. Random errors are a continuous stream of random error events. Burst errors are finite, defined bursts of random errors.

The Extended T1/E1 Simulation Option and SX/13a Error Targeting Option provide additional error targeting capabilities, if installed. These optional modules are discussed in Chapter 6, Using the Error Targeting Options.

The SX/13a front panel includes **EAST ERROR** and **WEST ERROR** LEDs, which flash briefly when either a random or burst error is injected into the channel's data stream. An indicator is steadily lit when an error rate exceeds the rate at which the indictor can flash. This does not necessarily mean that a continuous stream of errors is being injected; rather, it indicates that they are occurring often enough to keep the error indicator on.

The error-generating capabilities of the SX/13a help determine to which error degradations the test system is being subjected.

Understanding Error Distribution Characteristics

The random and burst error generators simulate background data transmission errors caused by Gaussian noise. For this reason, they are referred to as Gaussian. However, due to the discrete (digital) nature of the SX/13a, the distribution is actually Binomial. Binomial distribution simulates, as closely as possible, Gaussian distribution in discrete systems. Binomial distribution plots the actual number of o ccurrences of a particular event; in this case, an error rather than its intensity.

The time intervals between errors are considered Geometric when measured and plotted as a density function. This means that the errors are independent and that each data stream bit flowing through the SX/13a has equal probability of receiving an error. The error probability is the value entered as the random error rate or the burst error density.

Understanding Error Types

There are four error types available for burst errors: logic errors, bipolar violation errors, force-to-mark (1) errors, and force-to-space (0) errors. Only logic and bipolar error types are available for random errors. Not all interfaces support BPV errors. The data link interfaces that support BPV errors are as follows:

- SONET 51.84 Mbps (STS-1)
- DS3 (T3 44.736 Mbps)
- DS1 (T1 1.544 Mbps)
- G.703 (E3 34.368 Mbps)
- G.703 (E1 2.048 Mbps)

Logic Errors

This type of error reverses the logical value of a data bit on the channel. 1s are changed to 0s, and 0s are changed to 1s. The active interface module then converts the resulting data stream back to the appropriate line signals for the type of line being simulated.

Lower levels of line coding, such as the B8ZS code that might be used on a T1 line, are corrected by the interface for the new pattern of 1s and 0s in the data. The SX/13a is unaware of any higher levels of data stream formatting or framing. The injected logic error should be detected by the normal error detection mechanisms of the equipment being tested.

Bipolar Violation Errors

The bipolar violation (BPV) error injects an error at the line coding level of bipolar interfaces, such as DS1, DS3, and STS-1. Bipolar interfaces send data as an alternating series of pulses for each 1 transmitted and no pulse for each 0 sent. When the bipolar pulses fail to alternate, a bipolar violation is created.

In practice, special sequences of BPVs are legal and used to convey certain information. Any other pattern of BPVs is illegal and represents errors on the channel. Such illegal BPV events can be used to test the receiver circuits of equipment operating with these types of data channels. Different types of BPV errors may be selected from the setup screen of the active bipolar interface. The specific types of BPV errors that are available depend on the interface module in use. The BPV Error Mode field on the specific setup screen is not available when the active interface does not support bipolar line encoding.

Force-to-Mark Error

The force-to-mark error injects a forced 1 into the data stream, regardless of whether the data is initially a 1 or a 0. If the bit is already a 1, no error occurs and it remains unchanged. If the bit is a 0, setting the bit to 1 creates an error. Typically, this error type would be used with an error rate of 1. The net result would be a burst of continuous 1s for the entire length of the burst. Forced marks can be used to simulate the complete loss of a channel.

Force-to-Space Error

The force-to-space error injects a forced 0, regardless of whether the data is initially a 1 or a 0. If that bit is already a 0, no error occurs and it remains unchanged. If the bit is a 1, setting the bit to 0 creates an error. Typically, this type of error would be used with an error rate of 1. The net result would be a burst of continuous 0s for the entire length of the burst. Forced spaces can be used to simulate the complete loss of the channel.

Setting Random Errors

Random error rates can be set independently for East and West channels. Random error rates can range from 1×10^{-12} to 1 error per bit. The random error generator is inactive during burst errors and is active during the gaps between these bursts.

When measured and plotted as a density function, the time intervals between errors are Geometric. This means that the errors are independent and that each data stream bit flowing through the SX/13a has equal probability of receiving an error. The error probability is the value entered as the random error rate.

Changing the Random Errors Rate

The random errors parameters determine the rate at which random errors are inserted into the East and West channels. Random errors are active in the gaps between burst errors, if burst errors are also configured.

The error rate for each channel is entered as errors/bit (errors per bit) in exponential form. For instance, 1E-3 errors per bit indicate that one error will occur every 1,000 bits on average. The maximum random error rate is 1 error per bit (i.e., every bit in error), which can be entered in exponential form as 1E-0. The minimum, non-zero random error rate is 1E-12, or a one-bit error every 1,000,000,000,000 bits.

1. Display the **MAIN PARAMETERS** screen.
2. Move the cursor to either the East or West Random Errors field and press a key on the numeric keypad or press **ENTER**. This displays the **CHANGE RANDOM ERRORS** screen (see Figure 4.6).
3. Highlight the mantissa (the decimal part of a logarithm) of the channel.
4. Press a single-digit mantissa (0–9) for the number of errors and press **ENTER**. The cursor advances to the exponent of the error rate.
5. Press a one- or two-digit exponent (1–12) for the number of bits and press **ENTER**. The cursor advances to the Error Type field of the same channel.
6. Choose one of the following error types:

   <logic> — logic errors

   <BPV> — bipolar violation errors

   NOTE: The BPV error type is only available when a bipolar interface is active. If another type of interface is active, these selection keys will not appear, and the error type will default to "logic."

7. After entering a random error rate and error type for one channel, enter the other parameters for the other channel by using the same procedure. Alternatively, copy the error rate and error type using the **<W→E>** (copy West to East) or **<W←E>** (copy East to West) function keys.
8. Select **<done>**. The new settings for random error rate and error type take effect immediately.

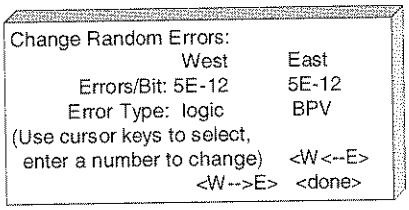

Figure 4.6 Change Random Errors Screen

Setting Burst Errors

Understanding Burst Errors

The burst error generator simulates periodic or sporadic error bursts caused by protection switching or natural events, such as lightning hits, solar flaring, and other physical phenomenon. This generator can insert any one of four error types: logical, BVP, force-to-mark, or force-to-space.

During an error burst, the random error generator is shut off and the burst error generator is used. The three parameters that define burst errors are burst length, gap length, and burst density. The burst length refers to the duration of the error burst. The burst density refers to the error rate that is applied to the channel during the burst length. In other words, the burst density is how many errors are injected during the burst. Gap length refers to the time between burst errors. The burst error generator is turned off and the random error generator is turned back on at the end of the error burst. The random error rate generates errors during the gap length.

Further, the burst length can be fixed or random, framed or unframed, and timed or triggered.

Figure 4.7 shows a sample slice of error stream with both random and burst errors, and burst error parameters. In this example, the burst is "framed" by errors. Framing an error burst ensures that the burst both begins and ends with an error. Framing bursts with errors is optional. Also, a random error occurs during the gap length.

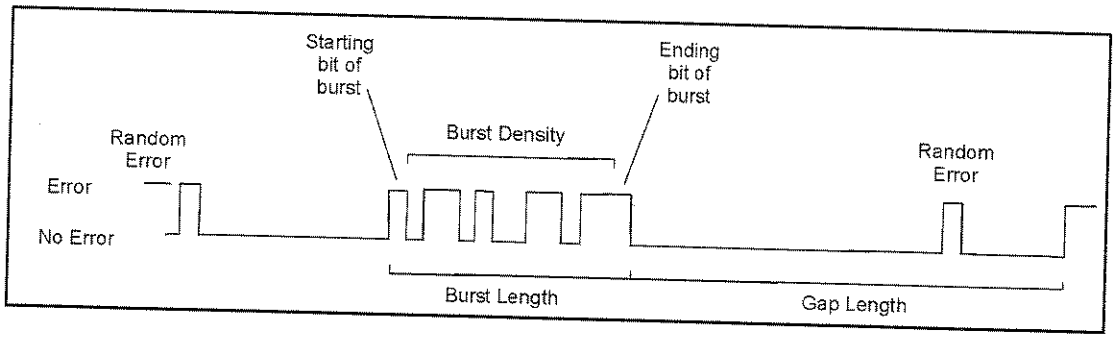

Figure 4.7 Error Stream with Random and Burst Errors

Setting the Burst Error Parameters

Setting Burst Length

The burst length parameter determines how long the burst density error rate is active. The burst length can range from 1 ms to 9,999 ms. The burst length can be set to fixed or random. Burst lengths that are longer than 1 bit can be either fixed at the length entered or they can vary randomly, using the entered length as the mean value. The distribution of random burst lengths approximates the Rayleigh density function. The burst length specifies the mode (i.e., the most frequently occurring burst length), and the mean burst length is approximately 25 percent larger than the value entered. The maximum burst length is four times the value entered.

The burst can also be framed or unframed. A framed burst begins and ends with a forced error, regardless of the burst density. Unframed bursts do not automatically start and end with errors. Instead, the probability of the first and last bits being in error for an unframed burst is the same as the probability of any other bit in the burst being in error.

The burst length can be entered in milliseconds, seconds, bits, kbits (n x 10^3), or Mbits (n x 10^6).

When measured in bits, the burst length can be set in 1-bit steps up to a maximum of 16,777,215 bits at or below 52 MHz.

NOTE: If the burst length is set to 1 bit, the SX/13a treats this as a special case. A 1-bit burst is always an error, regardless of the burst density setting. This special case is intended primarily for single error injection using manually triggered bursts. It permits the injection of single bit errors of any type, either manually or with a fixed- or random-timed gap length.

Changing a Burst Length

1. Display the **MAIN PARAMETERS** screen and press the **<change>** function key.
2. Highlight either channel's Burst Length field and press **ENTER** or a numeric key. This displays the **CHANGE BURST LENGTH** screen.

   The parameters that can be set for both East and West channels are:

   Number: burst length
   Params: fixed or random burst length
   Params: framed or unframed bursts

Entering a Burst Length Number

a) Enter a number for the burst length. This enables the units of measurement function keys.

b) Choose one of the following units of measure for the burst length:

<ms> — milliseconds

<sec> — seconds

<bits> — bits

<kbits> — kilobits

<mbits> — megabits

c) Press **ENTER**.

Selecting Fixed or Random Burst Lengths

Choose one of the following burst lengths:

<fixed> — The entered burst length number is used as the burst length

<random> — Enables the burst length to vary randomly with a mean value of the entered length. The distribution of random burst lengths approximates the Rayleigh distribution.

Selecting Framed or Unframed Bursts

Choose one of the following:

<framed> — Forces the first and last bit of the burst to be in error.

<unfrmd> — Does not force the first and last bit of the burst to be in error. The first and last bits are just as likely as any other bit to be erred. These bits may not be in error, although they are technically part of the burst error.

Copying a Burst Length Setting

The burst length settings can be independently set for the East and West channels. The settings can be manually entered for both channels, or the settings may be manually entered for one channel and copied to the other channel.

1. Select **<W→E>** to copy the West channel burst length settings to the East channel.
2. Select **<W←E>** to copy the East channel burst length settings to the West channel.

Setting a Gap Length

The gap length sets the amount of time between bursts. This length is also the time period during which the random error rate is active. This number can range from 1 to 99,999,999 m illiseconds. The burst length can either be a fixed length, vary about the mean randomly, or be controlled manually.

If randomly controlled, the SX/13a generates random gap lengths using a Bernoulli process, which produces a Geometric distribution with the gap length as the mean. If manually controlled, a key press triggers the burst.

Manual gap lengths are used for manual burst injection. When one of the burst inject function keys is pressed, a single burst is generated either on the West channel, both channels or on the East channel. The burst generator then waits for the next key press. The burst inject keys are:

<BW> — Burst West channel

<BB> — Burst both channels

<BE> — Burst East channel

Setting a Random or Fixed Gap Length

1. From the **CHANGE MAIN PARAMETERS** screen, highlight a gap length and press a numeric key or press **ENTER** to display the **CHANGE GAP LENGTH** screen (see Figure 4.8).
2. Enter a length and select **<ms>** (milliseconds) or **<sec>** (seconds).
3. Select either fixed gap length **<fixed>** to always generate the same length gap, or select random gap length **<random>** to generate random, varying gap lengths based on the length entered.

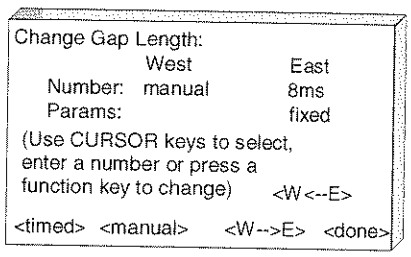

Figure 4.8 Change Gap Length Screen

Setting a Manual Gap Length for Triggered Bursts

1. From the CHANGE GAP LENGTH screen, select **<manual>**. If manual is selected, there is no second parameter choice available between fixed and random. The corresponding burst trigger function keys are enabled on the MAIN PARAMETERS screen and the ERROR STATISTICS screen.
2. If random was previously selected as the other parameter, reset it to fixed using the **<fixed>** function key.
3. Once a gap length is set to manual, the previously entered numeric gap is restored by selecting **<timed>**, and the gap can be set to fixed or random.

Copying a Gap Length

1. Enter the gap length parameters for one channel, East or West.
2. Select **<W→E>** (copy West to East) or **<W←E>** (copy East to West).

Setting the Burst Density Parameters

Setting Burst Density

When measured and plotted as a density function, the time intervals between errors are Geometric. This means that the errors are independent and that each data stream bit flowing through the SX/13a has equal probability of receiving an error. The error probability is the value entered as the burst error density.

The burst error density determines the error rate for the length of the burst. Burst error rates can range from 1×10^{-8} to 1 error per bit.

Burst density determines the rate that errors are inserted into a channel during an error burst. Enter errors as errors per bit in exponential form. For example, 1E-3 errors per bit means one error every 1,000 bits on average. Burst density parameters are entered independently for East and West channels.

The four possible burst density errors are: logic, BPV, force-to-mark, and force-to-space.

Changing a Burst Density

1. From the CHANGE MAIN PARAMETERS screen, highlight the Burst Density field and press a numeric key or **ENTER**. The CHANGE BURST DENSITY screen is displayed.
2. Select a single digit mantissa (0–9).
3. Select a single digit exponent (1–8).
4. Choose one of the following error types:

   <logic> — Logic: Reverses the logical value of a data bit on the channel

   <BPV> — Bipolar Violation: Injects an error at the line coding level of bipolar interfaces

   <space> — Force-to-Space Error: Injects a forced space (0) into the data stream

   <mark> — Force-to-Mark Error: Injects a forced mark (1) into the data stream

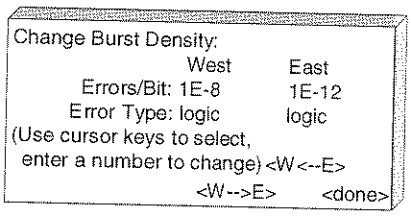

Figure 4.9 Change Burst Density Screen

Copying a Burst Density

1. Enter the burst density parameters for one channel, East or West.
2. Select **<W→E>** (copy West to East) or **<W←E>** (copy East to West).

Triggering Burst Errors Manually

Gap length must be set to manual for the burst error function keys to be enabled on the **MAIN PARAMETERS** screen and the **ERROR STATISTICS** screen.

The burst error triggers are:

<BW> — Burst West: This key triggers a burst on the West channel. It is displayed when the West gap length is set to manual and the burst length is not zero. If triggering a burst causes errors, the red error LEDs flash for each error injected.

<BE> — Burst East: This key triggers a burst on the East channel. It is displayed when the East gap length is set to manual and the burst length is not zero. If triggering a burst causes errors, the red error LEDs flash for each error injected.

<BB> — Burst Both: This key simultaneously triggers a burst on both the East and West channels. It is displayed when both the East and West gap lengths are set to manual and both burst lengths are not zero. If triggering a burst causes errors, the red error LEDs flash for each error injected.

Disabling Burst Errors

To turn off the burst error generator, it is recommended to set the burst length to zero. Another method to shut off burst errors is to set the gap length to manual.

Disabling All Errors

To turn off both the random and burst error generators, select the **<erroff>** function key on the **MAIN PARAMETERS** screen. This disables all errors on East and West channels and displays the **<erron>** function key. To resume error generation, select **<erron>**.

NOTE: The <erroff> function is useful for allowing data to flow through uncorrupted when setting up a new link and for checking system operation without errors.

Simulating Errors without Channel Delays

1. Set the delay parameters for the East and West channels to 0.
2. Set the data rate to the operating data rate.
3. Set the random error rate and burst error parameters to thedesired settings for each channel. No added delays are added to the data passing through the SX/13a.

Using Error Statistics

Three error statistics screens track error events and display statistics. Error measurements are shown separately for each channel direction. In addition to these statistics, the interfaces capable of injecting BPV errors, such as the DS1, DS3, STS-1, can detect and count bipolar violations on their inputs. This statistic is automatically displayed when a bipolar interface is active. In addition to counting error events, an elapsed time is displayed, indicating the period over which the counts have been made. This timer's resolution is 1/10 of a second and can run up to 744 hours. Error counts can accumulate up to 2^{48} (approximately 2.8 x 10^{14}). After a count reaches 99,999,999, it is displayed in scientific notation. The error statistics screens do not have to be displayed for the statistics to accumulate.

Stopping and Starting the Error Statistics Count

While the error statistics function is running, a **<stop>** function key appears on the error statistics screen. Select **<stop>** to stop accumulating error statistics. Regardless of the screen that is currently displayed, the error statistics will continue to accumulate until the **<stop>** key is pressed. Statistics are not cleared until **<clear>** is selected, or the power is turned off.

To begin the error statistics function again, select **<start>**.

Clearing the Error Statistics Count

To clear the accumulated error statistics, select **<clear>**.

Displaying Error Statistics

To access the ERROR STATISTICS screens:

1. Press **MENU**.
2. Select **<stats>**. The ERROR STATISTICS screen is displayed.
3. To display other error statistics screens, select **<next>** and **<previous>** to toggle between ERROR STATISTICS **1**, ERROR STATISTICS **2**, and ERROR STATISTICS **3**. The statistics for each screen are listed in Table 4.3.

   If manual bursts are enabled, errors can be injected from these screens.

Table 4.3 Error Statistics

Statistic	Description	Screen Name
Error Count	The total number of errors generated for that channel since the statistics accumulator was started.	ERROR STATISTICS 1
Error Seconds	The total number of seconds containing one or more errors on that channel since the statistics accumulator was started.	ERROR STATISTICS 1
Burst Error Seconds	The number of seconds with at least 100 errors on that channel since the statistics accumulator was started.	ERROR STATISTICS 1
Severely Errored Seconds	The total number of seconds when the error rate exceeded 1E-3 on that channel since the accumulator was started.	ERROR STATISTICS 1
Burst Count	The total number of error bursts on that channel since the accumulator was started.	ERROR STATISTICS 2
Burst Length Minimum	The length of the shortest burst on that channel since the accumulator was started.	ERROR STATISTICS 2
Burst Length Maximum	The length of the longest burst on that channel since the accumulator was started.	ERROR STATISTICS 2
Current BER	The bit error rate for the previous three seconds on that channel since the accumulator was started.	ERROR STATISTICS 3
Average BER	The bit error rate since on that channel since the accumulator was started.	ERROR STATISTICS 3
Received BPV Error Count	The total number of bipolar violations on the receive channel since the accumulator was started. This statistic is only displayed if the current interface supports BPV errors (T1, E1, STS -1, and so on).	ERROR STATISTICS 3

Chapter 5. Creating Programs for the SX/13a

Understanding Programs

The data rate, delays, and error settings create one fixed set of East and West channel characteristics. Programs extend the SX/13a's functionality by allowing these characteristics to change over time. Instead of one fixed set of characteristics, programs can be used to create several sets of characteristics. This can help better simulate a complex error sequence involving several sets of error and delay events. The SX/13a's programming feature is useful for setting up a series of similar tests. For example, a series of automated tests could be set up for a manufacturing test suite. In this case, each step's duration is set to manual, and each step tests a specific part of the implementation under test. The user starts the program and cycles through steps manually to verify that the implementation under test passes each step.

The SX/13a's programs use the same delay and error settings as the **MAIN PARAMETERS** screen, but each program consists of steps. In essence, every step is like another configurable **MAIN PARAMETERS** screen. The duration of each step is set in seconds. The range of each step's duration is from 1 to 999,999 seconds, and each program can contain up to 99 steps . Alternatively, the progression from step to step can be controlled manually rather than timed. After the last step, the program can repeat from the beginning or stop and restore the main parameters.

The SX/13a can save one program at a time in memory when the unit is turned off, and restore it when the unit is turned on. Both remote control options — the RS-232-C Remote Control Option and the IEEE-488 Remote Control Option — can be used to create multiple programs which can be downloaded to the SX/13a.

Weather conditions, such as rainstorms, lightning, and solar flare-ups, create error conditions that vary over time. An example of this is the affect a rainstorm has on a microwave link. As the storm approaches the path of the link, the burst and random errors increase. Then, as the storm moves past the path, the error profile slowly returns to normal. Many other physical phenomena cause a known sequence of channel conditions. Programs can be created to simulate local natural phenomena.

Creating a Program

Most of the procedures involved in creating a program are the same type of configuration of delays, errors, data rates, and related settings for the **MAIN PARAMETERS** screen. Setup of the **MAIN PARAMETERS** screen is described in Chapter 4, Operating the SX/13a. Setup for the specific interfaces is described in Chapter 3, Setting Up the SX/13a Interfaces. Creating, downloading, and uploading programs remotely is described in Chapter 7, Remotely Operating the SX/13a.

Using the Program Screen

Figure 5.1 shows the **PROGRAM** screen. This screen shows the settings for the current step. The upper right corner displays the data rate set for the program step. It does not necessarily show the current data rate. The data rates can be set to be different from one step to the next; however, it is usually not desirable because changing the data rate (or the delay setting) from step to step causes a discontinuity in the data stream while a new delay buffer length is calculated and set. A set of function keys is displayed at the bottom of the **PROGRAM** screen. Different functions keys are displayed for the **PROGRAM RUN** and **PROGRAM END** screens.

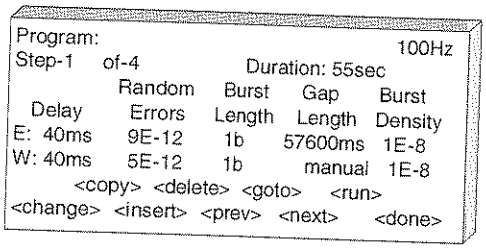

Figure 5.1 Program Screen

Basic Steps for Creating and Running Programs

1. Press MENU.
2. Select **<prog>** to display the PROGRAM screen.

   The PROGRAM screen is similar to the MAIN PARAMETERS screen in that in includes the data rate, delay, random and burst error settings. It is different in that it also includes the current step number, the total number of steps, the duration of the current step, and additional function keys.

   Step–n of nn — Displays the current step and the total number of steps: n is the current step and nn is the total number of steps. The maximum number of steps is 99.

   Duration — Displays the length of the current step in seconds. The maximum length for a step is 999,999 seconds.

   Delay, **Random Errors**, **Burst Length**, **Gap Length**, and **Burst Density** for both East and West channels — The setup is the same as for the MAIN PARAMETERS screen.
3. Select **<change>** to set the parameters for a step.
4. Create a set of parameters for each step.
5. Run the program.
6. Optionally, statistics for the program can be displayed.
7. Optionally, save the program. If a remote option is in use, the program can be saved remotely.

Changing a Step

1. From the PROGRAM screen, select **<change>**. The CHANGE PROGRAM PARAMETERS screen is displayed.
2. To change the desired parameters, perform one of the following:

   a) Select the appropriate function key for the desired parameter to be changed and enter the new parameter.

   Or:

   b) To change the step duration, press **ENTER** to display the STEP DURATION screen. Note that pressing a number key instead of **ENTER** displays the CHANGE STEP DURATION screen, which does not include the **<manual>** and **<timed>** function keys.

   Enter a number to set the duration in seconds, or select **<manual>** to make the step manually triggered. When the program is run, a manual step does not start until the user selects **<cont>** to start the step. To change a manual step back to a fixed duration, select **<timed>** at the STEP DURATION screen.
3. Select **<done>** to display the PROGRAM screen.

Inserting a Step

A new step can be inserted from the **PROGRAM** screen or **PROGRAM END** screen. Use the **<insert>** function key to insert a new step before the current step. The new step's parameters will be identical to those of the current step, unless there are no steps defined (the **PROGRAM END** screen will be displayed). In this case, the settings from the **MAIN PARAMETERS** screen are used.

To change the parameters of a displayed step, select **<change>**. To return to the **PROGRAM** screen at any time, select **<done>**.

Copying a Step

The parameters for a step can be copied into the current step from any step, from the previous step, or from the **MAIN PARAMETERS** screen. Copying is useful when the new step varies slightly from an already defined step.

1. From the **PROGRAM** screen, display the step that will be copied over.

   Remember that a new step can be inserted before the current step, and that the inserted step has the same parameters as the step it was inserted before. For more information, see "."

2. Select **<copy>**. The **COPY STEP** screen is displayed.
3. Perform one of the following copying methods:

   a) To copy the settings from a specific step: For the Source field, enter the number of the step to be copied to the current step. The Destination field displays "current step" and cannot be changed.

   Or:

   b) To copy the settings from the previous step: Select **<prev>** and then **<insert>**. The settings from the previous step are copied to the current step.

   Or:

   c) To copy the settings from the **MAIN PARAMETERS** screen: Select **<main>**. The main parameters settings are copied to the current step.

To change the parameters of a displayed step, select **<change>**. To return to the **PROGRAM** screen at any time, select **<done>**.

Starting, Stopping and Completing a Program

The displayed parameters for the current step do not affect the channel until the program is run. If the program memory is empty (no steps are defined), the **PROGRAM END** screen is displayed. Once a step or steps are defined for the program, it can be run. After a program has been started, statistics can be compiled and displayed for that program.

Starting a Program

- Select **<run>** to start the program from the current step.

  The **PROGRAM RUN** screen is displayed. The screen name — **PROGRAM RUN** — blinks while the program runs. The current step is displayed and the duration decrements.

The program runs until it is stopped or until it completes the last step. If the program is set to repeat, then all steps of the program are repeated indefinitely.

Stopping a Program

Select **<stop>** to stop a program.

Completing a Program

The **PROGRAM END** screen is displayed when the last step of a program is completed, or if no steps are defined for a program. In addition, steps can be inserted from the **PROGRAM END** screen.

1. When the program is completed, select **<done>** to return to the **PROGRAM** screen.
2. Select **<next>** to display the **PROGRAM END** screen and exit the program mode.

Repeating a Program

A program can be set to repeat continuously from the first step, or stop when it completes the last step. The settings from the **MAIN PARAMETERS** screen are restored as the current channel parameters when a program stops.

1. Use <goto> <end> to display the Program End screen, or press <next> until the Program End screen is displayed.
2. Select an option:

   <rpt on> — Repeat On

   <rptoff> — Repeat Off

The **PROGRAM END** screen is displayed when the last step of a program is completed, or if no steps are defined for a program. In addition, steps can be inserted from the **PROGRAM END** screen.

Displaying Program Statistics

A program usually must be started before the statistics counts can be begun. Statistics are not automatically started when a program is started. Statistics for a program are counted and displayed when **<start>** is pressed from any of the error statistics screens. The statistics operation and functionality is similar to displaying and running statistics from the **MAIN** screen, except that **<done>** displays the current program step.

1. Run the program.
2. Select **<stats>**. The **ERROR STATISTICS 1** screen is displayed.
3. Select **<start>**. The error counts are started and displayed.
4. Select **<done>** to display the **PROGRAM RUN** screen.

   Statistics are still counted after selecting **<done>**. It is possible to toggle between the **PROGRAM RUN** screen and the error statistics screens. Both statistics accumulation and the program can be stopped and started without resetting the counts. In both cases, when restarted the statistics continue to accumulate where the count left off. The counts must be cleared by using the **<clear>** function key to restart the statistics counters.
5. To clear the statistics counters, select **<clear>**.

Program Examples

Example 1 — Ship-to-Ship Link

The data channel is a radio frequency telemetry link between a mother and a daughter ship. Special forward error corrector (FEC) hardware and automatic request (ARQ) software was developed to transfer the data between the two ships reliably under severe ocean conditions. The new hardware and software needs to be bench-tested. The channel conditions to be simulated are:

Data rate: 6.312 Mbps
Delay: 100 bytes due to the transmission equipment
Gaussian error rate: $1x10^{-4}$ errors/bit
Short fade: errors increase to 0.5 errors/bit for an average length of 200 milliseconds once every second
Long fade: errors increase to 0.5 errors/bit for an average length of 10 seconds once every minute

These channel conditions can be simulated with a two-step program.

1. Set the main parameters to be used as defaults for the new program steps. The main parameters settings are:

   Data Rate = 6.312 MHz
   Delay = 100 bytes
   East/West Random Error Rate = 0
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

2. Enter the program mode and erase the program memory with the **<delete>** function. Select **<insert>** to insert the first step. The main parameters are copied to Step 1.

3. Then select **<change>** to set the parameters for the first step as follows:

   Step 1 Settings

   Data Rate = 6.312 MHz
   Step Duration = 50 seconds
   Delay = 100 bytes
   East/West Random Error Rate = $1x10^{-4}$
   East/West Burst Length = 200 milliseconds, random
   East/West Gap Length = 800 milliseconds, fixed
   East/West Burst Density = $5x10^{-1}$

4. After entering the Step 1 parameters, select **<done>** to return to the **PROGRAM** screen, **<next>** to move forward past Step 1 to the **PROGRAM END** screen, and then **<insert>** to insert a second step. The inserted step is the same as Step 1.

5. Step 2 will generate the elevated error rate for 10 seconds. Select **<change>**. The parameters for the second step are:

   Step 2 Settings

   Data Rate = 6.312 MHz
   Step Duration = 10 seconds
   Delay = 100 bytes
   East/West Random Error Rate = $5x10^{-1}$
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

6. Select **<done>** to return to the **PROGRAM** screen.
7. Select **<next>** to display the **PROGRAM END** screen.
8. Select **<rpt on>** to enable the program repeat function.
9. Select **<goto>**.
10. Select **<begin>**.
11. Select **<run>** to start the program.
12. When you are finished with the test, select **<stop>** to end the program.

The main parameters will determine the delay and error settings.

Example 2 — Backup Satellite Link

A terrestrial T1 data link has a backup satellite link. The test scenario simulates the resynchronizing ability of the T1 multiplexers when the link is switched. The example two-step program switches between the terrestrial and satellite data link simulation every 10 minutes.

The terrestrial link conditions are:

Data Rate: 1.544 Mbps
Delay: 2 milliseconds
Gaussian error rate: 1×10^{-7} errors/bit
Burst error characteristics: 10 bits average length, occurring at an average rate of once per second

The satellite link conditions are:

Data Rate: 1.544 Mbps
Delay: 240 milliseconds
Gaussian error rate: 5×10^{-8} errors/bit

1. From the **PROGRAM** screen, delete all the steps.
2. Select **<insert>** to insert the first step. The main parameters are copied to Step 1.
3. Select **<change>** to set the parameters for the first step as follows:

   Step 1 Settings

   Data Rate = 1.544 MHz
   Step Duration = 600 seconds (wait 10 minutes)
   Delay = 2 milliseconds
   East/West Random Error Rate = 1×10^{-7}
   East/West Burst Length = 10 bits, random
   East/West Gap Length = 1000 milliseconds, random
   East/West Burst Density = 5×10^{-1}
4. Select **<done>**.

5. Select **<insert>**, **<next>**, **<change>**, and change the settings for Step 2 as follows:

   Step 2 Settings

   Data Rate = 1.544 MHz
   Step Duration = 600 seconds (wait 10 minutes)
   Delay = 240 milliseconds
   East/West Random Error Rate = 5×10^{-8}
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

6. Select **<done>**.

7. Select **<goto>**, **<end>**, and **<rpt on>** to enable the program to run continuously.

8. When you are finished with the test, select **<stop>** to end the program.

Example 3 — Testing a T3 Multiplexer

The quality control department of a T3 multiplexer manufacturer needs to test its multiplexers under various error conditions. The SX/13a is used to simulate the T3 data channel. Example 3 simulates various error conditions. The manual step trigger option is used between certain steps in the program. The tester triggers manual steps with the **<continue>** function key.

1. Set the main parameters to be used as defaults for the new program steps.

   Main Parameters

   Data Rate = 44.736 MHz
   Delay = 40 milliseconds
   East/West Random Error Rate = 0
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

2. From the **PROGRAM** screen, delete all the steps.

3. Select **<insert>** to insert Step 1, which will set Gaussian errors at $1x10^{-8}$ errors per bit.

4. Select **<change>**, and set the parameters for Step 1 to the following:

   Step 1 — Gaussian errors at 1x10-8 errors/bit

   Data Rate = 44.736 MHz
   Step Duration = Manual
   Delay = 40 milliseconds
   East/West Random Error Rate = 1×10^{-8}
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

5. Select **<insert>** to insert Step 2, which will set Gaussian errors at $5x10^{-6}$ errors per bit.

6. Select **<change>**, and set the parameters for Step 2 to the following:

   Step 2 — Gaussian errors at 5x10-6 errors/bit

   Data Rate = 44.736 MHz
   Step Duration = Manual
   Delay = 40 miliseconds
   East/West Random Error Rate = 5×10^{-6}
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

7. Select **<insert>** to insert Step 3, which will set Gaussian errors at $2x10^{-5}$ errors per bit.

8. Select **<change>**, and set the parameters for Step 3 to the following:

   Step 3 — Gaussian errors at 2x10-5 errors/bit

   Data Rate = 44.736 MHz
   Step Duration = Manual
   Delay = 40 milliseconds
   East/West Random Error Rate = 2×10^{-5}
   East/West Burst Length = 0
   East/West Gap Length = Manual
   East/West Burst Density = 0

9. Select **<insert>** to insert Step 4, which will set 10 milliseconds average error bursts at $2x10^{-6}$ errors per bit, and 200 milliseconds average gaps with Gaussian errors at $2x10^{-9}$ errors per bit.

10. Select **<change>**, and set the parameters for Step 4 to the following:

    Step 4 — 10 ms average error bursts at 2x10-6 errors/bit, 200 ms average gaps with Gaussian errors at 2x10-9 errors/bit

    Data Rate = 44.736 MHz
    Step Duration = Manual
    Delay = 40 milliseconds
    East/West Random Error Rate = 2×10^{-9}
    East/West Burst Length = 10 ms, Random
    East/West Gap Length = 200 ms, Random
    East/West Burst Density = 2×10^{-6}

11. Select **<insert>** to insert Step 5, which will change the error simulation, starting at $5x10^{-8}$ for 10 seconds.

12. Select **<change>**, and set the parameters for Step 5 to the following:

    Step 5 — Changing error simulation, the error rate starts at 5x10-8 for 10 seconds

    Data Rate = 44.736 MHz
    Step Duration = 10 seconds
    Delay = 40 milliseconds
    East/West Random Error Rate = 5×10^{-8}
    East/West Burst Length = 0
    East/West Gap Length = Manual
    East/West Burst Density = 0

13. Select **<insert>** to insert Step 6, which will increase the error rate to $2x10^{-6}$ errors per bit for 20 seconds.

14. Select **<change>**, and set the parameters for Step 6 to the following:

    Step 6 — Error rate increases to $3x10^{-6}$ for 20 seconds

    Data Rate = 44.736 MHz
    Step Duration = 20 seconds
    Delay = 40 milliseconds
    East/West Random Error Rate = 3×10^{-6}
    East/West Burst Length = 0
    East/West Gap Length = Manual
    East/West Burst Density = 0

15. Select **<insert>** to insert Step 7, which will decrease the error rate for 30 seconds, the program ends, and no errors are returned.

16. Select **<change>**, and set the parameters for Step 7 to the following:

    Step 7 — Error rate falls for 30 seconds then program ends and returns to no errors

    Data Rate = 44.736 MHz
    Step Duration = 30 seconds
    Delay = 40 milliseconds
    East/West Random Error Rate = 1×10^{-9}
    East/West Burst Length = 0
    East/West Gap Length = Manual
    East/West Burst Density = 0

17. When you are finished with the test, select **<stop>** to end the program.

Chapter 6. Using the Error Targeting Options

There are two options that extend the error targeting ability of the SX/13a — the SX/13a Error Targeting Option and the Extended T1/E1 Simulation Option. The SX/13a Error Targeting Option is internally installed. The Extended T1/E1 Simulation Option is an interface that can be installed in one of the five card slots on the rear panel. Only one of these error targeting options can be enabled at a time. The options operate in a similar manner to target errors to a specific bit and in a specific pattern within formatted or unformatted data streams. Any bit can be targeted, which includes: overhead, framing, parity, data link, signalling, stuffing, alarm, cyclic redundancy check (CRC), and data bits. Bits can be targeted at specific time slots, and into single, continuous, or random multiframes.

These options test the effect of specific error events on the operation of telecommunication equipment. This is useful for equipment design verification and network qualification applications. Additionally, East and West channels can be programmed independently.

The SX/13a Error Targeting Option supports T1, E1, E3, T3, and STS-1 formats. While it extends the SX/13a's error targeting capability, it does not offer additional delay settings. The SX/13a does, however, offer a selection of delays from the menu screens.

The Extended T1/E1 Simulation Option supports T1 and E1 formats. It extends both the SX/13a's error targeting and delay capabilities.

If both time slot delays and error targeting are used, the delay is performed first. The CRC, if any, is recalculated and then errors are injected in the selected positions of the resulting data stream.

Error targeting settings — delay and error parameters — are stored in the SX/13a's battery-backed memory when the SX/13a is turned off. If an extended error targeting option is enabled and the unit is turned off, the setting is retained, and the option is enabled the next time the unit is turned on.

SX/13a Error Targeting Option

When the SX/13a Error Targeting Option is installed, it is indicated on the **SETUP** screen in an Option field. The Option field indicates whether the SX/13a Error Targeting Option is in targeting or pattern mode, and the frame type, if in targeting mode. The mode is also shown on the **MENU** and **MAIN PARAMETERS** screens.

Using the SX/13a Error Targeting Option

1. From the **SETUP** screen, select the Option field and press **ENTER** to display the **SELECT FUNCTION** screen.
2. Choose an error targeting mode: Error Targeting or Pattern Insertion mode.

Error Targeting Mode

One of six error types can be targeted into any of the overhead or data bit locations in the multiframe of a formatted data stream. Six types of errors can be independently programmed for each data bit in a multiframe, in addition to targeting any of the overhead bits. The six error types are: random logic, random space, random mark, forced logic, forced space, and forced mark.

Pattern Insertion Mode

In the Pattern Insertion mode, programmable error patterns can be inserted into random locations in unformatted data streams, such as in a V.35 or HSSI data stream, or into random locations in a formatted data stream, such as T3. The programmable error pattern can be up to 16,000 bits long and can include any of the six available error types. Patterns can be injected independently into either the Eastbound, Westbound, or both data streams. These can be injected into unformatted data streams one at a time, repeatedly, or randomly. The pattern *length* must be the same in both directions. This does not represent much of a limit, though, since the shorter of the two patterns can be padded to the length of the longer pattern with No Error selections for those bits beyond its actual pattern length. In addition to inserting error patterns, Pattern Insertion mode can be used to generate user data, such as frames or blocks, by inserting a pattern of forced 0s and 1s that comprise the desired data. This data would usually be injected into an idle data stream so it does not collide with existing data.

Using the Error Targeting Mode

When the SX/13a Error Targeting Option is enabled, the **ERROR TARGETING** screen displays the current data rate for each channel, if the data rates are in synchronization ("in-sync"). If the data rates are not in-sync, then "no-sync" is displayed. The clock timing and data rate should be "in-sync" before configuring the error targeting parameters. After error targeting is set up, the **<etdiag>** function key can be used to start error targeting diagnostics.

Three parameters must be set for each channel at the **ERROR TARGETING** screen: Error Targeting, Frame Type, and Bits Targeted (see).

Setting the Error Targeting Mode

1. From the **ERROR TARGETING** screen, highlight the Error Targeting field.
2. Choose a targeted error submode: off, continuous, or triggered.

   <off> — Disables error targeting to specific bits. In this submode, the error generators function normally, and errors are applied to any bit in the data stream with equal probability.

   <contin> (continuous) — Errors are targeted continuously (in every multiframe) into those bits programmed to receive targeted errors. Errors defined as one of the forced error types will be applied to every multiframe. Targeted error types override any error type selections made on the **RANDOM ERROR** and **BURST ERROR RATE** screens. Bits targeted to receive random errors receive errors in each multiframe where they coincide with error events from either the random or burst error generators.

   <triggr> (triggered) — Errors are targeted into one or more multiframes based on the Trigger Interval parameter. When the Trigger Interval parameter is set to Manual, errors can be triggered manually into a single multiframe. The trigger function keys are displayed on the **MAIN PARAMETERS** and **STATISTICS** screens:

   <TW> — Triggers the errors into a single, Westbound multiframe

   <TB> — Triggers the errors into one multiframe in each direction

   <TE> — Triggers the errors into a single, Eastbound multiframe

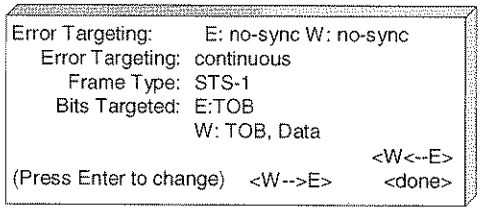

Figure 6.1 SX/13a Error Targeting Screen

Selecting a Framing Format

The Extended T1/E1 option supports 13 frame formats; the SX/13a Error Targeting Option supports 17 frame formats. , , shows the framing types and descriptions supported by each option. Select a frame format before targeting bits. Selecting a new frame format resets the time slot delays and bit error targeting.

To change the current frame format:

1. Select the Frame field and press **ENTER** to display the **SELECT FRAME TYPE** screen.
2. Select the new format and press **ENTER**. When a new format is selected, the bit error targeting and time slot delay settings are set to their default values of no bits and no time slots targeted. The frame type selection determines the bits available for targeting.

Table 6.1 Supported Framing Formats for Error Targeting

SX/13a Error Targeting Option	Extended T1/E1 Simulation Option	Format	Physical Link Type	Description
Yes	No	STS-1	SONET-1 (51.84 Mbps)	SONET (electrical) level 1 frame structure
Yes	No	T3	DS3 (44.736 Mbps)	DS3 basic M-frame structure
Yes	No	T3 C-bit	DS3 (44.736 Mbps)	DS3 using C-bit parity format
Yes	No	E3	G.703 (34.368 Mbps)	G.703 (34.368 Mbps) using G.751 frame structure
Yes	Yes	E1-F framed	G.703 (2.048 Mbps)	G.703 using two frame structures, no multiframe. Data bits are targeted by time slot.
Yes	Yes	E1-Fc clear channel	G.703 (2.048 Mbps)	G.703 using two-frame structure, no multiframe. Data bits are targeted individually.
Yes	Yes	E1-MFs with signalling	G.703 (2.048 Mbps)	G.703 using time slot 16 multiframe with signalling. Data bits are targeted by time slot.
Yes	Yes	E1-MFc clear channel	G.703 (2.048 Mbps)	G.703 using time slot 16 multiframe with signalling. Data bits are targeted individually.
Yes	Yes	E1-CRC4	G.703 (2.048 Mbps)	G.703 using CRC4 multiframe without signalling. Data bits are targeted by time slot.
Yes	Yes	E1-CRC4s with signalling	G.703 (2.048 Mbps)	G.703 using CRC4 multiframe with signalling. Data bits are targeted by time slot.
Yes	Yes	E1-CRC4c clear channel	G.703 (2.048 Mbps)	G.703 using CRC4 multiframe without signalling. Data bits are targeted individually.
Yes	Yes	T1-D3/D4	DS1 (1.544 Mbps)	T1 superframe multiframe structure without signalling. Data bits are targeted by DS0 time slot.
Yes	Yes	T1-D3/D4s with signalling	DS1 (1.544 Mbps)	T1 superframe multiframe structure with signalling. Data bits are targeted by DS0 time slot.
Yes	Yes	T1-D3/D4c clear channel	DS1 (1.544 Mbps)	T1 superframe multiframe structure without signalling. Data bits are targeted individually.
Yes	Yes	T1-ESF	DS1 (1.544 Mbps)	T1 extended superframe structure without signalling. Data bits are targeted by DS0 time slot.

SX/13a Error Targeting Option	Extended T1/E1 Simulation Option	Format	Physical Link Type	Description
Yes	Yes	T1-ESFs with signalling	DS1 (1.544 Mbps)	T1 extended superframe structure with signalling. Data bits are targeted by DS0 time slot.
Yes	Yes	T1-ESFc clear channel	DS1 (1.544 Mbps)	T1 extended superframe structure without signalling. Data bits are targeted individually.

Targeting Bits

The frame type should be selected before targeting bits because the frame type selection determines the bits available for targeting.

Most frame types include several selection screens for different types of targetable bits. Channelized T1 and E1 formats include screens for targeting by time slot. Data bits in the multiframe are displayed on a single, scrollable screen for clear channel frame formats. Use the up and down cursor keys to scroll. The bits are numbered starting from 1 and continue sequentially up to the last data bit of the multiframe.

Framing bits are displayed on separate screens from the data bits. through show the available bit types and numbering for frame formats for the SX/13a Error Targeting Option.

The targeting status of a particular bit (or time slot) is displayed as either a dash (–) when the bit is not selected ("no error"), or as a character representing one of the six error types: R, S, M, E, 0, or 1.

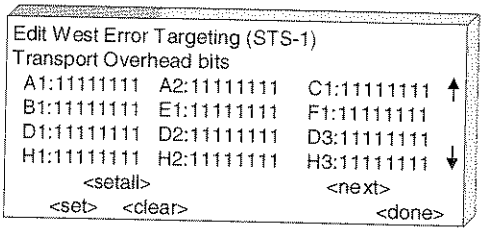

Figure 6.2 Example Editing Screen for Targeting Bits Using STS-1 Frame Format

Targeted Bit Error Types

The error targeting function provides six error types that can be targeted to specific places in the formatted data stream. In addition to these error types, any bit can be selected to receive no errors by selecting **<no-err>**, which is displayed as a dash on the selection screen. and show the error types.

Table 6.2 Targeted Bit Error Types

Error Type	Function Key	Description
Random Logic	<R>	Enables a selected bit position to receive a logic error (bit reversal) when the appropriate error generator creates an error bit for this particular bit time.
Random Space	<S>	Enables a selected bit position to be replaced with a space (or 0) bit when the appropriate error generator creates an error bit for this particular bit time.
Random Mark	<M>	Enables a selected bit position to be replaced with a mark (or 1) bit when the appropriate error generator creates an error bit for this particular bit time.

Depending on the operating mode, the probability of random errors occurring in the selected bit position is determined either by both the random and burst error generators or by the random error generator alone. In Continuous mode, both error generators determine the error probability. In Triggered mode, only the random error generator determines the error probability until an error is triggered. Forced error types generate errors, forced 0s or forced 1s directly, regardless of the error generators. Random error types generate errors, 0s, or 1s when they coincide with error events from the burst error generator.

Table 6.3 Forced Targeted Error Types

Error Type	Selection Key	Description
Forced Logic	<E>	Enables a selected bit position to receive a logic error (bit reversal) at every occurrence of this selected bit in the data stream.
Forced Space	<0>	Enables a selected bit position to receive a logic 0 at every occurrence of this selected bit in the data stream.
Forced Mark	<1>	Enables a selected bit position to receive a logic 1 at every occurrence of this selected bit in the data stream.

Forced errors occur in the selected bit position, regardless of any activity from the random or burst error generators.

Typical Error Targeting Setup

1. From the **ERROR TARGETING** screen, highlight the Bits Targeted field.
2. Select the East or West channel.
3. Press **ENTER**. The edit screen displayed depends on the frame type.
4. Bits can be targeted individually, all at one time, or all cleared at one time. Choose one of the following:

   <set> — Selects individual bits to be targeted. Use the cursor keys to highlight the bit to be targeted and select the function key.

   <setall> — Selects all bits to be targeted. Use the cursor keys to highlight the bit to be targeted and select the function key.

   <clrall> — Clears all targeted bits.

Data Bits Screens

Use the up and down cursor keys to show more data bits. Or use the **<go to>** function key to go to a specific bit, or the first or last bit. The **<repeat>** function key can be used to specify a range of bits as a pattern. The pattern can be repeated a specified number of times and can start at a specific bit.

Once a bit or all bits are set to be targeted, select an error type.

Most frame types include several different types of targetable bits. These are displayed on several subscreens. Use **<next>** and **<prev>** to display the different bit-type selection screens.

Using a Bit Mask for Channelized T1 and E1

The Bit Mask field on selection screens is used to select the time slots which will receive errors in the channelized T1 or E1 formats. For the specified time slots, select eight bits in each time slot that will receive the programmed errors. Use **<b-mask>** on the **TIME SLOT** screen to enable any or all of the eight time-slot bits. Bits may be enabled or disabled using the cursor keys, or **<enable>** or **<disabl>**. Enabled bits are displayed as an asterisk (*); disabled bits are displayed as a dash (–). Select **<done>** when the desired bits have been enabled. The default settings for the bits are all enabled. The bits are numbered 1 through 8, with 1 being the first bit in the time slot.

Copying Targeted Bit Selections

1. Target bits for one channel, either East or West.
2. From the **ERROR TARGETING** screen, select **<W←E>** (copy East to West) or **<W→E>** (copy West to East).
3. Edit the copied selection as necessary.

Targetable Bits Reference

STS-1 (SONET) Format

Frame Type Setting: STS-1

Setup Screens: Transport Overhead Bits
Data Bits

Table 6.4 STS-1 Bit Types

Bit to Target	Number of Targetable Bits
A1, A2 bits	16
B1, B2 bits	16
C1 bits	8
D1–D12 bits	96
E1 bits	8
F1 bits	8
H1, H2, H3 bits	24
K1, K2 bits	16
Z1, Z2, Z3 bits	24
Data bits	6264 (bits can be selected individually)

Table 6.5 STS-1 Data Bits

Row Number	Data Bit Numbers
1	1–696
2	697–1392
3	1393–2088
4	2089–2784
5	2785–3480
6	3481–4176
7	4177–4872
8	4873–5568
9	5569–6264

T3 and T3 C-Bit Format

Frame Type Setting: T3
T3 and T3 C-Bit

Setup Screens: X-, P-, M-Bits
F-Bits
C-Bits
Data Bits

Table 6.6 T3, T3 C-Bit Types

Bit to Target	Number of Targetable Bits
X bits	2
P bits	2
M0, M1, M0 bits	3
F bits	28
C bits	21 (meaning of bits varies with format)
Data bits	4704 (bits can be selected individually)

Table 6.7 T3, T3 C-Bit F-Bits

	Subframe Block Number							
Subframe	1	2	3	4	5	6	7	8
1	1–84	85–168	169–252	253–336	337–420	421–504	505–588	589–672
2	673–756	757–840	841–924	925–1008	1009–1092	1093–1176	1177–1260	1261–1344
3	1345–1428	1429–1512	1513–1596	1597–1680	1681–1764	1765–1848	1849–1932	1933–2016
4	2017–2100	2101–2184	2185–2268	2269–2352	2353–2436	2437–2520	2521–2604	2605–2688
5	2689–2772	2773–2856	2857–2940	2941–3024	3025–3108	3109–3192	3193–3276	3277–3360
6	3361–3444	3445–3528	3529–3612	3613–3696	3697–3780	3781–3864	3865–3948	3949–4032
7	4033–4116	4117–4200	4201–4284	4285–4368	4369–4452	4453–4536	4537–4620	4621–4704

E3 Format

Frame Type Setting: E3
G.703 (34.368 Mbps) with G.751 framing structure

Setup Screens: F-, A-, N-Bits
C, T-Bits
Data Bits

Table 6.8 E3 Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	10
Alarm (A) bit	1
National (N) bit	1
C bits	12
Tributary justification (T) bits	4
Data bits	1508 (bits can be selected individually)

Table 6.9 E3 Data Bits

Frame Data Set	Data Bit Numbers
Set 1 (bits 13–384)	1–372
Set 2 (bits 5–384)	373–752
Set 3 (bits 5–384)	753–1132
Set 4 (bits 9–384)	1133–1508

E1-F Format

Frame Type Setting: E1-F
The G.703 (2.048 Mbps) with two-frame/no multiframe structure format is intended for channelized applications of basic E1.

Setup Screens: Slot-0
Time Slots (1–31)

Table 6.10 E1-F Bits and Time Slots

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	16
Data time slots (31)	Selected by 8-bit time slots only; bits not individually selectable

E1-Fc Clear Channel Format

Frame Type Setting: E1-Fc
The G.703 (2.048 Mbps) with two-frame/no multiframe structure format is intended for clear channel (unchannelized) applications of basic E1. Numbering of the data bits for error targeting into this format is bits 1–248 for frame 0, and bits 249–496 for frame 1.

Setup Screens: Slot-0
Data Bits

Table 6.11 E1-Fc Bit Types

Bit to Target	Number of targetable bits
Frame alignment (F) bits	16
Data bits	496 (bits can be selected individually)

E1-MFs with Signalling Format

Frame Type Setting: E1-MFs
The E1-MFs multiframed/signalling format G.703 (2.048 Mbps) with time slot-16 multiframe structure with signalling format is intended for channelized applications of multiframe E1.

Setup Screens: Slot-0
Frame-0 Slot-16
Signalling for Time Slot
Time Slots (1–15 and 17–31)

Table 6.12 E1-MFs Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	128
Multiframe sync bits	4
Alarm/Spare (xyxx) bits	4
Time slot signalling (abcd) bits	120
Data time slots (30)	Selected by 8-bit time slots only; bits not individually selectable

E1-MFc Clear Channel Format

Frame Type Setting: E1-MFc
The E1-MFc clear channel format G.703 (2.048 Mbps) with time slot-16 multiframe structure format is intended for clear channel (unchannelized) applications of multiframe E1.

Setup Screens: Slot-0
Frame-0 Slot-16
Signalling for Time Slot
Data Bits

Table 6.13 E1-MFc Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	128
Multiframe sync bits	4
Alarm/Spare (xyxx) bits	4
Time slot signalling (abcd) bits	120
Data bits	3840 (bits individually selectable)

Table 6.14 E1-MFc Data Bit Multiframe Numbering

Frame	Data Bits	Frame	Data Bits
0	1–240	8	1921–2160
1	241–480	9	2161–2400
2	481–720	10	2401–2640
3	721–960	11	2641–2880
4	961–1200	12	2881–3120
5	1201–1440	13	3121–3360
6	1441–1680	14	3361–3600
7	1681–1920	15	3601–3840

E1-CRC4 Format

Frame Type Setting: E1-CRC4
The E1-CRC4 (CRC4 multiframe) format G.703 (2.048 Mbps) with CRC4 multiframe structure format is intended for channelized applications of CRC4 multiframe E1 without signalling.

Setup Screens: Slot-0
Time Slots (1–31)

Table 6.15 E1-CRC4 Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	128
Data time slots (31)	Selected by 8-bit time slots only; bits not individually selectable

E1-CRC4s with Signalling Format

Frame Type Setting: E1-CRC4s
The E1-CRC4s with signalling format G.703 (2.048 Mbps) with CRC4 multiframe structure with signalling format is intended for channelized applications of CRC4 multiframe E1 with time slot-16 signalling.

Setup Screens: Slot-0
Frame-0 Slot-16
Signalling for Time Slot
Time Slots (1–15 and 17–31)

Table 6.16 E1-CRC4s Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	128
Multiframe sync bits	4
Alarm/Spare (xyxx) bits	4
Time slot signalling (abcd) bits	120
Data time slots (30)	Selected by 8-bit time slots only; bits not individually selectable

E1-CRC4c Clear Channel Format

Frame Type Setting: E1-CRC4s
The E1-CRC4c clear channel format G.703 (2.048 Mbps) with CRC4 multiframe structure format is intended for clear channel (unchannelized) applications of CRC4 multiframe E1.

Setup Screens: Slot-0
Data Bits

Table 6.17 E1-CRC4c Bit Types

Bit to Target	Number of Targetable Bits
Frame alignment (F) bits	128
Data bits	3968 (bits individually selectable)

Table 6.18 E1-CRC4c Data Bit Numbering

Frame	Data Bits	Frame	Data Bits
0	1–248	8	1985–2232
1	249–496	9	2233–2480
2	497–744	10	2481–2728
3	745–992	11	2729–2976
4	993–1240	12	2977–3224
5	1241–1488	13	3225–3472
6	1489–1736	14	3473–3720
7	1737–1984	15	3721–3968

T1-D3/D4 Format

Frame Type Setting: T1-D3D4
The T1-D3/D4 format (superframe without signalling) format is intended for channelized applications of superframe T1-D3/D4 without signalling.

Setup Screens: F_T, F_S-Bits
DS0 Time Slots

Table 6.19 T1-D3/D4 Bit Types

Bit To Target	Number of targetable bits
Framing F_T bits	6
Multiframing F_S bits	6
DS0 time slots	24 time slots only; bits not individually selectable

T1-D3/D4s with Signalling Format

Frame Type Setting: T1-D3D4s
The T1-D3/D4s with signalling format is intended for channelized applications of superframe T1-D3/D4 with signalling.

Setup Screens: F_T, F_S-Bits
Signalling Bits
DS0 Time Slots

Table 6.20 T1-D3/D4s with Signalling Bit Types

Bit to Target	Number of Targetable Bits
F_T bits	6 (framing pattern)
F_S bits	6 (multiframe pattern)
Signalling bits A, B	48
DS0 time slots	24 (selected by 8-bit time slots only; bits not individually selectable)

T1-D3/D4c Clear Channel Format

Frame Type Setting: T1-D3D4c
The T1-D3/D4c clear channel format is intended for clear channel (unchannelized) applications of superframe T1.

Setup Screens: F_T, F_S-Bits
Data Bits

Table 6.21 T1-D3/D4c Bit Types

Bit to Target	Number of Targetable Bits
F_T bits	6 (framing pattern)
F_S bits	6 (multiframe pattern)
Data bits	2304 (bits individually selectable)

Table 6.22 T1-D3/D4c Data Bit Numbering

Frame Number	Data Bit Numbers	Frame Number	Data Bit Numbers
1	1–192	7	1153–1344
2	193–384	8	1345–1536
3	385–576	9	1537–1728
4	577–768	10	1729–1920
5	769–960	11	1921–2112
6	961–1152	12	2113–2304

T1-ESF Format

Frame Type Setting: ESF
The T1-ESF format (extended superframe without signalling) is intended for channelized applications of extended superframe T1 without signalling.

Setup Screens: FDL, FPS, CRC-Bits
DS0 Time Slots

Table 6.23 T1-ESF Bit Types

Bit to Target	Number of Targetable Bits
Data Link (FDL) bits	12
Framing Pattern (FPS) bits	6
Multiframe CRC bits	6
DS0 time slots (24)	Selected by 8-bit time slots only; bits not individually selectable

T1-ESFs with Signalling Format

Frame Type Setting: T1-ESF
The T1-ESFs with signalling format is intended for channelized applications of extended superframe T1 with signalling.

Setup Screens: F_T, F_S-Bits
Signalling Bits
DS0 Time Slots

Table 6.24 T1-ESFs with Signalling Bit Types

Bit to Target	Number of Targetable Bits
Data Link (FDL) bits	12
Framing Pattern (FPS) bits	6
Multiframe CRC bits	6
Signalling bits	ABCD (96)
DS0 time slots (24)	Selected by 8-bit time slots only; bits not individually selectable

T1-ESFc Clear Channel Format

Frame Type Setting: T1-ESFc
The T1-ESFc clear channel format is intended for clear channel (unchannelized) applications of extended superframe T1.

Setup Screens: FDL, FPS, CRC-Bits
Data Bits

Table 6.25 T1-ESFc Bit Types

Bit to Target	Number of Targetable Bits
Data Link (FDL) bits	12
Framing Pattern (FPS) bits	6
Multiframe CRC bits	6
Data bits	4608 (bits individually selectable)

Table 6.26 T1-ESFc Data Bit Numbering

Frame	Data Bits	Frame	Data Bits
1	1–192	13	2305–2496
2	193–384	14	2497–2688
3	385–576	15	2689–2880
4	577–768	16	2881–3072
5	769–960	17	3073–3264
6	961–1152	18	3265–3456
7	1153–1344	19	3457–3648
8	1345–1536	20	3649–3840
9	1537–1728	21	3841–4032
10	1729–1920	22	4033–4224
11	1921–2112	23	4225–4416
12	2113–2304	24	4417–4608

Using the Pattern Insertion Mode

Pattern Insertion mode is used to configure targeted-error patterns. When the Pattern Insertion mode is enabled, the **<pttrn>** function key is displayed on the **MAIN PARAMETERS** or **MENU** screen. As with the other parameters, all Pattern Insertion parameters are retained in the SX/13a's battery-backed memory.

The Pattern Insertion mode settings are:

- On or off
- Pattern length
- Pattern bit selection for the East and West channels

Bit-error patterns can be inserted into the data stream individually, repeatedly, or randomly as determined by the gap length parameter. Gap length is set on the **MAIN PARAMETERS** screen. Single-pattern insertions are created by setting the gap length to manual.

When set to manual, pattern insertions are triggered similarly to burst errors by using function keys. The function keys **<PW>**, **<PE>**, and **<PB>** are displayed on the **MAIN PARAMETER** screen to insert single patterns on either the West channel, East channel, or both.

To use random error types in patterns, set the gap length and pattern density parameters on the **MAIN PARAMETER** screen. These should be set as needed for the desired insertion interval and error rate for random error types during the pattern. Create repeating and random pattern insertions by setting the gap length to either fixed-millisecond or random-millisecond time values, respectively.

Select **<off>** to disable pattern insertion mode. When pattern insertion is disabled, the SX/13a's error generators function normally and are applied to any bit in the data stream with equal probability.

The contents of each inserted pattern are determined by the error types defined for the individual bits that comprise that pattern. The error types are the same six available in error targeting mode, as shown in and . Forced error types generate errors, forced 0s or forced 1s directly, regardless of the error generators. Random error types generate errors, 0s, or 1s when they coincide with error events from the burst error generator.

NOTE: The random error generator has no effect on bits inserted in the Pattern Insertion mode.

Choosing the Pattern Insertion Mode

1. On the **SETUP** screen, highlight the Option field for the SX/13a Error Targeting Option and press **ENTER**.
2. On the **SELECT FUNCTION** screen, highlight Pattern Insertion and press **ENTER** to display the **ERROR PATTERN INSERTION** screen.
3. Configure the three settings: Pattern Insertion, Pattern Length, and Edit Pattern. The Edit Pattern field appears when a positive value is entered for the Pattern Length field.
4. Select **<on>** to enable the Pattern Insertion mode.

Setting the Pattern Length

The pattern length parameter determines the length of the pattern to be inserted on the East and West channels. The programmable pattern can be up to 16,000 bits long; however, the pattern length must be identical in both directions. This does not represent much of a limit, though, since the shorter of the two patterns can be padded to the length of the longer pattern with No Error selections for those bits beyond its actual pattern length.

1. From the **ERROR PATTERN INSERTION** screen, highlight the Pattern Length field.
2. Enter the number of bits for the pattern length and press **ENTER**.
3. The cursor is moved to the Edit Pattern field for the East channel.

If the pattern length is set to 0, no function lines for entering or e diting the East or West patterns are displayed. Once the length is set to a value other than 0, two lines appear on the **ERROR PATTERN INSERTION** screen for editing the patterns.

Editing Pattern Bits

1. Set the pattern length.
2. From the **ERROR PATTERN INSERTION** screen, highlight the Edit Pattern field for either the East or West channel.
3. Use the keys defined in to edit the pattern. These are the same keys as found in the Error Targeting mode.

Table 6.27 Error Targeting Function Keys

Key	Description
<set>	Changes the menu of the entry screen to provide function keys for entering the six available error types (1, 0, E, M, S, R) or the "no error" option into any of the pattern bits. To assign an error type to a bit after selecting **<set>**, highlight the bit with the cursor keys and press the appropriate error type function key. When all the entries are complete, press the **<done>** function key to return to the editing menu. *NOTE: Holding down an error type function key causes the key to auto-repeat the same value to subsequent bits.*
<set all>	Functions similarly to the **<set>** command, except the error type selected is applied to all bits of the pattern.
<clear all>	Clears all the bits or time slots and sets them to the "no error" condition.
<go to>	Moves the cursor directly to any specific pattern bit number or to the first or last bit of the pattern.
<repeat>	Used to enter repetitive error patterns quickly. This function key copies any specified block of bit error definitions to any other bits in the pattern. Define the starting and ending bit numbers from which to copy, the number of copies desired, and the bit number to which to begin copying.
Cursor Keys	The cursor keys can be used to access bits anywhere in the pattern. If the cursor moves above the top or below the bottom of the currently displayed section of a long pattern, the displayed pattern bits will scroll up or down.

SX/13a Error Targeting Diagnostics

Diagnostics for the SX/13a Error Targeting Option are run from the Error Targeting mode, unlike other diagnostics.

The diagnostics tests are:

- East and West framing RAM
- East and West targeting RAM
- East and West SYNC1 logic
- East and West SYNC2 logic
- East and West targeting logic

Running SX/13a Error Targeting Option Diagnostics

1. On the SETUP screen, highlight the second Option field for the SX/13a Error Targeting Option and press **ENTER**.
2. From the Error Targeting screen, select **<contin>** or **<triggr>**.
3. Select **<etdiag>** to display the ERROR TARGETING DIAGNOSTICS screen.
4. Select **<single>** to run the diagnostic test sequence once, or select **<contin>** to run the diagnostics repeatedly.

   The status of each test for each channel is shown as the tests are run; the results are shown as either passed or failed. The testing can be canceled at any time by selecting **<done>**.

NOTE: If this diagnostic test generates a failed message, contact Technical Support for assistance in determining a course of corrective action.

Extended T1/E1 Simulation Option

Without the Extended T1/E1 Simulation Option, the SX/13a's main channel delay is applied to the entire T1 or E1 data stream. In this case, all framing bits, overhead bits, and DS0 time slots experience the same main channel delay. The Extended T1/E1 Simulation Option adds variable delays to DS0 time slots in the T1 or E1 data stream. If both time slot delays and error targeting are used, the delay is performed first. The CRC, if any, is recalculated and then errors are injected in the selected positions of the resulting data stream.

With the Extended T1/E1 Simulation Option installed and enabled, two sets of delay values, known as *delay taps*, are used to independently define the delay that is applied to each DS0 time slot. Meanwhile, the framing and overhead bits continue to experience the normal, main channel delay. Depending on which delay mode is selected, there are either ten or nine available delay taps that can be applied to each DS0 time slot. These delay taps *cannot* have their delay times set to randomly programmed values.

Due to the SX/13a's battery-backed memory, if the Extended T1/E1 Simulation Option was enabled and then the unit is turned off, the option will be enabled when the unit is turned on, and all extended T1/E1 delay and error parameters will be restored.

Enabling the Extended T1/E1 Simulation Option

1. From the **SETUP** screen, highlight the Option field and press **ENTER** to display the **EXTENDED T1/E1 SIMULATION** screen.
2. Select **<on>** to enable the Extended T1/E1 Simulation Option.
3. Once the option is enabled, **<XT1/E1>** is displayed on the **MAIN PARAMETERS** and **MENU** screens. The setup screen can be displayed by selecting this function key.

NOTE: When enabled, the option does not operate until it is in synchronization with the incoming data stream.

The ten parameter and status fields are shown in .

Table 6.28 Extended T1/E1 Simulation Option Parameters

Parameter	Description
XT1/E1	Enables or disables the Extended T1/E1 Simulation Option
E:/W:	The East and West channel data stream rates are displayed in the upper right corner of the screen. If the proper frame format is selected, the option is enabled, and a data stream is running through the SX/13a; this indicates that the module is in-sync. If there is a problem with the setup or no data stream is entering the SX/13a, the display reads "E: no-sync W: no-sync." Synchronization must be achieved before the option will target errors and inject time slot delays. If the unit is not in synchronization (in-sync), verify that the proper frame format is selected, the SX/13a's main parameters are set correctly, and formatted data is actually passing through the SX/13a.
Frame	Displays the **SELECT FRAME TYPE** screen to select a frame format.
Errors	Sets "continuous" or "triggered."
E	Displays the East channel edit screen to target bits. The screen displayed depends on the frame type chosen.
W	Displays the West channel edit screen to target bits. The screen displayed depends on the frame type chosen.
Tap	Sets a value for the delay tap. The tap can be set in milliseconds or frames.
Delay	The choices are one group or two groups. The one group setting uses the delay from the main parameters as a base with up to eight taps. The two-group setting uses zero (with up to three taps) or the main parameters delay as a base (with up to four taps).
E: 1, 2, 3, 4, 5, 6... (typical)	Sets and displays the East channel time slot delays.
W: 1, 2, 3, 4, 5, 6... (typical)	Sets and displays the West channel time slot delays.

Understanding Time Slot Delays

View or assign delay taps to the time slots in the T1 or E1 frames at the **TIME SLOT DELAY** screen for the East and West channels. To display the screen, press **ENTER** from the E: 1, 2, 3, 4... field. The screen assigns delay taps to time slots.

The following variables can effect the delay tap calculation:

- Main parameter delay (set on the **MAIN PARAMETERS** screen)
- Delay tap (milliseconds or frames)
- One- or two-groups delay (determines the base delay used, to which taps are added)
- Delay tap multiplier (chosen with function keys on the time slot delay screens)
- Frame format (determines the tap interval)

Depending on whether one or two groups are selected, there are either ten or nine delay taps available that can be applied to each DS0 time slot.

The delay is calculated as follows:

TS#:base+tap

Where **TS#** is the DS0/time slot number;

base is the main channel delay displayed in milliseconds or frames;

tap is the delay tap interval x N displayed in milliseconds or frames (when it is present on a particular delay tap).

There are two sets of available function keys that correspond to delay taps. Toggle between sets with **<more>** and **<prev>**. The available sets depend on whether one group or two groups is selected.

Setting the Tap

The delay tap interval is displayed and entered in the Tap field. The delay tap interval determines the delay spacing between the delay taps in the time slot delay function. Set this parameter in either milliseconds or frames. Valid values are 1 to 16 milliseconds, or 1 to 128 frames. Each frame of delay represents a one-byte delay (equivalent to 0.125 milliseconds) for that time slot. A millisecond tap interval represents an eight-frame delay, which is 8 bytes of delay for each time slot.

When a frame format that uses signalling is selected, signalling bit positions must be maintained. This is accomplished by limiting the values for this field to a multiple of a multiframe. For T1 streams the main channel delay and the delay tap interval must be a multiple of 3 milliseconds. For T1-ESF, the main channel delay and the delay tap interval must be a multiple of 24 frames. For T1- D3/D4, the main channel delay and the delay tap interval must be a multiple of 12 frames. For E1 streams that use in-band signalling, the main channel delay and the delay tap interval must be a multiple of 2 milliseconds (or 16 frames).

Choosing a Delay

The One Group delay has nine available delay taps; the Two Group delay has ten.

To help understand time slot delays, use the examples, , and .

One Group Example

Frame Type: T1-D3D4
Delay on the MAIN PARAMETERS Screen: 40 milliseconds (this is the base channel delay)
Tap: 4 milliseconds
Delay: One Group

Two Groups Example

Frame Type: T1-D3D4 (24 time slots)
Delay on the MAIN PARAMETERS Screen: 40 milliseconds
Tap: 4 milliseconds
Delay: Two Groups

Table 6.29 One-Group Delays Calculations

Function Key	Time Slot Delay Setting	Added Delay
<0>	No Delay	0 ms
<base>	Channel Delay (i.e., 40 ms)	40 ms
<b+1tap>	Channel Delay + (Tap Interval x 1)	40 ms + 4 ms = 44
<b+2tap>	Channel Delay + (Tap Interval x 2)	40 ms + 8 ms = 48
<b+3tap>	Channel Delay + (Tap Interval x 3)	40 ms + 12 ms = 52
<b+4tap>	Channel Delay + (Tap Interval x 4)	40 ms + 16 ms = 56
<b+5tap>	Channel Delay + (Tap Interval x 5)	40 ms + 20 ms = 60
<b+6tap>	Channel Delay + (Tap Interval x 6)	40 ms + 24 ms = 64
<b+7tap>	Channel Delay + (Tap Interval x 7)	40 ms + 28 ms = 68
<b+8tap>	Channel Delay + (Tap Interval x 8)	40 ms + 32 ms = 72

Table 6.30 Two-Group Delays Calculations

Function Key	Time Slot Delay Setting	Added Delay
<0>	No Delay	0
<0 + 1tap>	No Delay + Tap Interval x 1	0 + 4 ms = 4
<0 + 2tap>	No Delay + Tap Interval x 2	0 + 8 ms = 8
<0 + 3tap>	No Delay + Tap Interval x 3	0 + 12 ms = 12
<base>	Channel Delay	40 ms
<b + 1tap>	Channel Delay + (Tap Interval x 1)	40 + 4 ms = 44
<b + 2tap>	Channel Delay + (Tap Interval x 2)	40 + 8 ms = 48
<b + 3tap>	Channel Delay + (Tap Interval x 3)	40 + 12 ms = 52
<b + 4tap>	Channel Delay + (Tap Interval x 4)	40 + 16 ms = 56

The delay times provided by delay taps 1 through 9 are determined by the main channel delay and a tap interval parameter. The practical application of this mode is when all the channels are traveling the same basic transmission path, but there might be some small variation between the individual DS0/time slot delays due to switching and cross-connect equipment. Delay taps 1 through 9 could be assigned to various time slots to simulate this situation.

Delay number 0 could be used when there is a large delay difference between some of the time slots. In that case, one or more time slots could be assigned to delay 0 while the others would be assigned to delay taps 1 through 9.

The default time slot delay assignment is delay tap 1 (the main channel delay) for all time slots, which is what occurs when the option is disabled. These two delay tap groups can simulate two very different transmission paths for the time slots, each of which has some variation in the delays experienced by individual time slots traveling that path. For example, some of the time slots could be over a satellite path while the others may take a terrestrial path. For each of these paths, there may be slight variations in time slot delay due to switching equipment.

The same parameters used in the one group mode (main channel delay and tap interval) determine the tap delays in the two groups mode (see).

Table 6.31 Comparison of One Group and Two Groups

One Group Mode		*Two Groups Mode*	
Delay Tap	**Time Slot Delay Setting**	**Delay Tap**	**Time Slot Delay Setting**
0	No Delay	0	No Delay
1	Channel Delay	1	No Delay+Tap Interval x 1
2	Channel Delay+Tap Interval x 1	2	No Delay+Tap Interval x 2
3	Channel Delay+Tap Interval x 2	3	No Delay+Tap Interval x 3
4	Channel Delay+Tap Interval x 3	4	Channel Delay
5	Channel Delay+Tap Interval x 4	5	Channel Delay+Tap Interval x 1
6	Channel Delay+Tap Interval x 5	6	Channel Delay+Tap Interval x 2
7	Channel Delay+Tap Interval x 6	7	Channel Delay+Tap Interval x 3
8	Channel Delay+Tap Interval x 7	8	Channel Delay+Tap Interval x 4
9	Channel Delay+Tap Interval x 8	9	Not Assigned

For either mode, the main channel delay can be set to any valid channel delay value in milliseconds or frames. The main channel delay is always applied to the framing bits of the data stream.

Formats of T1 and E1 streams that use signalling put additional constraints on the values of the tap interval and the main channel delay parameters. Signalling bits are carried in the time slots of these streams. For proper functioning of the downstream equipment, these signalling bits must be delayed by times that are a multiple of a multiframe length, or they will be moved to the wrong location in another multiframe, upsetting signalling. For T1 streams that use in-band signalling, the main delay and the tap interval must be a multiple of 3 milliseconds (or 24 frames for ESF, 12 frames for D3/D4 if set in frames) — the length of a multiframe. This ensures that the signalling bits arrive in the same position in another multiframe. For E1 streams that use in-band signalling, the main channel delay and the tap interval must be a multiple of 2 milliseconds (or 16 frames), which is the length of an E1 multiframe. This ensures that the signalling bits arrive in the same position in another E1 multiframe.

East and West Delay Settings

The bottom two fields of the right column of the display are used to select the delay taps assigned to time slots for the East and West channels. They also provide a summary of the time slots currently assigned to delay taps.

A typical display might look like "E:1,2,3,4,5,6..." where the numbers are the time slotnumbers in the T1 or E1 frame. In this example, the East channel time slots 1 through 6 and possibly more are assigned to a delay tap that is greater than 0 delay.

Function keys are provided to copy the delay tap selections from one channel to the other when one of these two fields is highlighted. To view or change the delay tap selections, highlight the East or West field with the cursor keys and press **ENTER**. This displays a **TIME SLOT DELAY** screen for that channel direction.

East and West Error Targeting Settings

The bottom two fields of the left column of the display are used to select the bits to be targeted for errors for the East and West channels. They also provide a summary of the bits that are currently targeted to receive errors. A typical display might look like "E:FT,FS, Data for T1 D3/D4 format." In this example the East channel is targeted to receive errors in the F_T and F_S framing bits as well as in the data bits of the frame. Function keys are provided to copy the targeted bit selections from one channel to the other when one of these two fields is highlighted. To view or change the targeted bit selections, highlight the East or West field with the cursor keys and press **ENTER**. This displays the first of a series of error targeting screens for that channel direction.

Operating the Targeted Error Mode

After assigning error types to the desired bits, return to the targeting screen to make sure that targeting is set to the desired operating mode and is in synchronization with the data stream befor e continuing.

If targeting is set to the "Off" mode, the targeting function will have no effect on error injection.

If targeting is set to either the "continuous" or "triggered" mode, but the SX/13a is not in sync with the incoming stream, no errors will be injected. This could occur, for example, if the wrong format was selected, or if the data stream was unformatted.

Chapter 7. Remotely Operating the SX/13a

There are two options that extend the remote operating functionality of the SX/13a: the IEEE-488 Remote Control Interface and the RS-232-C Remote Control Interface. Both provide the same functionality, but each supports different hardware. The IEEE-488 Remote Control Interface connects the SX/13a mainframe to controller, such as a PC. The RS-232-C Remote Control Interface connects the SX/13a mainframe to a controller, such as a PC or any controller that can emulate a VT-100 terminal.

IEEE-488 Remote Control Interface

The IEEE-488 Remote Control Interface controls the SX/13a remotely using an IEEE-488 controller, a PC, or a workstation equipped with an IEEE-488 port and communications software. This module supports controllers and computers that accept ANSI screen commands to improve the appearance of the screen display. However, the remote control interface will also function with display devices that do not recognize ANSI screen codes.

With the IEEE-488 Remote Control Interface, any SX/13a operation that can be performed by pressing a key on the mainframe's front panel can be executed with remote commands.

Setting Up the IEEE-488 Remote Control Interface

To modify the IEEE-488 Remote Control Interface parameters:

1. Display the **SETUP** screen on the SX/13a unit.
2. Highlight the remote Option field and select the IEEE-488 Remote Control Interface.
3. Set the parameters and select **<done>**.

   The parameters are as follows:

   Device Address — An address was assigned at the controller for the IEEE device during software installation. The device address setup for this field should be the same address. Set an address between 1 and 30. The address 00 is reserved for the bus master and should not be used as the device address.

   ANSI Mode —

   <on> — ANSI commands are sent to the controller to determine the display attributes of text, such as highlighting, blinking, cursor positioning, and so on. This helps to duplicate the SX/13a's screen appearance as closely as possible on the controller screen.

   <off> —ANSI commands are *not* used, and the ANSI character attributes are replaced by ASCII braces { } to indicate highlighted or blinking areas of the SX/13a's screen.

   ANSI Home — If ANSI Mode is "on," this parameter is used to position the SX/13a's screen display at a fixed position on the controller's screen. The row and column position determine where the upper left corner of the SX/13a screen is displayed on the controller screen.

Using the IEEE-488 Remote Commands

The IEEE-488 remote commands are divided into three groups:

- **Front panel key commands** — These can accomplish any function that is usually performed by pressing keys on the SX/13a's front panel.
- **Commands not available from the SX/13a keypad** — These commands perform functions specifically related to remote control and are not available through the SX/13a keypad.
- **Direct function commands that perform a specific function** — These provide a more direct method of performing frequently used functions that would otherwise be accessed through the front panel key commands, but are quicker to access through these direct functions.

The Remote Control Command Reference section, on page 7-7, includes complete lists of the available commands and corresponding keys for the front panel of the SX/13a and the remote controller.

The basic conventions for the remote commands are:

- IEEE-488 remote commands consist of alphanumeric ASCII characters. Each command begins with a one- or two-character mnemonic and ends with a CR (carriage return) terminator. The exceptions are:
  - 0–9
  - Space (only a space before the command is permitted)
  - Period
  - C
- Uppercase and lowercase letters may be used interchangeably.
- Multiple functions can be entered on the same line by separating them with a space or semi-colon delimiter. The last function must end with a CR terminator.

When entering a multiple-digit number, numeric entry does not need to be terminated individually with a CR or command delimiter. A sequence can be sent to the SX/13a in a string terminated with a single CR. After sending a numeric string to the SX/13a, the parameter can be accepted with a second CR, which is equivalent to pressing **ENTER** on the SX/13a front panel.

NOTE: If the controller does not allow a single CR to be sent, send an "E" mnemonic to the SX/13a. This mnemonic represents the SX/13a ENTER key.

Using the IEEE-488 Interface Functions

The SX/13a implements the following IEEE-488 interface functions:

- Serial polling
- Interface clear
- Remote/Local/Local lockout
- Device clear
- Group execute trigger

Serial Polling

A service request interrupt is generated when certain error conditions occur. The device causing the interrupt will have its service request bit set when the next serial poll is performed. Performing a serial poll to the SX/13a causes a status byte to be output with the following bits:

- Bit 0 (01H) = Command syntax error
- Bit 1 (02H) = Command unavailable error
- Bit 2 (04H) = Download CRC error
- Bit 6 (40H) = Request Service Bit 1

The error bits are only valid the first time the serial poll byte is read in response to Request Service Bit 1 being set. Request Service Bit 1 is automatically cleared after the serial poll byte is read. The error bits are not cleared; instead, they remain unchanged until the next error occurs. The error bits are not valid and should be ignored any time Request Service Bit 1 is not set.

Interface Clear

Stops any pending input or output transmission.

Remote/Local/Local Lockout

Complete capability is available. Normal keyboard operation is possible whenever the SX/13a is not processing a remote command. If local operation is not desirable, send the IEEE Local Lockout command to disable the front panel keys until the IEEE Local command is sent.

Device Clear

Resets the SX/13a to its power-up state.

Group Execute Trigger

Continues running an SX/13a program that is waiting for a manual trigger.

RS-232-C Remote Control Interface

The RS-232-C Remote Control interface controls the SX/13a remotely using an RS-232-C controller, a PC, or a workstation equipped with an RS-232-C port and communications software. This module supports terminals and computers that accept ANSI screen commands to improve the appearance of the screen display. However, the RS-232-C Remote Control interface also functions with display devices, such as basic ASCII terminals, that do not recognize ANSI screen codes. Any terminal that supports VT-100 can be used.

Any SX/13a operation that can be performed by pressing a key on the mainframe's front panel can be executed with remote commands.

Setting Up the RS-232-C Remote Control Interface

First, the communications and terminal parameters must be defined. Set the communications parameters, including the baud rate, number of stop bits, and parity, on both the SX/13a mainframe and on the controller software. The settings must be defined and be the same. Set the data bits to 8 bits with no parity.

To ensure that the controller displays the SX/13a screens as accurately as possible, the controller connected to the SX/13a should support ANSI commands. ANSI commands permit the controller screen to display the SX/13a screen in a fixed position at all times. Without ANSI, any SX/13a screen displayed scrolls upward as new commands are entered.

These communication and terminal parameters are retained in the SX/13a's battery-backed memory when the unit is turned off.

Using the RS-232-C Communication and Terminal Parameters

To modify the RS-232-C settings:

1. From the MENU screen, select **<setup>**.
2. Highlight the Remote field. Press **ENTER** to display the SETUP **RS-232-C** REMOTE screen.
3. Change the following parameters as necessary:

   Baud Rate — 19200, 9600, 4800, 2400, 1200, 600, or 300

   Parity — None, Odd, or Even

   Stop Bits — 1 or 2

   Auto Display —

   <on> — The SX/13a sends a copy of its display to the terminal after every command is executed.

   <off> — A copy of the display is only sent when requested from the terminal using the RD command (read current SX/13a display).

ANSI Mode —

<on> —ANSI commands are sent to the controller to determine the display attributes of text, such as highlighting, blinking, cursor positioning, and so on. This helps to duplicate the SX/13a's screen appearance as closely as possible on the controller screen.

<off> —ANSI commands are *not* used and the ANSI character attributes are replaced by ASCII braces { } to indicate highlighted or blinking areas of the SX/13a's screen.

ANSI Home — If ANSI Mode is "on," this parameter is used to position the SX/13a's screen display at a fixed position on the controller's screen. Enter a row and column position to determine where the upper-left corner of the SX/13a screen is displayed on the controller screen.

Using RS-232-C Remote Commands

The RS-232-C remote commands are divided into three groups:

- **Front panel key commands** — These can perform any function that is usually done by pressing keys on the SX/13a's front panel.
- **Commands not available from the SX/13a keyboard** — These commands perform functions specifically related to remote control and are not available through the SX/13a keypad.
- **Direct function commands that perform a specific function** — The third group of commands provides a more direct method of doing often-used functions that could otherwise be accessed through the front panel key commands, but are quicker to access through these direct functions.

The Remote Control Command Reference section, on page 7-7, includes complete lists of the available commands and corresponding keys for the front panel of the SX/13a and the remote controller.

The basic conventions for the remote commands are:

- RS-232-C remote commands consist of alphanumeric ASCII characters. Each command begins with a one- or two-character mnemonic and ends with a CR (carriage return) terminator. The exceptions are:
  - 0–9
  - Period
  - C
- Uppercase and lowercase letters may be used interchangeably.
- Multiple functions can be entered on the same line by separating them with a space or semi-colon delimiter. The last function must end with a CR terminator.

When entering a multiple-digit number, numeric entry does not need to be terminated individually with a CR or command delimiter. A sequence can be sent to the SX/13a in a string terminated with a single CR. After sending a numeric string to the SX/13a, the parameter can be accepted with a second CR, which is equivalent to pressing **ENTER** on the SX/13a front panel.

NOTE: If the controller does not allow a single CR to be sent, send an "E" mnemonic to the SX/13a. This mnemonic represents the SX/13a ENTER key.

Depending on the command type executed, the SX/13a may or may not return a response string after a command is received. Whether or not a response is generated, the SX/13a returns a prompt when the command execution is complete. To begin a new line, prompts are preceded by CR and LF. The prompts are shown in Table 7.1.

Table 7.1 RS-232-C Command Prompts

Prompt	Description
>	Command received and processed successfully.
?	Syntax error in the received command.
@	Command not available in the current state of the SX/13a.
!	CRC error occurred during a program or configuration download.

During the SX/13a's response to the read current display command (RD), upload configuration command (UC), and upload program command (UP), the X-ON and X-OFF flow control messages are supported. To start or stop transmission, send X-ON or X-OFF messages to the SX/13a during its response. During long transmissions to the SX/13a, such as downloads of configuration settings or simulation programs, X-ON or X-OFF messages may be issued by the SX/13a to control the flow of incoming data.

NOTE: The terminal must be able to accept the X-ON and X-OFF messages to prevent data loss.

Remote Control Command Reference

Table 7.2 SX/13a Front Panel and Remote Controller Keys

SX/13a Front Panel Key	Controller Key(s)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
0	0
.	.
CLR	C
ENTER	E
MENU	M N
<Function 1>	F 1
<Function 2>	F 2
<Function 3>	F 3
<Function 4>	F 4
<Function 5>	F 5
<Function 6>	F 6
<Function 7>	F 7
<Function 8>	F 8
<Function 9>	F 9
↑	C U
↓	C D
←	C L
→	C R
HELP	H P

Table 7.3 Remote Control Commands

Command Syntax	Command Name	Description
!	Interface Clear	Resets the remote control interface and stops commands. A CR is not needed to terminate this command.
ID	Send Identification	Remotely determines the SX/13a firmware revision.
LL	Local Lockout	Remotely disables the SX/13a keyboard.
LO	Local Lockout Off	Remotely re-enables the SX/13a keyboard.
RD	Read Current SX/13a Display	Uploads the current SX/13a display.
RS	Reset	Enables the SX/13a keyboard for local operation. This function re-enables errors if they were disabled and sets the SX/13a data path to Normal, terminating any loopback or bypass modes that may be active. Reset also stops any functions in progress, such as recording error statistics or running programs.

Remote Control Upload Commands

The SX/13a implements four upload commands to save commonly used parameter setups and programs to the remote controller. These files are restored by downloading them to the SX/13a. However, there is no separate download command. Downloads are performed by sending an uploaded file back to the SX/13a exactly as it was received by the controller.

Table 7.4 Remote Control Upload Commands

Command Syntax	Command Name	Description
UC	Upload Configuration	Causes the SX/13a to send its current parameter settings. The returned value is an ASCII file of approximately 270 characters that ends with a carriage return character and contains the current SX/13a parameter settings. To download, send this file back to the SX/13a.
UP	Upload Program	Causes the SX/13a to send the contents of its program memory. The returned value is an ASCII file of approximately 150 characters per program step and ends with a single carriage return character. It contains the current SX/13a program memory contents. To download, send this file back to the SX/13a.
UT	Upload Targeting Parameters	Causes the SX/13a to send its current Error Targeting Option parameter settings. The returned value is an ASCII file of approximately 5,000–13,000 characters and ends with a carriage return character. It contains the current SX/13a Error Targeting Option parameter settings. To download these parameters, send this file back to the SX/13a.
UX	Upload Extended T1/E1 Parameters	Causes the SX/13a to send its current Extended T1/E1 Simulation Option parameter settings. The returned value is an ASCII file of approximately 13,000 characters and ends with a carriage return character. It contains the current SX/13a Extended T1/E1 Simulation Option parameter settings. To download, send this file back to the SX/13a.

Direct Function Remote Commands

Table 7.5 Remote Control Direct Function Syntax Conventions

Syntax	Description
[ ]	Indicates an optional item in a command. To include the item, type only the item within the brackets. Do not include the brackets themselves.
|	Separates mutually exclusive options in a syntax line for a given command.
xx, yy	Represent numeric entries of up to a certain number of digits indicated by the number of x or y characters.

Table 7.6 Remote Control Direct Function Commands

Command	Command Name	Description and Syntax
ANSIOFF	ANSI Off	Turns ANSI screen control mode off. Syntax: ANSIOFF
ANSION	ANSI On	Turns ANSI screen control mode on. Syntax: ANSION
BB	Burst Both	Triggers manual burst errors on the East and West channels. Syntax: BB
BE	Burst East	Triggers manual burst errors on the East channel. Syntax: BE
BW	Burst West	Triggers manual burst errors on the West channel. Syntax: BW
DE	Density East	Enters the East burst density parameter. Syntax: DE[xxEyy][L|B|S|M] Parameters: [L|B|S|M] L: Logic errors B: Bipolar errors S: Space errors (force to 0) M: Mark errors (force to 1) Example: DE26E06L (density East = 2.6e-5 logic errors/bit)
DL	Delay	Enters the delay parameter for one or both channels. Syntax: DL[E|W][xxxx[K|M]][U|S|B|W] Parameters: [E|W] (default is both channels) E: Set delay for East channel only W: Set delay for West channel only [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [U|S|B|W] (default is current units) U: Microseconds S: Milliseconds B: Bytes (available at or below 8.448 MHz) W: Words (available above 8.448 MHz) Examples: DL1000B (delay = 1000 bytes) DL1.2KS (delay = 1200 milliseconds)

Command	Command Name	Description and Syntax
DR	Data Rate	Enters the data rate parameter. Syntax: DR[xxxxxxxx[K|M]] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) Examples: DR100 (data rate = 100 Hz) DR1K (data rate = 1000 Hz) DR1.544M (data rate = 1,544,000 Hz)
DW	Density West	Enters the West burst density parameter. Syntax: DW[xxEyy][L|B|S|M] Parameters: [L|B|S|M] L: Logic errors B: Bipolar errors S: Space errors (force to 0) M: Mark errors (force to 1) Example: DW2E6L (density East = 2e-6 logic errors/bit)
EE	Error East	Enters the East random error parameter. Syntax: EE[xxEyy][L|B] Parameters: [L|B] L: Logic errors B: Bipolar errors Example: EE1E9L (East error rate = 1e-9 logic errors/bit)
EOF	Error Off	Disables the SX/13a error generator. Syntax: EOF
EON	Error On	Enables the SX/13a error generator. Syntax: EON
EW	Error West	Enters the West random error parameter. Syntax: EW[xxEyy][L|B] Parameters: [L|B] L: Logic errors B: Bipolar errors Example: EW35E8L (error West = 3.5e-7 logic errors/bit)

Command	Command Name	Description and Syntax
GE	Gap East	Enters the East burst gap length parameter in milliseconds. Syntax: GE[xxxxxxxx[K|M][F|R]|M] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [F|R] (default is current) F: Fixed length of x R: Random length with x as mean [M] (alternative to x) M: Manual gap Examples: GE12345678F (gap = 12,345,678 milliseconds, fixed length) GE1MR (gap = 1,000,000 milliseconds, random length) GE2KF (gap = 2,000 milliseconds, fixed length) GEM (gap = manual)
GW	Gap West	Enters the West burst gap length parameter in milliseconds. Syntax: GW[xxxxxxxx[K|M][F|R]|M] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [F|R] (default is current) F: Fixed length of x R: Random length with x as mean [M] (alternative to x) M: Manual gap Examples: GW12345678F (gap = 12,345,678 milliseconds, fixed length) GW1MR (gap = 1,000,000 milliseconds, random length) GW2KF (gap = 2,000 milliseconds, fixed length) GWM (gap = manual)
ID	Send	Causes the SX/13a to send its identification and revision number. Syntax: ID Returned value is an ASCII string containing the SX model and software revision; for example, "SX/xx Data Channel Simulator Rev x.xx"

Command	Command Name	Description and Syntax
LE	Length East	Enters the East burst length parameter. Syntax: LE[xxxxxxxx[K|M][B|S]][F|R][/F|/U] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [B|S] (default is current units) B: Bits S: Milliseconds [F|R] (default is current) F: Fixed length of x R: Random length with x as mean [/F|/U] (default is current units) /F: Framed /U: Unframed Examples: LE12345678BF (length East = 12,345,678 bits, fixed length) LE1.4MBR (length East = 1,400,000 bits, random length) LE2.1KSF/F (length East = 2,100 milliseconds, fixed length, framed) LE10SR/U (length East = 10 milliseconds, random length, unframed)
LL	Local Lockout	Disables the SX/13a keyboard. Syntax: LL
LO	Local Lockout Off	Enables the SX/13a keyboard for local operation. Syntax: LO
LW	Length West	Enters the West burst length parameter. Syntax: LW[xxxxxxxx[K|M][B|S]][F|R][/F|/U] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [B|S] (default is current units) B: Bits S: Milliseconds [F|R] (default is current) F: Fixed length of x R: Random length with x as mean [/F|/U] (default is current units) /F: Framed /U: Unframed Examples: LW12345678BF (length West = 12,345,678 bits, fixed length) LW1.4MBR (length West = 1,400,000 bits, random length) LW2.1KSF/F (length West = 2,100 milliseconds, fixed length, framed) LW10SR/U (length West = 10 milliseconds, random length, unframed)
PM	Program Mode	Enters the SX/13a into its programming mode. Syntax: PM
PR	Program Run	Starts the execution of the SX/13a program. Syntax: PR
PS	Program Stop	Stops the SX/13a program execution. Syntax: PS

Command	Command Name	Description and Syntax
PT	Program Step Time Duration	Enters the SX/13a program step time duration parameter. Syntax: PT[xxxxxx[K|M]|[M]] Parameters: [K|M] (default is x) K: Multiply x by 1,000 (add three zeros) M: Multiply x by 1,000,000 (add six zeros) [M] M: Manual step duration Examples: PT1 (1 second step duration time) PT3.6K (3,600 seconds step duration time) PT2M (2,000,000 seconds step duration time) PTM (Manual step duration)
PX	Program Exit	Causes the SX/13a to exit from its programming mode. Syntax: PX
RD	Read Display	Causes the SX/13a to send its current display. Syntax: RD The returned value is an ASCII string containing the eight lines of information displayed on the SX/13a display, plus a ninth line identifying the function keys. When not in ANSI mode, the string begins with a CR, LF sequence, and each line of the display string ends with a CR, LF sequence. In addition, brace characters { } are used to delimit the highlighted or blinking areas of the display when ANSI mode is not enabled. When the ANSI option is enabled, cursor positioning and highlighted or blinking areas of the SX/13a display are displayed using ANSI control commands instead. Example: When the **MAIN** screen is displayed, the returned string might be: **MAIN PARAMETERS: 8.4480MHz** **DELAY / RANDOM ERRORS / BURST LENGTH / GAP LENGTH / BURST DENSITY** **E: 993ms 99E-12 16777kb 99999s 0** **W: off 0 100b manual 0** **[change] [BW] [erroff] [setup]** **F1 F2 F3 F4 F5 F6 F7 F8 F9**
RS	Reset	Resets the SX/13a to its power-on state. This also clears temporary modes, such as "Errors Disabled" and "Program Run." Syntax: RS
UC	Upload Configuration	Causes the SX/13a to send its current parameter settings. Syntax: UC The returned value is an ASCII file of approximately 270 characters and sends with a carriage return character. It contains the current SX/13a parameter settings. To download, send this file back to the SX/13a.

Command	Command Name	Description and Syntax
UP	Upload Configuration	Causes the SX/13a to send the contents of its program memory. Syntax: UP The returned value is an ASCII file of approximately 150 characters per program step and ends with a single carriage return character. It contains the current SX/13a program memory contents. To download, send this file back to the SX/13a.
UT	Upload Targeting Parameters	Causes the SX/13a to send its current Error Targeting Option parameter settings. Syntax: UT The returned value is an ASCII file of approximately 5,000–13,000 characters and ends with a carriage return character. It contains the current SX/13a Error Targeting Option parameter settings. To download these parameters, send this file back to the SX/13a.
UX	Upload Extended T1/E1 Parameters	Causes the SX/13a to send its current Extended T1/E1 Simulation Option parameter settings. Syntax: UX The returned value is an ASCII file of approximately 13,000 characters and ends with a carriage return character. It contains the current SX/13a Extended T1/E1 Simulation Option parameter settings. To download, send this file back to the SX/13a.

Chapter 8. Diagnostics and Troubleshooting for the SX/13a

Contacting Technical Support

Technical support is available Monday through Friday between 07:00 and 18:00 Pacific Standard Time.

To obtain technical support for any product, please contact our Technical Support Department using any of the following methods:

Toll Free:	1-800-SPIRENT (1-800-774-7368) (available in the U.S. and Canada)
Phone:	1-818-676-2300
Fax:	1-818-880-9154
E-mail:	support@spirentcom.com
Web:	http://support.spirentcom.com

In addition, the latest versions of user manuals, application notes, and software and firmware updates are available on our website at:

http://www.spirentcom.com

Company Address
Spirent Communications, Inc.
26750 Agoura Road
Calabasas Hills, CA 91302
USA

Diagnostic Tests Description

The SX/13a features two levels of diagnostic testing. On power-up, the SX/13a runs an internal self-test, which performs an abbreviated check of the internal circuitry and each installed option. The second level of diagnostics includes a set of user-controlled routines that perform detailed internal circuitry tests. The four sets of user-controlled routines are:

- **<test>** — Full Internal Test: Performs a full internal self-test, but does *not* test any interfaces that may be installed. This routine is recommended to functionally test the SX/13a for internal problems.

- **<cust>** — Custom Test: Allows the user to select individual diagnostic routines that are supported by the **<test>** option. Six test routines are listed in the Custom Test menu and any combination of diagnostic routines may be selected from this list. Used to test for problems related to a particular section of the SX/13a.

- **<bert>** — BERT Test: The Bit Error Rate Test (BERT) sends a pseudo-random pattern through the SX/13a and checks the pattern after it has passed through the SX/13a's circuitry. This test is useful as an overall data path test and as an interface test.

- **<cert>** — Certification Test: The certification test requires the presence of a T1 interface and a SONET interface. It performs the diagnostic tests of the **<test>** function and also tests these types of interfaces. This test is used in factory certification testing by Spirent Communications personnel.

Running the Full Internal Tests

The full internal system test includes six diagnostic routines to test the: keyboard, memory, delay, clock generator, error generator, and data path.

There are two test modes:

- In single test mode, the routine stops after completing the entire set of tests.
- In continuous test mode, the test sequence restarts after the last test but omits the keyboard test on all subsequent passes. In this mode, the SX/13a displays the number of times the test sequence has passed. The test sequence restarts from 0 after the system has run the diagnostic 65535 times.

Figure 8.1, on the next page, shows the diagnostics screens hierarchy.

1. Turn on the unit. The installed interfaces and options are listed, then the SETUP screen is displayed.
2. Press MENU.
3. Select **<more>**.
4. Select **<diags>**.
5. From the **SX/13A DIAGNOSTICS (SELF TEST)** screen, select **<single>**.
6. The first of the six routines is a keyboard test. Press each key on the SX/13a's front panel while verifying that the on-screen label for that key is erased when you press the corresponding key. Start with the numeral 1 on the numeric keypad, and press each key in order as it corresponds to the on-screen display. Select **DONE**. This is the last key and initiates the remainder of the tests.
7. The remaining tests complete without intervention.

The entire diagnostics complete in about 20 minutes, if no problems are found. If problems occur, the test number and error message regarding the failure is displayed. The diagnostics can be cancelled by selecting **<esc>**. If no problems are found, the MENU screen is displayed.

NOTE: If the automatic system start up test or the diagnostics test indicates a problem, immediately contact Technical Support for assistance.

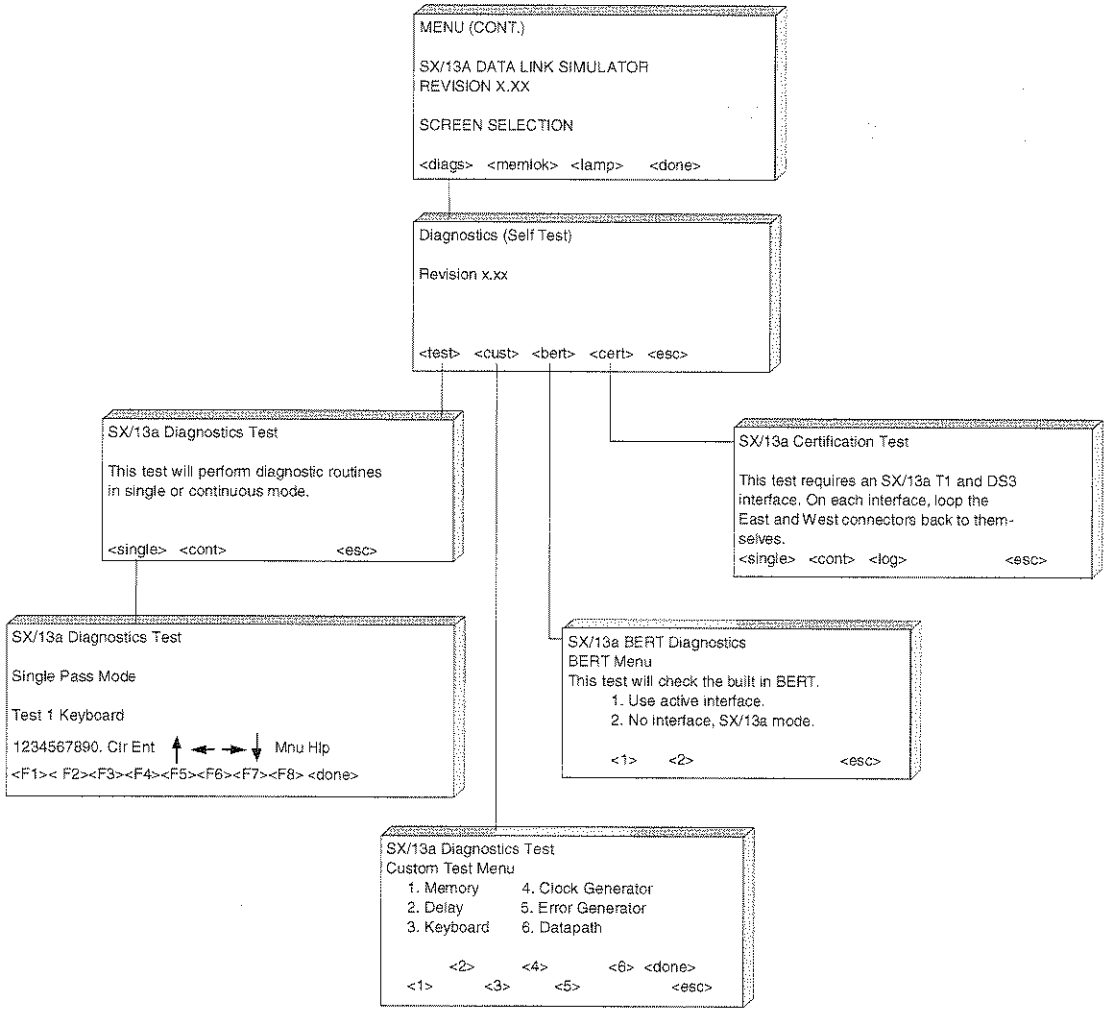

Figure 8.1 Diagnostics Screens

Running Custom Tests

The custom test option can select any of the six diagnostic routines included in the full internal test suite: keyboard, memory, delay, clock generator, error generator and data path.

1. Select **<cust>**.
2. Select which of the test routines to run by pressing the function keys labeled **<1>** through **<6>** in any combination. More than one test may be selected. Select **<done>** to register your choice(s). The test options are:
    1. Memory
    2. Delay
    3. Keyboard
    4. Clock Generator
    5. Error Generator
    6. Datapath
3. Select either Single **<single>** or Continuous **<cont>** test mode.
4. The keyboard test runs first, if it was selected. Press each key on the SX/13a's front panel while verifying that the on-screen legend for that key is erased when you press the corresponding key.

    NOTE: The custom test can be cancelled at any time by pressing ***<esc>****.*
5. Select **<done>** last to begin the next routine in the sequence.

    The remainder of the diagnostic routines run as they would in the full internal test. If no problems are found, the **MAIN** screen is displayed. If problems occur, the test number and error message regarding the failure is displayed.

Running a BERT Test

The bit error rate test (BERT) diagnoses the internal circuitry of the mainframe, or the circuitry of the selected interface. It does this by sending a pseudo-random pattern through the SX/13a and checking the pattern after it has passed through the SX/13a's circuitry. The BERT test runs in one of two modes:

- **Mode 1** — Uses an internal clock to pass a pseudo-random pattern through the internal data path of the SX/13a and checks the resultant data stream coming out of the internal circuitry for errors. No interfaces need be present for this test to run.
- **Mode 2** — Passes data through the internal data path of the SX/13a, out the current active interface module, through an external loopback cable connected to the interface ports, and back to the BERT checker for testing. Prior to starting a test in Mode 2, loopback cables must be connected to each of the East and West interface ports of the active interface.

1. Select **<bert>** to begin the BERT test.
2. Select **<1>** or **<2>**. Mode 1 uses the active interface; mode 2 uses the mainframe, not the active interface and requires a loopback. The **SX/13A BERT DIAGNOSTICS** screen is displayed.
3. There are six available function keys:

   <0's> — Not used. Use **<pttrn>** instead.

   <1's> — Not used. Use **<pttrn>** instead.

   <pttrn> — Sends a pattern of 0s and 1s through the SX/13a circuitry. These should go into synchronization when <sync> is selected and pass through with no errors.

   <sync> — Starts the BERT test. This causes the BERT receiver to begin synchronizing to the pattern.

   <rst> — Clears the error counts. The Error Seconds counts should remain at 0 while the Error-Free Second counts should increment.

   <esc> — Cancels the BERT test.

   This screen also presents the time duration of the BERT test, the Sync Status, an Errored Seconds count and an Error-Free Seconds count for both East and West channels.
4. Select **<sync>** to start the BERT test. To cancel the test, select **<esc>**.

   The Sync Status should display as **SYNC**. If the status **NO SYNC** is displayed or if errors are detected, there is either a setup or functional problem with the SX/13a.

Certification Test

Since the certification test is intended for factory testing of the SX/13a, its operation is not described here. If any error messages are generated or any problems are detected during any of the diagnostic routines, contact Technical Support for assistance in determining a course of corrective action.

Chapter 9. SX/13a Specifications

SX/13a Mainframe Unit Specifications

Physical Specifications

Dimensions: 19" (48.3 cm) wide by 5.25" (13.3 cm) high by 14" (35.56 cm) deep
Weight: 19 lbs.
Program and Parameter Memory: 10-year battery-backup
Flanges: Rack-mountable flanges permanently attached
Rear Panel Ports: Five (5) rear panel ports for interfaces and options; One (1) port for the Remote Control Option, if purchased

Interfaces
SONET 51.84 Mbps (STS-1)
DS3 (T3 44.736 Mbps)
DS1 (T1 1.544 Mbps)
G.703 (E3 34.368 Mbps)
G.703 (E1 2.048 Mbps)
HSSI (up to 51.84 Mbps)
V.35
RS-449 (RS-422-A)
RS-232-C

Error Targeting Options
SX/13a Error Targeting Option
Extended E1/T1 Simulation Option

Remote Control Options
IEEE-488 Remote Control Module
RS-232-C Remote Control Module

Power

Rated Voltage: 110 VAC or 230 VAC
Frequency: 50 Hz or 60 Hz
Rated Input Current: 5 A at 110 V or 3 A at 230 V

The SX/13a can operate using 115 or 230 VAC power sources; the power supply automatically adjusts to the input line voltage.

NOTE: The fuse is pre-set by the factory to the shipping destination's line voltage rating.

External Clock Input

Impedance: 75 ohms
Low-Input Voltage Level: –0.5 to 1.0 V
High-Input Voltage Level: 4.0 to 5.5 V
Maximum Frequency: 52.0 MHz
Duty Cycle: 50% ±5%

Fuse

4 A Slo-Blo® 230 V
5 A Slo-Blo® 110 V

Type of Channel

Channel Type: Full-duplex

Calibration Certification

This certifies that, at the time of manufacture, all SX/13a Data Link Simulators made by Spirent Communications are calibrated in accordance with applicable Spirent Communications procedures. This Spirent Communications equipment is calibrated using national standards, consensus standards, and ratio-type measurements based on self-calibration techniques. By design, the equipment has no user adjustments and does not require further calibration. Products are calibrated within the published environmental specifications for the products. At the time of shipment, this Spirent Communications product met its published operating specifications.

SX/13a Available Products and Part Numbers

The SX/13a uses many components similar to the SX/13 and SX/14. Therefore, the part descriptions in the following table correctly identify the SX/13a components.

Table 9.1 SX/13a Products and Part Numbers

Part Number	Part Description
340-5038-001	SX/13a User Manual
130501	SX/13/14 Hard Carrying Case
130402CE	SX/13/14 RS-232-C Remote Control Interface (CE)
130402	SX/13/14 RS-232-C Remote Control Interface
130401CE	SX/13/14 IEEE-488 Remote Control Interface (CE)
130401	SX/13/14 IEEE-488 Remote Control Interface
130311CE	SX/13/14 RS-232-C Interface Module (CE)
130311	SX/13/14 RS-232-C Interface Module
130308CE	SX/13/14 RS-449 (RS-422-A) Interface Module (CE)
130308	SX/13/14 RS-449 (RS-422-A) Interface Module
130307CE	SX/13/14 V.35 Interface Module (CE)
130307	SX/13/14 V.35 Interface Module
130306A	SX/13/14 SONET STS-1 (51.84 Mbps) Interface Module
130305ACE	SX/13/14 G.703 (E3) (34.368 Mbps) Interface Module (CE)

Part Number	Part Description
130305A	SX/13/14 G.703 (E3) (34.368 Mbps) Interface Module
130304CE	SX/13/14 G.703 (E1) (2.048 Mbps) Interface Module (CE)
130304	SX/13/14 G.703 (E1) (2.048 Mbps) Interface Module
130303ACE	SX/13/14 DS3 (T3) (44.736 Mbps) Interface Module (CE)
130303A	SX/13/14 DS3 (T3) (44.736 Mbps) Interface Module
130302CE	SX/13/14 DS1 (T1) (1.544 Mbps) Interface Module (CE)
130302	SX/13/14 DS1 (T1) (1.544 Mbps) Interface Module
130301CE	SX/13/14 HSSI Interface Module (CE)
130301	SX/13/14 HSSI Interface Module
130202CE	SX/13/14 Extended T1/E1 Simulation Option (CE)
130202	SX/13/14 Extended T1/E1 Simulation Option
130201CE	SX/13 Error Targeting Option (CE)
130201	SX/13 Error Targeting Option
130101ACE	SX/13a Data Channel Simulator Mainf rame (CE)
130101A	SX/13a Data Channel Simulator Mainframe

Warranty Plan

All Spirent Communications SX test systems carry a 1-year warranty.

Warranty Service

For warranty service and repair, the product must be returned to Spirent Communications. The buyer shall prepay all shipping charges required to return the product to Spirent Communications, and Spirent Communications shall pay all shipping charges required to return the product to the buyer. If the product is returned to a destination outside of the United States, the buyer shall pay all shipping charges, duties, and taxes.

Warranty Limitations

Extended Warranty protection does not apply to software, or to damage to hardware resulting from improper or inadequate maintenance by the buyer, unauthorized modification, misuse, buyer-supplied software or interfacing, operation outside of the environmental specifications for the product, or improper site preparation. No other warranty is expressed or implied.

Extended Warranty Plan

All Spirent Communications SX Data Link Simulator components come with a 1-year warranty. The Spirent Extended Warranty Plan allows the purchase of additional years of warranty for a percentage of the Spirent Communications hardware purchase price. The Extended Warranty Plan covers all parts and labor.

For warranty service and repair, the product must be returned to Spirent Communications. The buyer shall prepay all shipping charges required to return the product to Spirent Communications, and Spirent Communications shall pay all shipping charges required to return the product to the buyer. If the product is returned to a destination outside of the United States, the buyer shall pay all shipping charges, duties, and taxes.

Interface Specifications

Table 9.2 Interface Specifications

	SONET (STS-1)	DS3 (T3)	DS1 (T1)	G.703 (E3)	G.703 (E1)	HSSI	RS-422-A	RS-232-C	V.35
Data Rate	51.84 Mbps	44.736 Mbps	1.544 Mbps	34.368 Mbps	2.048 Mbps	51.84 Mbps	10 Mbps	20 kbps	10 Mbps
Connectors	Four BNC connectors: East receive, East transmit, West receive, West transmit	Four BNC connectors: East receive, East transmit, West receive, West transmit	Two bantam jacks: East receive and transmit; West receive and transmit; 15-pin, D-type connectors	Four BNC connectors: East receive, East transmit, West receive, West transmit	Two bantam connectors with East receive, East transmit, West receive, West transmit; two 15-pin, D-type female connectors	Two 50-pin HSSI connectors (AMP 749075-5 or equivalent receptacle) (SCSI-2)	Two 37-pin, D-type female connectors: East is DTE; West may be either DTE or DCE connected	Two 25-pin, D-type connectors: East is DTE; West may be either DTE or DCE connected	Two 34-pin Winchester MRA-34-P-JTC6-H8 female connectors: East is DTE; West may be either DTE or DCE connected
LEDs	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active	Green = power; amber = active
Interfaces with	Network equipment (such as DCS, add-drop MUXs) and CPE	Network equipment (such as DACS and channel banks) and CPE	Network equipment	Network equipment and CPE	Network equipment	DTE	DTE, DCE	DTE, DCE	DTE, DCE
Installation	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage	Place in any one of the five interface slots in the card cage

	SONET (STS-1)	DS3 (T3)	DS1 (T1)	G.703 (E3)	G.703 (E1)	HSSI	RS-422-A	RS-232-C	V.35
Output Amplitude	Transmit cable length selected on Setup STS1 Interface screen, nominal pulses: 0.5 V (225+ ft) or 0.36 V (0–225 ft). East and West channels independ-ently selectable.	Transmit cable length selected on Setup DS3 Interface screen, nominal pulses: 0.77 V (225+ ft) or 0.6 V (0–225 ft). East and West channels independ-ently selectable.	Transmit cable length selected on Setup DS1 Interface screen: Five line build-out for up to 655 feet (2.4 V–3.6 V, 3.0 V nominal pulse)	Transmit cable length selected on Setup E3 Interface screen, nominal pulses: 1.1 V (high) or 0.9 V (low). East and West channels independ-ently selectable.	2.37 V (75-ohm coaxial cable setting), 3.0 V (120-ohm twisted pair setting)	ECL 10 KH signals -0.9 V to -1.75 V with 330 ohms to Vee	Balanced differential +/-5 V peak-to-peak into 100 ohms (maximum)	+/-10 V into 7 K ohms	Clock and data +/-1.10 V peak-to-peak into 100 ohms. Signalling leads +/-10 V into 7 K ohms.
Cabling	75-ohm coaxial with BNC connectors	75-ohm coaxial with BNC connectors	Transmitter complies with ATT CB-199 requirements when using ABAM cable	75-ohm coaxial with BNC connectors	Maximum range is 1,500 feet. Optional adapter cables are the ADP-BNC and the ADP-TWX.	Maximum of 50 feet, 110-ohm twisted-pair with braided shield (SCSI-2 cable)	Less than 200 feet recom-mended	Less than 50 feet recom-mended	Less than 100 feet
Line Coding	B3ZS	B3ZS	AMI or B8ZS	HDB3	HDB3	Balanced Differential	Balanced Differential	Non-Return to Zero	Balanced Differential
Framing	Transparent to STS-1 framing	Transparent to DS3 framing	Transparent to DS1	Transparent to G.704 framing	Transparent to G.704 framing				
Consecutive Zeros Before Loss of Signal (LOS)			160–190 (175 nominal)		160–190 (175 nominal)				

	SONET (STS-1)	DS3 (T3)	DS1 (T1)	G.703 (E3)	G.703 (E1)	HSSI	RS-422-A	RS-232-C	V.35
Receiver Sensitivity	550 mV–1.1 V	550 mV–1.1 V	–10 db below DSX-1	550 mV–1.1 V	–12 dB (1.5 Vpp)	ON signal: Line "+" is more positive than line "-". OFF signal: Line "+" is more negative than line "-".	ON signal: Line A is positive with respect to Line B. OFF signal: Line A is negative with respect to Line B.	OFF signal interchange voltage < -3 V. ON signal interchange voltage > 3 V.	OFF signal interchange voltage < -3 V. ON signal interchange voltage > 3 V. Clock and data: OFF (binary "1"); mark; Line A is nominally -0.55 V with respect to Line B. ON (binary "0"); space is >; Line A is nominally +0.55 V with respect to Line B.
Input Impedance	75 ohms	75 ohms	100 ohms	75 ohms	75 ohms (coaxial cable), 120 ohms (twisted pair)	110 ohms	100 ohms	3 k to 7 k ohms	Clock and data: 100 ohms. Signalling leads: 3 k to 7 k ohms.
Receiver Jitter Tolerance			300 UIs at 10 Hz to 0.4 UIs at 100 kHz		300 UIs at 10 Hz to 0.4 UIs at 100 kHz				
Pulse Shape Compliance	Complies with Bellcore GR-253-CORE	Complies with ANSI T1.102-1993 for DS3		Complies with ITU-T G.703-1991 for 34.368 MHz	Complies with ITU-T G.703 for 2.048 MHz				

	SONET (STS-1)	DS3 (T3)	DS1 (T1)	G.703 (E3)	G.703 (E1)	HSSI	RS-422-A	RS-232-C	V.35
Recover Received Timing	Recovers timing from data received from connected equipment	Recovers timing from data received from connected equipment	Recovers timing from data received from connected equipment	Recovers timing from data received from connected equipment	Recovers timing from data received from connected equipment	N/A	In synchronous DTE-to-DTE, timing is provided by connected equipment. In asynchronous DTE-to-DTE, timing is by sampling. In DTE-to-DCE, the DCE provides TX and RX clocks. In "From DTE and DCE," both types provide their own clocks. In asynchronous DTE-to-DCE, timing is by sampling.	In synchronous DTE-to-DTE, timing is provided by connected equipment. In asynchronous DTE-to-DTE, timing is by sampling. In DTE-to-DCE, the DCE provides TX and RX clocks. In "From DTE and DCE," both types provide their own clocks. In asynchronous DTE-to-DCE, timing is by sampling.	In synchronous DTE-to-DTE, timing is provided by connected equipment. In asynchronous DTE-to-DTE, timing is by sampling. In DTE-to-DCE, the DCE provides TX and RX clocks. In "From DTE and DCE," both types provide their own clocks. In asynchronous DTE-to-DCE, timing is by sampling.
Internal	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer or fixed-frequency crystal oscillator on the interface	SX/13a internal clock synthesizer: available with loop timing off or on	SX/13a internal clock synthesizer: available with loop timing off or on	SX/13a internal clock synthesizer: available with loop timing off or on

	SONET (STS-1)	DS3 (T3)	DS1 (T1)	G.703 (E3)	G.703 (E1)	HSSI	RS-422-A	RS-232-C	V.35
External	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms)	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms): available with loop timing off or on	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms): available with loop timing off or on	Clock source is connected via the External Clock Input BNC connector (TTL, 75 ohms): available with loop timing off or on
Error Type	Logic or BPV	Logic or BPV	Logic or BPV (Select on Change Random Errors screen)	Logic or BPV	Logic or BPV	Logic	Logic	Logic	Logic
BPV Error Types	BPV insertion, pulse reversal, B8ZS disable, wrong substitution	BPV insertion, pulse reversal, B3ZS disable, wrong substitution	BPV insertion, pulse reversal, B8ZS disable (Select on Setup DS1 Interface screen)	BPV insertion, pulse reversal, HDB3 disable, wrong substitution	BPV insertion, pulse reversal, HDB3 disable, wrong substitution	N/A	N/A	N/A	N/A
Burst Density Types	Logic, BPV, space, mark	Logic, BPV, space, mark	Logic, BPV, space, mark	Logic, BPV, space, mark	Logic, BPV, space, mark	Logic, BPV, space, mark	Logic, space, mark	Logic, space, mark	Logic, space, mark

Appendix A. Abbreviations

ABAM
insulated twisted pair wiring that is 22 gauge, 110 ohms

AMI
Alternate Mark Inversion

ANSI
American National Standards Institute: a U.S. standards body

ARQ
automatic request

B3ZS
Bipolar 3 Zero Substitution

B8ZS
Bipolar 8 Zero Substitution

BB
Burst Both

BE
Burst East

BER
Bit Error Rate

BERT
Bit Error Rate Test

BW
Burst West

BPV
bipolar violation

CCITT
Comité Consultatif International Télégraphique et Téléphonique
(Consultative Committee for International Telegraph and Telephone);
now known as ITU-T

CEPT
Conference des Administrations Europeenes des Postes et Telecommunications
(European Conference of Postal and Telecommunications Adminstrations)

CPE
Customer Premises Equipment

CRC
Cyclic Redundancy Check

CTS
Clear To Send

CS
clear to send

CSU
Channel Service Unit

DM
Data Mode

dB
decibels

DCE
Data Communication Equipment

DS-0
digital signal, level 0

DS-1
digital signal, level 1

DS-3
digital signal, level 3

DSU
Data Service Unit

DTE
Data Terminal Equipment

DUT
Device Under Test

E
East (as in the East channel)

E1
Also known as CEPT1, the 2.048 Mbps rate used by European CEPT carrier to transmit 30 64 kbps digital channels for voice or data calls, plus a 64 kbps signal ling channel, and a 64 kbps channel for framing and maintenance

E3
Also known as CEPT3, the 34.368 Mbps rate used by European CEPT carrier to transmit 16 CEPT1s plus overhead

EIA
Electronic Industries Association

EMI
electromagnetic interference

ESF
extended superframe

FIFO
First In, First Out

G.703
ITU-T Recommendation G.703, Physical/Electrical Characteristics of Hierarchical Digital Interfaces

G.704
ITU-T Recommendation G.704, Synchronous Frame Structures Used at Primary and Secondary Hierarchy Levels

HDB3
High-Density Bipolar 3 (zeros)

HSSI
High-Speed Serial Interface

Hz
hertz

IC
Incoming Call

IEEE
Institute of Electrical and Electronics Engineers; a worldwide engineering publishing and standards-making body for the electronics industry

IEEE 802.3
A local area network protocol suite commonly known as Ethernet. Ethernet has either a 10 Mbps or 100 Mbps throughput and uses a carrier-sense multiple-access bus with collision detection CSMA/CD. This method allows users to share the network cable. However, only one station can use the cable at a time. A variety of physical medium-dependent protocols are supported.

IS
In Service

ISDN
Integrated Services Digital Network

ITU-T
International Telecommunications Union Telecommunications; previously CCITT

kbps
kilobits per second

LL
Local Loopback

LAN
Local Area Network

LANE
LAN Emulation

LCD
Liquid Crystal Display

LED
Light Emitting Diode

Mbps
megabits per second

MHz
megahertz

ms
milliseconds

NS
New Signal

OC-n
optical carrier level "n" (where "n" is an integer)

RD
Receive Data

RR
Receiver Ready

RTS
Request To Send

Rx or RX
receive

SB
standby indicator

SC
Send Common

SD
Send Data

SES
Severely Errored Seconds

SF
superframe
signal frequency

SG
Signal Ground

SI
signalling rate indicator

SONET
synchronous optical network

SQ
Signal Quality

ST
Send Timing

STS-n
Synchronous Transport Signal "n" (where "n" is an integer)

TM
Test Mode

TR
Terminal Ready

TT
Terminal Timing

TTL
Transistor to Transistor Logic

Tx or TX
transmit

UC
Upload Configuration

µs
microseconds

UT
upload targeting parameter

UX
upload extended T1/E1 parameters

VAC
Volts Alternating Current

W
West (as in the West channel)

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