INSTRUCTION MANUAL
MODEL 5000
PHASE STANDARD

1,2500 JJ

(212) 255-2940

clarke-hess

COMMUNICATION RESEARCH CORP.

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DIAGRAMS

7-1 INTRODUCTION

WARRANTY

All CLARKE-HESS instruments are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery of the instruments. The CLARKE-HESS Communication Research Corp. will repair or replace instruments that prove to be defective during the warranty period. For such repair or replacement the instrument must be returned to CLARKE-HESS and, in our opinion, the instrument must not have been subjected to unreasonable usage or to internal reworking. No other warranty is expressed or implied.

CLARKE-HESS assumes no liability for secondary damages or charges.

PHASE ANGLE

Range: 0.000° to ±999.999°

Resolution: 0.001° from 1Hz to 100kHz

Accuracy:

1Hz-1kHz	1kHz-6.25kHz	6.25kHz-50kHz	50kHz-100kHz
±(4.9 + 0.1R)m°	±(9 + R)m°	±(24 + R)m°	±(48 + 2R m°

R is the ratio of the larger Output Voltage to the smaller Output Voltage.
The phase accuracy is specified for Output Voltages between 0.25V and 100V after the Standard has been AUTOZEROED with the device under test in place.

OUTPUT FREQUENCY

Range: 1Hz to 100kHz

Resolution: 1Hz from 1Hz to 6250Hz
10Hz from 6250Hz to 50kHz
20Hz from 50kHz to 100kHz

Accuracy: Better than ±150 parts per million.

OUTPUT AMPLITUDE

Range: 100mV rms to 100V rms

Resolution: 2mV from 100mV to 7.098V
25mV from 7.1V to 100V

Accuracy:

1 Hz to 50 kHz
Better than ±5mV from 250mV to 1V.
Better than ±0.5% of setting from 1V to 100V.

50 kHz to 100 kHz
Better than ±25mV from 250mV to 1V.
Better than ±2.5% of setting from 1V to 100V.

TOTAL HARMONIC DISTORTION

Amplitudes between 0.5V and 100 V
Less than 0.02% (-74dB) from 1Hz to 500Hz
Less than 0.05% (-66dB) from 500Hz to 1000Hz
Less than 0.15% (-56dB) from 1000Hz to 50kHz
Less than 0.50% (-46dB) from 50kHz to 100kHz

NOISE

Less than 0.1mV from dc to 100kHz
Less than 0.05mV from 100kHz to 10MHz

OUTPUT DC OFFSET

Less than 0.5% of the ac Output

OUTPUT CURRENT CAPABILITY

3mA minimum

OUTPUT IMPEDANCE

Less than 5 ohms from 1Hz to 50kHz

IEEE-488 1978 SUBSETS

SH1,AH1,T6,L4,SR1,RL1,PP0,DC1,DT0

WARMUP TIME

Less than 10 minutes for all Specifications

TEMPERATURE RANGE

Operating: 23°C ±5°C
Storage: -40°C to 75°C

RELATIVE HUMIDITY

Operating: Less than 60%
Storage: Less than 95%

LINE VOLTAGE, FREQUENCY AND POWER CONSUMPTION

100V ±10%, 120V ±10%, 220V ±10%, 240v ±10%.
Rear panel switch selectable
50Hz or 60 Hz. 3/4 MDL Fuse for 120 V operation
Power Consumption less than 60W.
Volt Amperes less than 75 VA

PHYSICAL

Rack or bench mount
Weight: 24 pounds / 11 kilograms
Size: 19" x 7" x 15" / 48.3 x 17.8 x 38.1 cm

I-1 INTRODUCTION

In this section an overview of the properties of the Model 5000 Phase Standard is first presented. This is followed by a more detailed look at the various controls and features available to the operator. Finally a step by step set of operating instructions is presented.

I-2 GENERAL DESCRIPTION

The Model 5000 Phase Standard is a precision calibration instrument which produces two digitally synthesized low distortion sine waves over a frequency range of 1Hz to 100kHz and with independently selectable amplitudes from 100mV to 100V. The phase angle between the two sinewaves is selectable over a range extending between -999.999° and 999.999° with a resolution of 1m°. A fixed OFFSET, with the same range as the PHASE is also selectable.

Function selection is made via front panel key switches and is displayed on a vacuum fluorescent display having 32, large (0.45"), bright dot matrix characters. The current values of PHASE, FREQUENCY, REFERENCE AMPLITUDE and VARIABLE AMPLITUDE are displayed at all times in the normal operation mode. STANDBY and OPERATE modes, which allow the output sinewaves to be reduced to zero and then restored to their previous values, are also selectable via key switches.

A special key switch matrix simplifies data entry by allowing the operator to increment any digit of the current values of PHASE, FREQUENCY, REFERENCE AMPLITUDE or VARIABLE AMPLITUDE with a single key stroke. A RESET key switch allows the operator to quickly restore the initial settings of the standard.

The Model 5000 has as a standard feature the IEEE-488 interface which is accessible from the rear panel. Any function which can be entered manually can be programmed and sent to the Phase Standard over the IEEE bus. A REMOTE lamp on the front panel indicates when the standard is being controlled by the IEEE bus. When this lamp is illuminated data entry via the front panel is impossible; however, a LOCAL key switch is provided which allows the operator to regain local control.

The Phase Standard is designed to operate with line voltages of 100V, 120V, 220V and 240V at frequencies of 50Hz or 60Hz. A switch in the line cord receptacle on the the rear panel permits the voltage selection. This receptacle also contains a line filter which restricts the passage of high frequency signals both from the Standard to the line and from the line to the Standard.

The Phase Standard is contained in a 19" wide, 7" high and 17" deep (including rack handles) and may be used on the bench or mounted in a standard relay rack.

1-3 SPECIFICATIONS

The detailed specifications for the Model 5000 are included in the table preceding this section.

1-4 CONTROLS AND TERMINALS

This Sub Section describes in reasonable detail the function and properties of the various front and rear panel controls and terminals. The user of the Model 5000 Phase Standard should familiarize himself thoroughly with this material before attempting to operate the instrument.

Figure 1-4-1 illustrates the front panel controls while Fig. 1-4-2 illustrates the rear panel controls. Each control will be discussed in numerical sequence.

1 POWER SWITCH

Depressing this switch applies line power to the Phase Standard and initiates the internal system SELF TEST routines which last approximately 15 seconds. Upon completion of the SELF TEST the Phase Standard is set to its initial values of:

PHASE	= 060.00°
OFFSET	= 000.000°
FREQUENCY	= 500Hz
REFERENCE AMPLITUDE	= 1.000V
VARIABLE AMPLITUDE	= 1.000V

The Phase Standard is also placed in its STANDBY mode which is indicated by the flashing of the R (REFERENCE) and the V (VARIABLE) on the display.

2 REFERENCE OUTPUT

A BNC connector supplies the REFERENCE sinewave output. Signal levels range from 100mV to 100V rms. Currents up to 3mA can be supplied at any voltage level without any degradation of the specifications.

3 VARIABLE OUTPUT

A BNC connector supplies the VARIABLE sinewave output. Signal levels range from 100mV to 100Vrms. Currents up to 3mA can be supplied at any voltage level without any degradation of the specifications.

4 RESET KEY SWITCH

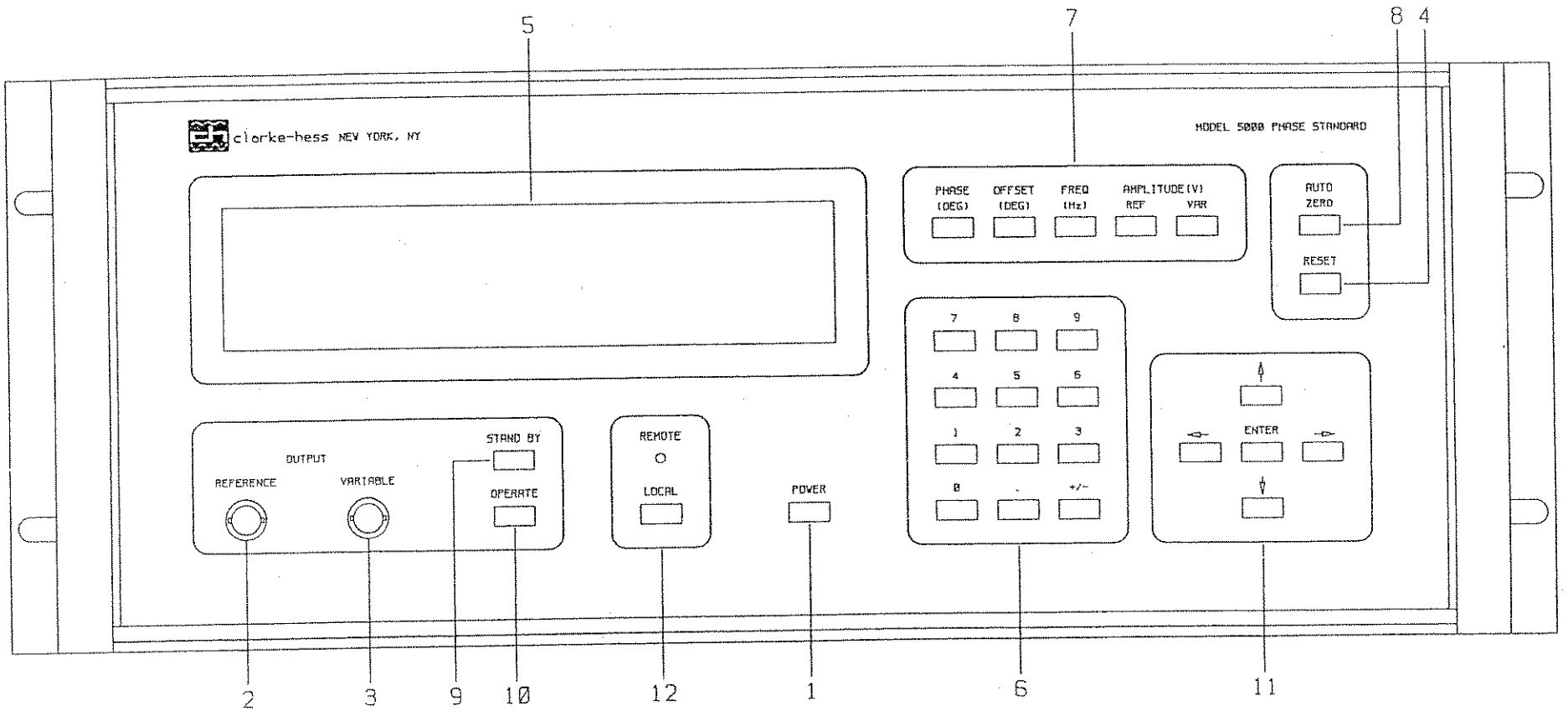
The RESET key switch provides a hardware reset for the system microprocessor. Depressing it results in a complete system initialization. It does not, however, provide a hardware reset for the IEEE interface. If this should be required the POWER should be turned off for 10 seconds and then back on again.

5 DISPLAY

The 32 character, vacuum fluorescent, dot matrix display provides a continuous

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET OF



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	

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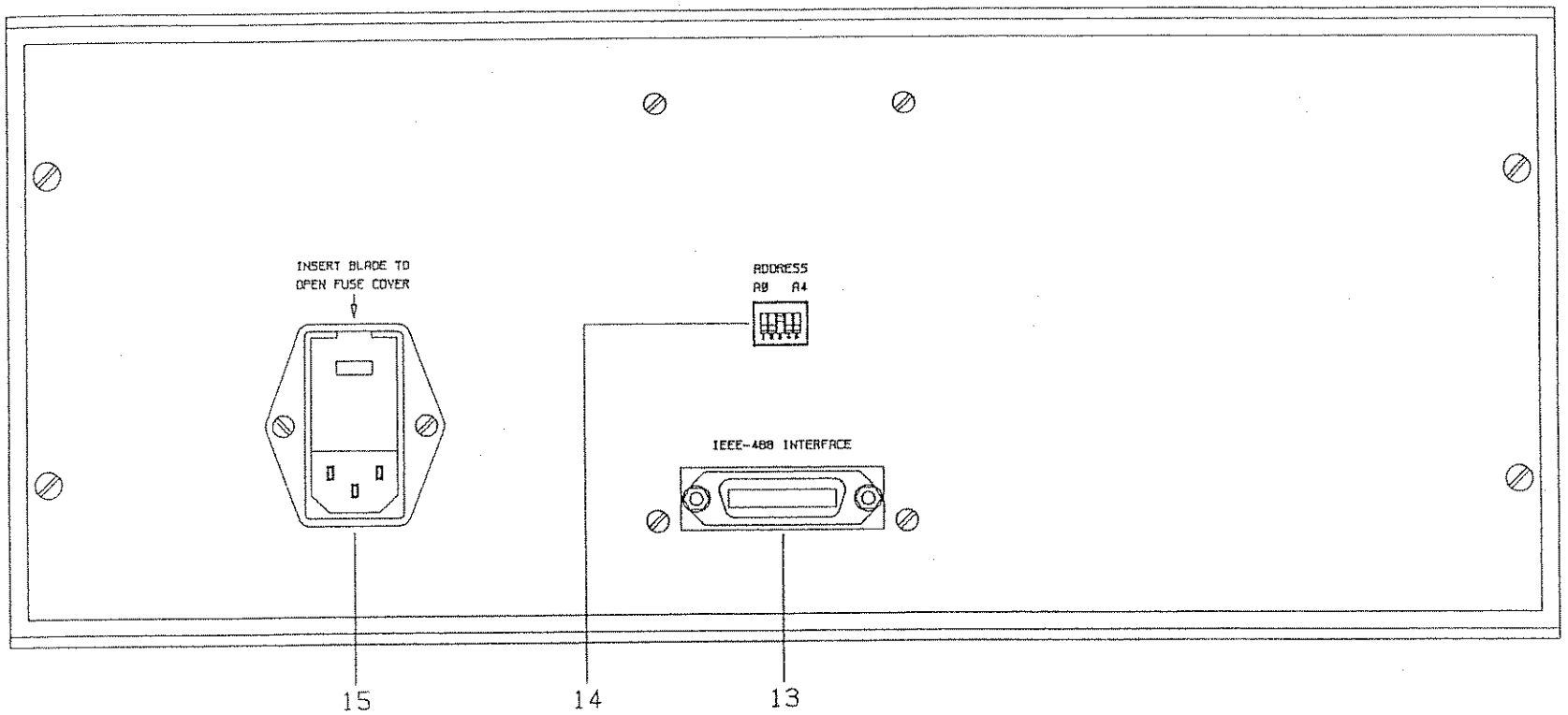
FIGURE 1-4-1
FRONT PANEL CONTROLS

SIZE	CODE IDENT NO.	DRAWING NO.
C		

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE | SHEET OF



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

CONTRACT NO.

APPROVALS	DATE
DRAWN	
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FIGURE 1-4-2
REAR PANEL CONTROLS

SIZE C | CODE IDENT NO. | DRAWING NO.

indication of the PHASE, FREQUENCY and AMPLITUDE (REFERENCE and VARIABLE) which have been set into the Phase Standard. The normal format for these data takes the form

P 060.000° R1.000V
F 500.Hz V1.000V

where the values shown are those following initialization. The P stands for PHASE, the F stands for FREQUENCY and the R and the V stand for REFERENCE and VARIABLE AMPLITUDE respectively. As will be discussed, the format changes when data are entered, when the instrument is AUTOZEROING and when error or calibration messages are presented. The underlined R and V are flashing to indicate that the Standard is in its STAND BY mode (see 9 and 10 below).

6 NUMERIC KEYPAD

This panel on the Phase Standard faceplate functions as a normal calculator keypad. It is employed to assign new numerical values to the various functions when the corresponding entry mode has been selected (see 7 below). If a key on this pad is pressed prior to entering a function entry mode, or at the wrong time while in the mode (e.g., a second decimal point within a single entry), the Standard "beeps" to indicate an attempted incorrect entry.

7 FUNCTION ENTRY PANEL

This panel on the Phase Standard faceplate comprises six key switches which are employed to enter one of the five input modes. Once a mode is entered the numeric keypad permits the user to assign a new value to the function. If at any point during the numeric data entry an error is made, depressing the same function switch clears the incorrect data from the display. If the user decides he does not wish to change the value of the function after he has begun the numeric entry, pressing the ENTER key switch causes the Model 5000 to exit the input mode without affecting any function settings.

Each input mode is now considered in detail.

PHASE: Depressing this key switch causes the Phase Standard to enter the PHASE input mode which is indicated by the following display format.

PHASE 060.000°
OFFSET 000.000°

The line under PHASE indicates that it is flashing and ready to accept numeric PHASE data. In addition to PHASE, any OFFSET which had been set into the instrument is also shown. When the first digit from the numeric keypad is entered, the PHASE stops flashing, the previous phase information disappears, and the digit entered appears in the next to the last position on the top line of the display followed by a flashing cursor in the last position. The cursor indicates the position of the next digit to be entered. When the complete entry is made, the new PHASE is rounded to the nearest 1.37m° and entered asynchronously into the Phase Standard. The display returns to its normal format with the new PHASE value which was entered. At the point where the Standard changes its PHASE internally, the REFERENCE OUTPUT remains continuous; however the VARIABLE OUTPUT jumps to its new value. This can occur anywhere within a cycle.

The PHASE, in degrees, should be entered as a minus sign (the +/- key switch if required), one, two or three digits, a decimal point, and an additional three

digits. No additional keystrokes are required to have the data accepted. If the operator enters three digits initially, he need not, but may, enter the decimal point since the Model 5000 will automatically position it.

OFFSET: Depressing this key switch causes the Phase Standard to enter the OFFSET input mode which is indicated by the following display format.

PHASE 060.000°
OFFSET 000.000°

When the first digit from the numeric keypad is entered, the OFFSET stops flashing, the previous OFFSET information disappears, and the digit entered appears in the next to the last position on the bottom line of the display followed by a flashing cursor in the last position. The cursor indicates the position of the next digit to be entered. When the complete entry is made, the new OFFSET is rounded to the nearest 1.37m° and entered into the Phase Standard. The display returns to its normal format with the new OFFSET value which was entered. All other properties and data entry procedures of the OFFSET input mode are identical with those of the PHASE input mode.

FREQUENCY: Depressing this key switch causes the Phase Standard to enter the FREQUENCY input mode which is indicated by the following display format.

PHASE 060.000°
FREQ 500.Hz

When the first digit from the numeric keypad is entered, the FREQ stops flashing, the previous FREQUENCY information disappears, and the digit entered appears in the next to the last position on the bottom line of the display followed by a flashing cursor in the last position. The cursor indicates the position of the next digit to be entered. When the complete entry is made, the FREQUENCY is rounded to the nearest permissible value and entered asynchronously into the Phase Standard. The display returns to its normal format with the new rounded FREQUENCY value. For FREQUENCY values from 1Hz to 6250Hz no rounding is performed. For FREQUENCY values above 6250Hz to 50000Hz the entry is rounded to the nearest 10Hz. For FREQUENCY values above 50000Hz the entry is rounded to the nearest 20 Hz.

Whenever a FREQUENCY entry is made which passes through 1000Hz in either direction, the Phase Standard automatically performs an AUTOZERO operation (see 8 below). Automatic AUTOZEROING also occurs for all FREQUENCY entries above 6250Hz.

When the Standard updates the FREQUENCY it does so by controlling the internal frequency synthesizer. This results in a frequency transient which has a duration in the order of 50msec in the worst case. During this transient both OUTPUT signals exist with uncertain frequency.

The FREQUENCY, in Hertz, should be entered as one, two, three, four or five digits followed by a decimal point. No additional keystrokes are required to enter the FREQUENCY. If the fifth digit is entered the Phase Standard automatically supplies the decimal point. In the FREQUENCY input mode two special cases are of interest. First if 0.Hz is entered the Standard changes the entry to 1.Hz. Second, if the operator desires a FREQUENCY of 100000Hz he must enter 99999.Hz (a permissible 5 digit entry). The Standard rounds the entry to 100000.Hz.

REFERENCE AMPLITUDE: Depressing this key switch causes the Phase Standard to enter the REFERENCE input mode which is indicated by the following display format.

REFERENCE 1.000V
VARIABLE 1.000V

When the first digit from the numeric keypad is entered, the REFERENCE stops flashing, the previous REFERENCE information disappears, and the digit entered appears in the next to the last position of the top line followed by a flashing cursor in the last position. The cursor indicates the position of the next digit to be entered. When the complete entry is made the REFERENCE AMPLITUDE is rounded to the nearest permissible value and entered into the Phase Standard. At this point both the REFERENCE and VARIABLE OUTPUT drop asynchronously to zero for 10msec to allow the various amplitude setting relays to settle. They then return asynchronously to the updated values. The display returns to its normal format with the new rounded REFERENCE AMPLITUDE displayed as the closest four digit value after an AUTOZERO operation is performed (see 8 below). For REFERENCE AMPLITUDE values between 100mV and 7.100V the entry is rounded to the nearest 1.7mV. For REFERENCE AMPLITUDE values above 7.100V up to 100V the entry is rounded to the nearest 25mV.

The REFERENCE AMPLITUDE, in Volts, is entered as four digits plus a decimal point in the appropriate position. No additional keystrokes are required to enter the REFERENCE AMPLITUDE value. In cases where the position of the decimal point is without question, the Phase Standard will position it automatically. For example if a 5 and a 4 have been entered as the first two digits, the Standard will insert a decimal point since a reading of 540V is not permitted. If a decimal point is entered first the Standard accepts the entry after the next three digits have been entered.

VARIABLE AMPLITUDE: This input mode is the same as that for REFERENCE AMPLITUDE.

8 AUTOZERO KEY SWITCH

The AUTOZERO key switch activates the AUTOZERO function of the Phase Standard provided that the Standard is not in its STAND BY mode (see 10 below). This function automatically sets the two output signals to be in quadrature, measures the angle between them and adds a correction to the VARIABLE OUTPUT signal so that the difference between the signals is exactly 90° The correction value is stored internally within the Standard and is applied to correct for any PHASE error at the selected operating FREQUENCY. If the selected FREQUENCY is above 6125Hz the AUTOZERO is performed at the selected FREQUENCY and the correction is applied directly, otherwise it is performed at 5000Hz and the correction value is scaled by the ratio of the operating FREQUENCY to 5000Hz.

During the AUTOZERO function the display format takes the form.

* * * *
AUTOZEROING

No other function with the exception of RESET is possible until the display returns to its normal format. The AUTOZERO function, in general, is completed in well under two seconds. If for some reason the Phase Standard is unable to AUTOZERO after 15 attempts, the Standard beeps and the display takes the form

NOT
AUTOZEROED

It is generally advisable to press the AUTOZERO key at this point to complete the AUTOZEROING; however the Standard will respond to any additional entries in its usual fashion and AUTOZERO again after the first complete entry.

The AUTOZERO function is performed automatically by the Phase Standard any time a different REFERENCE or VARIABLE AMPLITUDE is entered into the Standard or any time a FREQUENCY which passes through 1000Hz or is above 6250Hz is entered. Manual AUTOZEROING is required when the Standard is operated for long periods of time (more than 30 minutes) without activating the automatic AUTOZERO function. Manual AUTOZEROING is also recommended 30 seconds after a major change in AMPLITUDE or FREQUENCY is made. Although the Standard will be within specification immediately following the change, small thermal errors can be greatly reduced by the second AUTOZEROING.

The sensors for the AUTOZERO circuits are placed directly across the OUTPUT terminals so that any phase error introduced by the connection of external cabling is also corrected. Therefore the device requiring the OUTPUT signals from the Standard must be connected to the Standard prior to either a manual or an automatic AUTOZERO operation.

The internal limit for successful AUTOZEROING is ±1.37m°; hence it is possible, on successive AUTOZERO attempts, to have the output phase angle vary by this amount.

9 STAND BY KEY SWITCH

Depressing the STAND BY key switch reduces both the REFERENCE and the VARIABLE OUTPUT signals to zero without affecting the output impedance of either OUTPUT or affecting the internal settings of the Standard. When the STAND BY mode is entered, both the R and the V in the normal display mode flash to indicate that no OUTPUT exists. This feature should be employed whenever output cables must be changed during a high voltage set of measurements. When the Standard is in the STAND BY mode function values may be changed; however the Standard will not AUTOZERO until the output signals have been restored. The STAND BY mode is entered automatically whenever the Standard is initialized and whenever either output voltage is switched from a value below 20V to a value above 20V.

10 OPERATE KEY SWITCH

Depressing the OPERATE key switch restores normal operation after the Standard has been placed in its STAND BY mode. If a new AMPLITUDE has been entered or a FREQUENCY which normally requires AUTOZEROING has been entered while in the STAND BY mode, the Standard automatically AUTOZEROs when the OPERATE key is pressed.

11 INCREMENT KEY PAD

The INCREMENT KEY PAD permits the operator to increment PHASE, FREQUENCY, REFERENCE or VARIABLE AMPLITUDE data entries without going through the normal function entry procedure. When any of the four ARROW keys are pressed, a flashing cursor appears at its last required position in one of the numeric fields of the normal display mode. The first time an ARROW key is pressed after the Standard is turned on, the flashing cursor appears in the least significant PHASE position. If the LEFT ARROW or the RIGHT ARROW is now pressed,

the cursor moves in the corresponding direction through the numeric field in which it lies. If the flashing cursor is in the least significant position of a particular field, pressing the RIGHT ARROW key causes the cursor to jump to the least significant position of the next numeric field in the sequence PHASE, FREQUENCY, REFERENCE AMPLITUDE, VARIABLE AMPLITUDE and back to PHASE. If the flashing cursor is in the most significant position of a particular field, pressing the LEFT ARROW key causes the cursor to jump to the least significant position of the previous field in the above sequence.

With the flashing cursor in any position, if the UP ARROW is depressed, the digit the cursor is superimposing is increased by 1 with a carry to the next digit if required. If the DOWN ARROW is depressed, the digit the cursor is superimposing is decreased by 1 with a borrow from the previous digit if required. When any digit is incremented the new value is immediately entered into the Phase Standard within the constraints of the normal input rounding. Automatic AUTOZEROING occurs in the same fashion it would with normal entries.

The rounding of the entry does not always permit a digit to be increased or decreased by one. In such cases the Phase Standard jumps to the next permissible value. For example, if the least significant FREQUENCY digit is incremented with the FREQUENCY above 6250Hz, both the display and the output frequency jump by 10Hz in the same fashion they would if the next most significant digit were incremented.

Depressing the ENTER key switch allows the operator to exit the increment mode. This results in the cursor becoming invisible without changing any of the existing values.

12 REMOTE INDICATOR/LOCAL KEY SWITCH

The REMOTE lamp, indicates when the Phase Standard is being controlled by the IEEE-488 interface. When it is illuminated, no manual data entry is possible via the front panel; however all remote data entries and the current settings of PHASE, FREQUENCY and AMPLITUDE are shown on the Display. Depressing the LOCAL key switch (provided that the interface has not placed the Standard in the Local Lockout state) allows the operator to restore the standard to its LOCAL state where normal data entry is possible.

13 IEEE-488 INTERFACE CONNECTOR

This rear panel connector is the standard IEEE-488 connector which mates with the standard, stackable cable connectors which permit parallel bus connections. To avoid possible mechanical damage it is recommended that no more than three connectors be stacked on any one instrument.

14 INTERFACE ADDRESS SWITCH

This switch is set by the operator to be the address to which the instrument responds when under control of the IEEE-488 interface. The address may be set on the switch, which is binary weighted, to have any value between 0 and 30. The Phase Standard is set at the factory with an address of 4 as shown in Fig. 1-4-2. If a change in switch setting is made by the operator, the POWER switch must be turned off for 10 seconds and then back on again to enter the new address into the Standard.

15 POWER RECEPTACLE

The POWER RECEPTACLE accepts the input line cord, provides a fuse for the high voltage line, includes the switch for selecting the various input voltages, and incorporates a line filter for minimizing the interference from the Phase Standard back to the line. Both the line fuse and the line voltage selection switch may be reached by opening the back cover of the receptacle. This is best accomplished by inserting the blade of a screwdriver in the opening at the top and then gently twisting the blade. With the back cover open, the fuse may be reached (and replaced if necessary with a 3/4A MDL fuse) by pulling out the fuse cradle which is marked with a white arrow. This cradle should be replaced with the arrow in the same direction as the arrow on the inside of the back cover.

With the back cover open, the line voltage may be selected by removing the switch drum, rotating it so that the desired line voltage will show through the small window in the back cover, and then replacing it. The cover should then be closed and snapped in place.

NOTE

Any attempt to rotate the switch drum without first removing it will result in damage to the switch contacts.

1-5 INSTALLATION

The Model 5000 Phase Standard is shipped ready for either bench or rack operation. Before applying power to the Standard for the first time, the operator should check that his correct line voltage appears through the window of the POWER RECEPTACLE (see 15 in the previous section). If it does not, the switch should be changed as described above.

1-6 OPERATING INSTRUCTIONS

In this sub section the step by step procedure for supplying a device under test (DUT) the following parameters is considered.

PHASE:	-455.632°
OFFSET:	0.000°
FREQUENCY:	7016Hz
REFERENCE AMPLITUDE:	10.00V
VARIABLE AMPLITUDE:	50.00V

As a basis for this procedure, it is assumed that Sub section 1-4 has been read and understood.

To activate the Model 5000, the POWER switch should be depressed. This causes the Standard to run through its initialization and check out procedures during which the display indicates

* MODEL 5000 *
SELF TEST

The SELF TEST takes approximately 15 seconds and finally ends with the following set of parameters set into the Standard.

PHASE: 60.000°
OFFSET: 0.000°
FREQUENCY: 500Hz
REFERENCE AMPLITUDE: 1.000V
VARIABLE AMPLITUDE: 1.000V

With these parameters the normal display format takes the form

P 060.000° R1.000V
F 500Hz V1.000V

The R and V are flashing to indicate that the Standard is in its STAND BY mode.

At this point the device under test should be connected via equal length cables to the two OUTPUT terminals of the Standard. This is important because the AUTOZERO operation, which will automatically occur after the AMPLITUDE data has been entered and the OPERATE switch pressed, compensates not only for the internal phase inequalities of the two channels of the Standard but also for the phase errors introduced by loading the output terminals of the Standard.

To enter the new PHASE data press the following keys in sequence.

PHASE +/- 4 5 5 6 3 2

Since no OFFSET is required no entry has to be made. To be sure, however, that the existing OFFSET is indeed zero, press the OFFSET key to display the OFFSET and then, if the value is correct, press the ENTER key to restore the normal display format.

To enter the new FREQUENCY data press the following keys in sequence.

FREQ 7 0 1 6 .

When the decimal point is entered the Display returns from its FREQUENCY input to its normal format which now takes the following form.

P-455.632° R1.000V
F 7020Hz V1.000V

Note that the FREQUENCY has been rounded to the nearest 10Hz. To enter the REFERENCE and VARIABLE AMPLITUDE data press the following keys in sequence.

REF 1 0 . 0 0 VAR 5 0 0 0

Note that a decimal point must be placed after the first zero in the REFERENCE entry to ensure 10 and not 100 is entered. After the first zero in the VARIABLE data is entered however, the Standard automatically places the decimal since an entry of 500 is not possible. After the complete entry the Display returns to its normal format which has the following form.

P-455.632° R10.00V
F 7020Hz V50.00V

After these values are checked for accuracy press the OPERATE key. The Standard now enters its AUTOZERO mode which is indicated on the Display. While in this mode the REFERENCE and the VARIABLE OUTPUT signals shift to the AUTOZERO frequency where the VARIABLE signal switches its phase between 90° and 270° several times. The signal AMPLITUDES remain at 10.00V and 50.00V respectively. In most cases this switching should have no effect on the DUT other than, perhaps, slightly increasing its settling time. When the Display has returned to its normal format the required measurement can be made.

1-6 REMOTE OPERATION

This Sub Section is intended for the person who has a good working knowledge of the IEEE-488 interface and the associated controller programming and

needs only a knowledge of the device dependent functions to get started using the Phase Standard remotely. If the material in this sub section is not sufficiently detailed for the reader, he should first read Section V where the interface is considered more thoroughly.

1-6-1 INTERFACE FUNCTIONS

The following tabulation lists the level to which each of the IEEE-488 interface functions are implemented in the Phase Standard.

SH1 Source Handshake Complete capability.

AH1 Acceptor Handshake Complete capability.

T6 Talker Basic talker with Serial Poll capability . Unaddressed if MLA.

L4 Listener Basic listener unaddressed if MTA.

SR1 Service Request Complete capability.

RL1 Remote local Complete capability.

PP0 Parallel poll No capability.

DC1 Device clear Complete capability.

DT0 Device trigger No capability.

1-6-2 DEVICE ADDRESS

The device address (between 0 and 30) is set via the five position rear panel switch. The switch is binary coded with the A0 position corresponding to a 1, the next position to a 2, the next position to a 4 and so on. The positions are activated by pushing them up (on). The Standard is shipped from the factory set with an address of 4 (the middle switch position up and all others down). After the address switch is set, the Standard must be turned off for 10 seconds and then back on to enter the address into the Standard.

1-6-3 DATA FORMATS

The formats that the data must take to set the various functions of the standard are now considered.

PHASE: P-XXX.XXX where X represents any digit from 0 to 9 inclusive. The - sign may be omitted or replaced by a + sign. Leading 0's may be omitted but trailing 0's must be kept. Entries are in degrees.

OFFSET: O-XXX.XXX where X represents any digit from 0 to 9 inclusive. The - sign may be omitted or replaced by a + sign. Leading 0's may be omitted by trailing 0's must be kept. Entries are in degrees.

FREQUENCY: FXXXXX. where X represents any digit from 0 to 9 inclusive. In this case all but one of the X's may be omitted however the decimal point at the end is essential. Entries are in Hertz.

AMPLITUDE: RXXX.X (REFERENCE) or VXXX.X (VARIABLE) where X represents any digit from 0 to 9 inclusive. In this case none of the X's may be omitted even if they are zero but the decimal point may be moved one, two or three places to the left. Entries are in Volts.

STANDBY: S

OPERATE: N

AUTOZERO: Z

SRQ MASK: See 1-6-5 below.

1-6-4 SERIAL POLL

The Status byte returned when the Phase Standard responds to a Serial Poll has the following format.

Bit 0, bit 1, bit 2, and bit 3 are reserved for messages from the Phase Standard. In particular, bit 0 being set indicates that a hardware error with the keyboard or Buscard exists. Bit 1 being set indicates that the Standard could not AUTOZERO after an AUTOZERO function has been performed. Bit 2 being set indicates that a BOARD OUT error was encountered during initialization and bit 3 being set indicates that the initialization Sine Table check of the both channels has failed.

Bit 4 being set indicates that a message was received by the Phase Standard which it did not recognize. This could result if valid data are sent followed by a Carriage Return, Line Feed or both. The data are accepted but the additional bytes are unrecognized.

Bit 5 being set indicates that the Phase Standard is "busy" and is not prepared to handshake. This condition results when the Standard is in the AUTOZERO mode or when it has been sent a Device Clear command and is reinitializing.

Bit 6 being set indicates that the Phase Standard has requested service by activating the SRQ line. This condition results when a bit in the SRQ mask has been set and the corresponding bit in the Status byte occurs.

Bit 7 is not used.

Bit 0 through bit 4 are reset when the next valid message is received by the Phase Standard except when the SRQ line has been asserted. In this case the bits are reset following the next Serial poll received by the Standard. Bit 5 is reset at the point that the Standard is no longer "busy", and bit 6 is reset following the next Serial poll request received by the Standard.

1-6-5 SRQ MASK

The SRQ Mask is set by sending MY over the interface to the Standard. In this case Y is a byte whose bits correspond to the bits in the Status byte. Only bit 0 through bit 4 may be unmasked by placing a 1 in the appropriate bit positions. When a bit in the Status byte corresponding to an unmasked position occurs, bit 6 in the Status byte is also set and the SRQ interface line is activated by the Phase Standard.

1-7 ERROR MESSAGES

Three significant errors can be detected by the microprocessor in the Model 5000. The first is a hardware error involving either the keyboard or the IEEE-488 interface which is indicated by the message on the Display

ERROR 1
KEYBRD/INTERFACE

When this message is encountered, the POWER should be turned off for at least 10 seconds and then back on again. If the error persists the Standard may be in need of servicing. The second, which is detected during SELF TEST, is a loose board condition which is indicated by the message on the Display

ERROR 4
BOARD OUT

This condition can be remedied by turning the POWER off, removing the top cover, and pressing down firmly on each board in the card rack.

The third error, which is detected during SELF TEST, is a result of one or more bits of the digital sine function in the Variable channel not matching the corresponding bits in the Reference channel. This condition is indicated by the message on the Display

ERROR 8
CHANNEL MISMATCH

When this message is encountered, the POWER should be turned off for at least 10 seconds and another attempt to initialize made. If the error persists the boards in the card rack should be pressed down as described above. If the error still persists the Standard may indeed have a problem and require service.

After any error message normal operation may generally be resumed by pressing the ENTER key.

II THEORY OF OPERATION

2-1 INTRODUCTION

In this section the theory required to understand the operation of the Model 5000 Phase Standard is presented in two levels. First a general overview of the digital synthesis of the two sine waves precisely separated in phase is considered and then a more detailed view of the actual circuits employed to realize this synthesis is presented.

2-2 GENERAL OPERATION

Digital sinewave generation is accomplished by approximating the sinewave by an integral number (per cycle) of precise, equally spaced, steplike samples and then placing the resultant waveform through a sharp cutoff low pass filter to remove the steps. On the basis of the "Sampling Theorem", an exact replica of the approximated sinewave is produced provided that the low pass filter introduces no attenuation and no phase shift. Consequently, if two sinewaves, one a reference and one having a variable phase angle relative to the reference, are generated in this fashion the basic waveforms for the Phase Standard are obtained.

The Phase Standard implements the steplike approximation of the sinewave in three steps. First, an 18 bit phase latch is incremented in fixed equal steps clocked at a fixed frequency (f) such that after an integral number (m) of steps the latch settings repeat. This latch contains the phase settings for the steps approximating the sinewave which will have a frequency of f/m. Second, the output of the phase latch is placed through a 16 bit angle to sine converter which produces the digital values corresponding to the step amplitudes. Finally the converter output drives a digital to analog converter to produce the actual steps.

The Standard produces a variable phase signal from the reference signal by adding the variable phase angle setting to the phase latch for the reference signal, placing the sum through a second 16 bit angle to sine converter which in turn drives a second digital to analog converter.

If the low pass filter which removes the steps from the sinewave approximation is not ideal and has some phase shift, that phase shift adds to the phase angle of the generated signal. If however, both the reference and the variable sinewaves pass through identical filters, the filter phase shifts cancel. Therefore only the filter amplitude response needs to be flat and this is accomplished with sharp cutoff Butterworth filters.

The frequency of the reference and variable sinewaves is obtained by choosing values for f and m. These values are broken into two bands. In the high band f varies by a factor of 2 between 1.6 and 3.2MHz and m takes on values of 32, 64, 128 and 256 such that output frequencies between 6250Hz and 100kHz may be obtained. In the low band f also varies by a factor of 2 between 200kHz and 400kHz and m takes on values of 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536, 131072 and 262144 such that output frequencies

between 1Hz and 6250Hz may be obtained. The Butterworth filter must only filter the steps occurring with the frequency f; hence two fixed filters, one for the high band and one for the low band, can accommodate the two to one variation in frequency in each band. The high band filter has 5 poles and a bandwidth of 500kHz while the low band filter has 4 poles and a bandwidth of 38kHz.

After filtering, the two sinewaves are amplified in variable gain amplifiers and fed to the output terminals. Unfortunately, these amplifiers, when their gains are adjusted differently, add different amounts of phase shift to the two signals. To correct for this phase shift as well as any which results from the mismatch of the Butterworth filters in the two channels, the error which results when the reference and variable signals are set in quadrature is measured with a precision quadrature phase detector and then used as the basis for a correction term which is subtracted from the variable signal. This measurement and correction is performed automatically under microprocessor control; hence it is referred to as Autozeroing.

Basic control of the Phase Standard is accomplished by a microprocessor which not only supervises the keyboard, the display and the IEEE-488 interface but also sets the parameters required for the phase, offset, frequency, reference and variable amplitude.

Figure 2-1-1 is a Simplified Block Diagram which relates the various components discussed above to the actual printed circuit boards in the Phase Standard.

2-3 SPECIAL SYSTEM FEATURES

Before considering the more detailed theory of operation, some of the more important features of the Phase Standard, which contribute to its superior performance, are outlined separately.

2-3-1 BALANCED DIGITAL TO ANALOG CONVERTERS

To properly generate precision sinewaves, a high quality digital to analog converter (DAC) is required. In particular if accuracies are to be kept well below 5m°, at least a 16 bit DAC must be employed. Such converters, however, have a limit on their high frequency performance for two reasons. First the settling time due to internal energy storage is not instantaneous. Second, and much more important, the switching transients or glitches generated when the digital address lines switch to the value for a new step become a much more significant piece of the step duration as the frequency increases. Since the glitch energy is different for different phase angle settings in the variable channel, a significant phase error can be introduced at high frequencies.

The Model 5000 overcomes both of these problems by employing a balanced set of DAC's in both the reference and the variable channel. With this technique, 16 bit accuracy without the phase distortion due to glitches is obtained to beyond 100kHz. The two DAC's alternate in providing the output step approximations for the sinewave. A high speed switching bridge grounds the output of one DAC while the other is supplying the output. In this fashion one DAC is set to a new level and its glitches settle while the other DAC is supplying the the previous level to the output. Not only is deglitching obtained in this fashion, but each DAC operates at half the frequency a single DAC would have to

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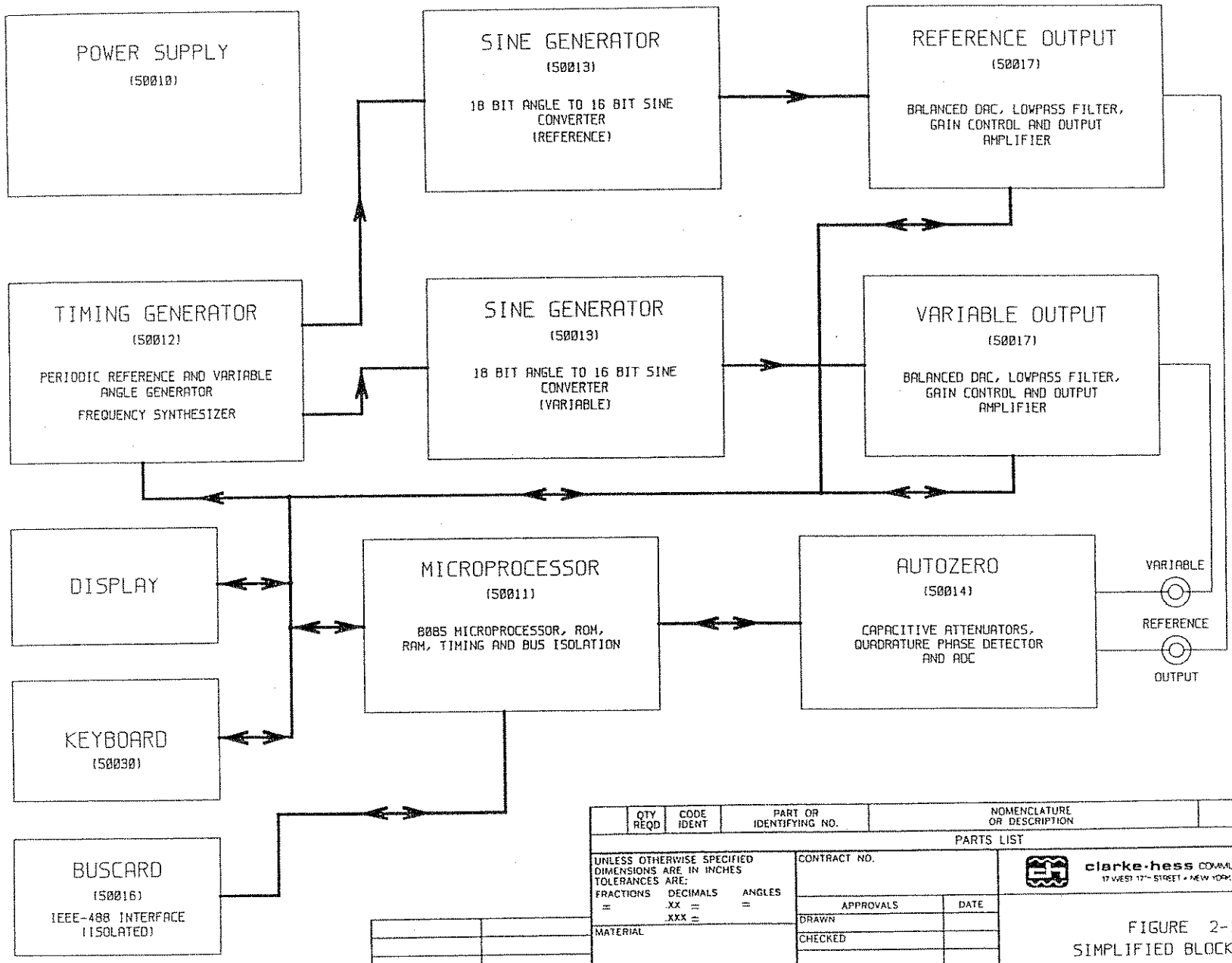

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

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FIGURE 2-1-1
SIMPLIFIED BLOCK DIAGRAM

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operate at with the result that the internal transients have twice the time to settle.

2-3-2 CAPACITIVE ATTENUATOR

The autozero circuit employs a phase detector which determines the error between the two output channels such that a correction can be made. Although the detector has a reasonable input dynamic range, it performs best if its input signals are kept within a 2 to 1 range. Consequently attenuators are required to bring the signals from the output terminals within this range. Unfortunately, any phase shift introduced by one attenuator which is not exactly compensated for by the other attenuator cannot be eliminated from the phase error. This problem becomes particularly severe at high frequencies.

To overcome this problem, the Model 5000 employs high quality binary capacitive attenuators and performs the autozeroing at just one frequency of 5000Hz in the Low band such that the attenuator need only be accurate between 5000Hz and 100000Hz. Unlike resistor or inductor attenuators, capacitor attenuators are immune to the effects of stray capacitance; hence their frequency range is greatly extended. It is true that stray capacitance across any capacitor in the attenuator might result in a slightly different attenuation ratio but it does not affect the phase of the attenuated signal which is the critical parameter.

Each capacitor attenuator employs high quality multi-layer ceramic capacitors which have Q factors in excess of 10,000 in the autozero frequency range. This ensures a maximum phase shift of only one or two millidegrees if the Q's of the various capacitors in an attenuator vary by as much as 2 to 1. To further ensure that the Q' of the capacitors in the attenuator are approximately equal, the majority of the attenuator arms are formed with two capacitors placed in parallel.

Autozeroing at just one frequencys in the Low band is possible because it has been experimentally determined that any phase error caused by channel mismatch increases linearly with frequency with a deviation from a straight line that is well within the accuracy specification of the Phase Standard. Consequently, the phase error determined at the autozero frequency is linearly scaled and applied as a correction at any other frequency in the band.

It is apparent that the standard must autozero at any point where the possible phase shift in either channel is altered. Therefore the Standard must be autozeroed (which is done automatically by the microprocessor) each time an amplitude setting is changed and each time the frequency moves from the high band to the low band which occurs at 6250Hz. Automatic autozeroing also occurs when the frequency crosses 1000Hz since at this point an additional 0.068 microfarad capacitor is switched across the output to reduce high frequency noise.

2-3-3 FREQUENCY SYNTHESIZER

The frequency synthesizer in the Model 5000 has been designed in such a way that no decimal to binary conversions are required to obtain the final input to the synthesizer. The result of this feature is that any frequency appearing on the display has an accuracy determined only by the crystal used in

the synthesizer. The crystal accuracy is typically better 80 parts per million or 0.008%

2-3-4 ANGLE TO SINE CONVERTER

The angle to sine converter generates internally a 16 bit output with an accuracy of the order of 18 bits and then uses the 15 most significant bits plus a sign bit to drive the output DAC. This ensures a maximum error of +/- 0.5 bit in the digital sinewave values supplied to the DAC. The converter itself comprises a set of two 2048 byte read only memories (ROM) which together store 16 bit angle values every $90°/2^{11} = 43.9m°$ over the interval 0° to 90° (See Fig. 2-3-1), and a 2048 byte ROM which adds 32, 8 bit, correction values between each set of sine values or one every 1.37m°. A new set of 32 correction values is introduced every 90°/64 = 1.406°.

The least significant 16 phase angle bits are placed through an "exclusive or" latch which is controlled by bit 17. The 16 bit output of the latch, whose value is complimented every 90°, drives the ROM's; hence the modified drive moves from 0° to 90° on the sine table and then back to 0° where it starts again as the phase angle moves from 0° to 360°. In addition, the combined output of the ROM's is shifted down one bit (the least significant bit is discarded and the most significant bit is set at zero) and then is placed through an "exclusive or" latch which is controlled by bit 18 of the phase. This latch compliments the output values from 180° to 360° thereby providing the proper digital drive to produce a negative going sinewave in this region. The two "exclusive or" latches extend the 0° to 90° sine tables to 0° to 360°.

The accuracy of the above procedure can best be seen by considering an angular deviation of y away from an angle x. If z = sin(x + y) then z may be expanded in the form

$$z = \sin(x)\cos(y) + \cos(x)\sin(y)$$

which for small angles may be approximated by

$$z = \sin(x)(1 - y^2/2) + \cos(x)(y - y^3/6).$$

The sin(x) term is the term contained in the first set of ROM's, the cos(x)y term is the correction term contained in the correction ROM and the other two terms are error terms. In the worst case for the first term when sin(x) = 1, the error produced by the deviation between two successive samples is $y^2/2$ where y is the angle between two successive samples expressed in radians; hence with a deviation of 43.9m° the error has a value of 0.294×10^{-6} or equivalently is less than 1 bit in 21. For the worst case for the second term when cos(x) = 1, the error produced by the deviation between two successive updates in the value of cos(x)y in the correction table is $y^3/6$ where y is expressed in radians. With a deviation of 1.406° the error has a value of 2.46×10^{-6} or equivalently is in the order of 1 bit in 18. This error dominates however it is still extremely small since only the first 15 bits are being kept.

2-4 SYSTEM TIMING

The timing signals for the Phase Standard are shown in Fig 2-3-1. The

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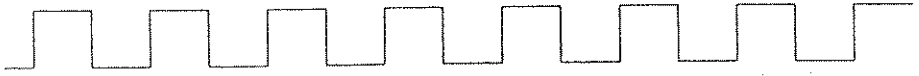
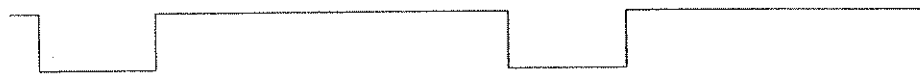
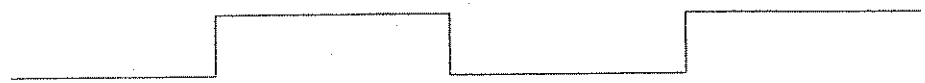
NAME	WAVEFORM	COMMENTS
CLKLF		FREQUENCY SYNTHESIZER OUTPUT
CLK = CLK1 =CLK2		PHASE & SINE LATCHES CLOCKED ON POSITIVE TRANSITIONS
$\overline{\text{UPDATE}}$		BASIC SIGNAL FOR OUTPUT DAC ALTERNATION
PLSIN		FAST PULSE FOR DAC1 AND DAC2 GENERATION
$\overline{\text{PLSIN}}$		FAST PULSE FOR DAC1 AND DAC2 GENERATION
DAC1 INPUT LATCH DAC2 OUTPUT LATCH		LATCH OF DAC LOADED WHEN PULSE IS LOW
DAC1 OUTPUT LATCH DAC2 INPUT LATCH		LATCH OF DAC LOADED WHEN PULSE IS LOW
DAC1		WHEN HIGH DAC1 DRIVES OUTPUT AMPLIFIER
DAC2		WHEN HIGH DAC2 DRIVES OUTPUT AMPLIFIER

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

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FIGURE 2-3-1
PHASE STANDARD TIMING SIGNALS

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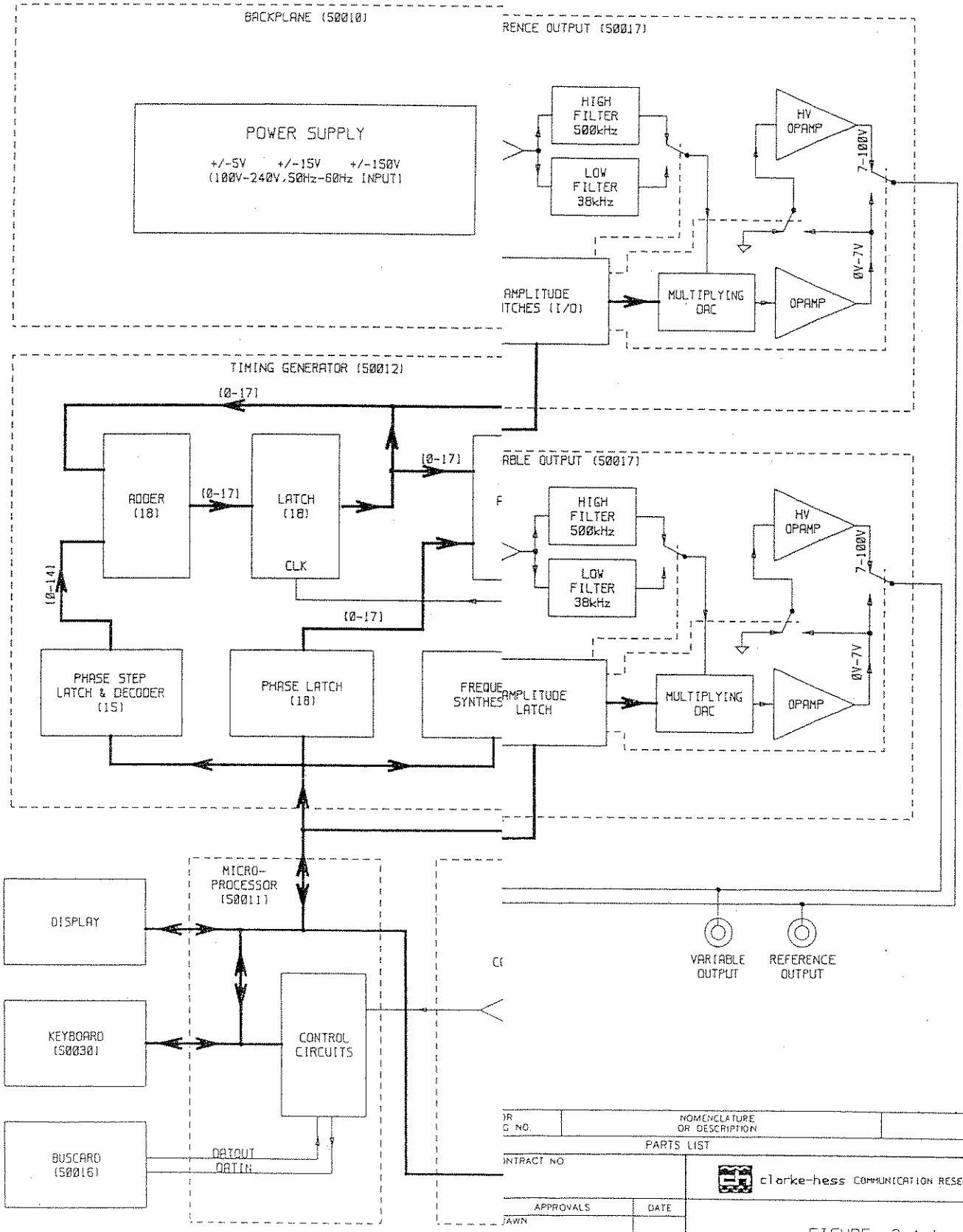

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FIGURE 2-4-1
DETAILED BLOCK DIAGRAM

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2-5-2 MICROPROCESSOR (50001)

The microprocessor board provides the intelligence for the Phase Standard. Via a program stored in the Programmable Read Only Memories (PROM) (U4, U5 and U6) and a Random Access Memory (RAM) (U7), the 80C85 microprocessor supervises the IEEE-488 interface, the Keyboard and the Display and provides the required phase, frequency and amplitude data for the latches on the Timing Generator board and on the two Output boards. The microprocessor communicates with the isolated IEEE-488 interface in a serial fashion over the DATOUT and DATIN lines. The serial format comprises one stop bit, eight data bits (no parity) and two stop bits. The rate is 300 Baud.

The microprocessor communicates with everything else, including the Keyboard and in the Display, over an eight line isolated bus (BUS0 - BUS7) by reading or writing to external latches. The isolation, which prevents off board failures from loading the internal bus (BI0 - BI7), is provided by two I/O buffers U14 and U15. An external latch is placed on the bus to receive or send data by a memory mapped write or read strobe which enables that latch. The strobes are generated by U10, U11 and U12 which are 3 line to 8 line decoders that are enabled by either the read or write outputs from the microprocessor.

The microprocessor board also contains a timer U1 which receives its input clock from a divide by 2 counter (U8) which reduces the 2.592MHz clock output of the microprocessor to 1.296MHz. The timer, as well as the ROM's and RAM, communicate with the microprocessor over the internal bus. The main function of the timer is to provide independent timing for the 300Hz baud rate used in communicating with the isolated IEEE-488 interface and to provide independent timing for the Autozero function.

An input latch, U13, which also communicates with the microprocessor over the isolated bus, samples the "board in" status of the various printed circuit boards, samples the comparator output from the Autozero board and samples the not UPDATE signal from the Sine Generator board. The "board in" information is used during initialization to ensure that all printed circuit boards are secure in the card rack, while the comparator output is used as the basis for the analog to digital conversion which is required to determine the value of the analog phase detector output on the Autozero board. The UPDATE signal provides the means for independently setting the two DAC's on either output board.

The additional circuits on the board are the High Address Latch (U3) which stores the multiplexed high address during each cycle of the 80C85, and 3 line to 8 line address decoder (U9) which provides the "chip enable" signals for all of the memory mapped devices on the board which include the ROM's, RAM and Timer.

2-5-3 TIMING GENERATOR (50002)

The timing generator produces phase input signals for both the reference and the variable channels. The phase input for the reference channel results from adding fixed increments to an 18 bit Reference Phase latch (U6, U12 and U19). The size of these increments is determined by the size of the phase latch (18 bits: 262144) divided by the number of increments per cycle (m). Table 2-5-3 contains the size of the increments required for the various fre-

quency ranges of the Standard. For any selected frequency, the increment is calculated by the microprocessor and placed in the four least significant bit positions of U20 (FRBIT0 -FRBIT3). The latch output is placed through a 4 line to 16 line decoder (U10 and U18) which in turn drives one input of a 20 bit adder (U1, U7, U11, U16 and U21). The other input of the adder is driven by the output of the Reference Phase latch. The output of the adder drives the input to the Reference Phase latch to complete the feedback loop. When the latch is clocked with the CLK signal, the delay around the loop is sufficient to ensure that the new value loaded into the Reference Phase latch is the previous value plus the required increment.

As an example of the operation assume that the microprocessor stores a 5 in the lowest positions of U20. This activates the 5 line of the 4 line to 16 line decoder and also activates the fifth input line of the adder. This causes a 16 to be added to the phase latch each time a CLK pulse occurs.

The phase input for the variable channel is obtained by adding the required phase angle, which is placed by the microprocessor in the 18 bit latch (U9, U14 and U20), to the output of the Reference Phase latch. The addition is performed by the 20 bit adder comprising U2, U8, U13, U17 and U22.

Table 2-5-3 Increment Size for Various Output Frequencies

Increment	Line	Increments per cycle	Frequency range	Frequency Band
16384	15	16	Not presently used	
8192	14	32	50kHz - 100kHz	High
4096	13	64	25kHz - 50kHz	High
2048	12	128	12.5kHz- 25kHz	High
1024	11	256	6250Hz - 12.5kHz	High
4096	13	64	3125Hz - 6250Hz	Low
2048	12	128	1563Hz - 3125Hz	Low
1024	11	256	781Hz - 1563Hz	Low
512	10	512	391Hz - 781Hz	Low
256	9	1024	195Hz - 391Hz	Low
128	8	2048	98Hz - 195Hz	Low
64	7	4096	49Hz - 98Hz	Low
32	6	8192	24Hz - 49Hz	Low
16	5	16384	12Hz - 24Hz	Low
8	4	32768	6Hz - 12Hz	Low
4	3	65536	3Hz - 6Hz	Low
2	2	131072	2Hz - 3Hz	Low
1	1	262144	1Hz - 2Hz	Low

2-5-4 FREQUENCY SYNTHESIZER (50002)

This board also contains the Frequency Synthesizer which comprises the digital synthesizer (U4), the loop amplifier (U15) and the voltage controlled oscillator (U23) which are arranged to form a Phase Locked Loop (PLL). The digital synthesizer contains two programmable counting chains whose outputs are compared in a phase detector which, in turn, drives the loop amplifier. The output of the amplifier drives the control input of the VCO. The output of the VCO both provides an input to the digital synthesizer which completes the PLL and serves as the synthesizer output.

The first counting chain in the digital synthesizer divides an internal 2.3040MHz crystal oscillator by 1800 to obtain 1280Hz while the second divides the VCO output by a factor N. Since the action of a PLL is to keep the two signals entering the phase detector identical in frequency, it is apparent that

$$f_v = N \times 1280Hz$$

where f_v is the frequency of the synthesizer output. Thus as N is programmed between 2500 and 5000, f_v varies in proportion between 3.2MHz and 6.4MHs which is the required range of variation for the high band.

A divide by 10 counter (U24) provides the synthesizer output for the low band. In this case values of N between 3125 and 6250 cause the synthesizer output to vary in proportion between 400kHz and 800kHz. Logic circuits (U26) controlled by the three most significant bits of latch U3 (which is set by the microprocessor) select the high band or the low band output to form CLKLF (the synthesizer output from the board).

The counting chains of the digital synthesizer are programmed by a series of 4 bit instructions applied as D0, D1, D2 and D3 and strobed to the synthesizer by a positive going LOAD pulse (see Dwg. No 50002). Each nibble requires a minimum settling time of 50 microseconds. The format for the serial entry is an address nibble followed by the corresponding data nibble. Table 2-5-4 shows the complete programming sequence for the synthesizer. In the table N0 is the least binary coded decimal (BCD) nibble of N, N1 is the next significant nibble and so on. The microprocessor accomplishes this loading sequence by strobing the appropriate values into the 5 lowest bits of latch U3 in sequence.

Table 2-5-4. Programming Sequence for Synthesizer

D0 - D3	Comments
F (hex)	Address of first counting chain
1	Value for division by 1800
E (hex)	Address of second counting chain MSB
N3	MSB of N
D (hex)	Address of second counting chain NMSB
N2	NMSB of N
C (hex)	Address of second counting chain NLSB
N1	NLSB of N
B (hex)	Address of second counting chain LSB
N0	LSB of N

2-5-5 SINE GENERATOR (50003)

Two identical sine generation circuits are contained on the Sine Generator board. Each comprises an input "exclusive or" latch, sine table ROM's, an adder and an output "exclusive or" latch. The "exclusive or" latches are made up of a set of inverting and a set of non inverting latches which are wired in parallel. The latch data or their compliment are obtained by enabling the output of the non inverting set or the inverting set respectively. The operation of the circuit has been described in Sub Section 2-2-4 above with the aid of the block diagram shown in Fig. 2-4-1. One additional point should be noted

however. Since both input and output latches are clocked by the same signal CLK which also clocks the Reference Phase latch, a pipelining effect is present. Hence the sine data in the output "exclusive or" latch lag the phase data in the input "exclusive or" latch by one clock period. For the same reason the data in the input latch lag the phase data in the Reference Phase latch (Dwg. No. 50012) by the same amount. To equalize the effect of pipelining, bit 16 of the input phase signal must be clocked into a single latch before it is used to control the first "exclusive or" latch while bit 17 must be clocked successively through two latches before it is used to control the second "exclusive or" latch.

Table 2-5-5 contains the circuit designations for the various integrated circuits which comprise the blocks in the diagram.

Table 2-5-5 Circuits Contained in Block Diagram.

Description	Reference Channel	Variable Channel
Input XOR Latch	U1, U2, U3 and U4	U16, U17, U18 and U19
Sine Table ROM's	U5 (high) and U6 (low)	U20 (high) and U21 (low)
Correction ROM	U7	U22
Adder	U8, U9, U10 and U11	U23, U24, U25 and U26
Output XOR Latch	U12, U13, U14 and U15	U27, U28, U29 and U30

The additional circuits on this board divide the CLK signal by 2 to obtain not UPDATE which is the basic timing signal for multiplexing the output DAC's and then they logically combine UPDATE with CLKLF to obtain the high speed current pulses PLSIN and not PLSIN form the collectors of Q1 and Q2 respectively. The leading edges of these pulses are employed on the Output boards to generate the switching signals which drive the switching bridge at the DAC outputs.

2-5-6 OUTPUT (VARIABLE AND REFERENCE) (50007)

Each output board contains the set of 16 bit DAC's (U17 and U18), the high speed switching bridge (U19) and its driver, the summing amplifier (U21), the high band filter (U22 and U23), the low band filter (U24 and U25), the multiplying DAC (U26) to control the gain, the low voltage amplifier (U27) and the high voltage amplifier (U28). The 16 bit DAC's are driven in parallel by the appropriate output (Reference of Variable) of the Sine Generator board. Each DAC contains two internal 16 bit latches, an input and an output latch through which the digital sine values are pipelined. The output latch directly controls the analog current output. Figure 2-3-1 shows the timing waveforms (lines 6 and 7 of the figure) which control the flow or data through the latches. These waveforms are generated internally within the latches from the UPDATE, not UPDATE and CLK signals. It is apparent from the points in time at which the input latches of both DAC's are loaded that the digital sine values, which are updated on each positive going transition of CLK, alternate between the two DAC's on each output board. After the output latches are loaded and given time to settle, the DAC1 and DAC2 signals which are applied to the switching bridge, switch the appropriate DAC output current from a short to ground to the input of the summing amplifier. The output of this amplifier yields the desired analog sinewave at a 7.07V rms level.

A set of potentiometers permits the precise adjustment of the zero level and the full scale value of each DAC. P2 and P4 are the zero adjust potentiometers while P1 and P3 are the full scale adjust potentiometers for DAC1 and DAC2 respectively.

The discrete driving network develops the precise DAC1 and DAC2 signals from the PLSIN and not PLSIN high speed pulses. The PLSIN pulse saturates Q3 and Q6 which reduces DAC1 to -5V and simultaneously increases DAC2 to +5V. The not PLSIN pulse saturates Q4 and Q5 which reduces DAC2 to -5V and simultaneously increases DAC1 to +5V. During the time the high speed pulses are not present, the levels of DAC1 and DAC2 are held constant by the input capacitance of U19. The saturated transistors also have a chance to recover thereby permitting more rapid and precise switching at the occurrence of the next pulse.

The high filter comprises two stages of active filtering to obtain four of the five poles of a 500kHz Butterworth filter. The fifth pole is obtained by means of C55 and C56 and the internal DAC resistors in the feedback loop of the summing amplifier. The low filter comprises two stages of active filtering to obtain the four pole 38kHz Butterworth filter. Both the high and the low filter have unity transmission in their pass bands; hence, the signal level at the output of either filter when it is connected to the output is 7.07V rms. Any offset introduced by the high filter can be adjusted to zero by P7 while and offset introduced by the low filter can be adjusted to zero by P8.

Gain control on the output board is accomplished by means of the 12 bit multiplying DAC whose current output drives the low voltage output amplifier. The parameters of this combination have been selected to produce an output of slightly greater than 7.10V when all bits of the DAC have been activated. A potentiometer P5 permits accurate adjustment of this level. Consequently with proper control of the DAC, output voltages between 100mV and 7.1V may be obtained at the output of the low voltage amplifier. The 12 control lines of the DAC are driven by latch U31 and the 4 most significant bits of U32. The required values are set in these latches by the microprocessor via its external bus.

Output voltages between 7.1V rms and 100V rms are obtained from the high voltage output operational amplifier which has a gain of approximately 14. Exact adjustment of this gain is accomplished with the aid of potentiometer P9. Potentiometer P6 permits the dc offset adjustment of the high voltage amplifier.

A set of relays on the Output board select between the high and the low filter and the low voltage and high voltage amplifier. The relays are activated by the relay drivers contained in U33, which are in turn controlled by the four least significant bits of the microprocessor controlled latch, U32. Relays RL1 and RL2 connect either the high filter or the low filter to the input of the multiplying DAC. Relays RL6 and RL7 connect either the low voltage amplifier or the high voltage amplifier to the output terminals. When RL7 is closed RL3 is also closed to connect the low voltage amplifier to the input of the high voltage amplifier. In addition, when RL6 is closed RL4 is also closed to supply a short circuit for the input of the high voltage amplifier. Relay RL5 connects a capacitor C58 across the output of the low voltage amplifier for frequencies below 1000Hz such that the small residual output noise is reduced even further at low frequencies. Complimentary drives for RL1 and RL2 and for

RL6 and RL7 are obtained from two inverters contained within U34.

Two additional output latches, U29 and U30, are included on the Output board. These latches, which are connected to the external microprocessor bus, sample the digital sine values which are applied to the set of DAC's so that any digital errors may be automatically detected. When power is first applied to the Phase Standard, the microprocessor sets the phase difference between the two Output boards at zero and then slowly increments the Reference and Variable phase such that all possible outputs of the two Angle to Sine converters occur. Each of these possible outputs is sent via the external bus from U29 and U30 of each Output board to the microprocessor where they are compared. If all of the outputs compare exactly, then the entire digital portion of the Phase Standard must be functioning properly.

2-5-7 AUTOZERO BOARD (50004)

The Autozero Board, in conjunction with the microprocessor, compares the Reference and the Variable Output Signals, appropriately attenuated and set in quadrature, in a quadrature phase detector and determines any phase difference. This phase difference is algebraically subtracted from the Variable channel phase and the process is repeated. If the new difference is less than ±1.37m° (one phase bit), the Autozero operation is terminated. If it is not, the new, smaller difference is algebraically subtracted from the Variable channel and the process is again repeated. This operation continues (for a maximum a 15 cycles) until less than a ±1 bit phase error is obtained. The final phase correction is then used by the microprocessor to correct for Reference or Variable channel phase differences which result when the amplitude or frequency in the High band is changed or different filters are placed in the channels.

The phase measurement is performed in four parts to eliminate any errors that might be introduced by the phase detector itself. The Variable Output is first set at 90° with respect to the Reference Output and the detector output R_1 is stored in memory by the microprocessor. The inputs to the phase detector are then reversed and the detector output R_2 is stored in memory. These two measurements are then repeated with the Variable Output set at 270° with respect to the Reference Output to produce detector output values of R_3 and R_4 which are stored in memory. The microprocessor then performs the calculation

$$[(R_1 - R_3) + (R_2 - R_4)] / 4$$

which yields the desired phase difference. The differences $(R_1 - R_3)$ and $(R_2 - R_4)$ eliminate the effects of dc offset and signal crossover in the phase detector while the sum of the two difference terms eliminates the effect of any phase difference in the two channels of the detector itself.

Each measurement is performed by the microprocessor in 50msec with the result that the two terms in brackets which must be subtracted are measured precisely 100msec apart. This is done such that both values are measured at the same phase point of either a 50Hz or 60Hz signal; hence the effect of line frequency pickup in the high impedance attenuator is virtually negligible since it is canceled by the subtraction.

The Autozero function is implemented by the following circuits on the Autozero Board: the reference and the variable attenuators, the corresponding high input impedance amplifiers (U2 and U7), the phase quadrature phase detector, the channel gain adjust DAC (U11), and the DAC (U10) and comparator (U8)

which function in conjunction with the microprocessor as the Analog to Digital Converter.

Each attenuator is a dual input, constant 4500pF impedance (as viewed from the output), 5 stage binary attenuator. The second input to the attenuator is via a 91pF capacitor shunted by a variable capacitor to provide an additional precisely adjustable, factor of 32 attenuation. C1 and C18 permit this adjustment in the Reference and the Variable channel respectively. The attenuator settings are controlled by SPST relays which are driven by relay drivers (U12 - U15). The drivers are selected by the microprocessor controlled latches (U19, U20 and U21). Table 2-5-7-1 illustrates the relay closures which keep the signal output of the attenuator between 67mV and 133mV rms as the attenuator input varies between 100mV and 100.9V rms.

Table 2-5-7-1

Input Voltage	Activated Relays	
	Reference Channel	Variable Channel
100mV-199mV	RL2, RL4, RL5	RL14, RL16, RL17
201mV-398mV	RL2, RL4, RL6	RL14, RL16, RL18
400mV-799mV	RL2, RL4, RL7	RL14, RL16, RL19
801mV-1.598V	RL2, RL4, RL8	RL14, RL16, RL20
1.600V-3.198V	RL2, RL4, RL9	RL14, RL16, RL21
3.200V-6.399V	RL1, RL3, RL5	RL13, RL15, RL17
6.401V-12.77V	RL1, RL3, RL6	RL13, RL15, RL18
12.80V-25.57V	RL1, RL3, RL7	RL13, RL15, RL19
25.60V-51.17V	RL1, RL3, RL8	RL13, RL15, RL20
51.20V-100.9V	RL1, RL3, RL9	RL13, RL15, RL21

The attenuator output is connected via SPST relays to the gain of 8 amplifier which produces signal levels between 533mV rms and 1067mV rms at the multiplier (U1) inputs. Activating relays R11 and R23 connects the attenuators in a normal fashion to the two amplifiers while activating relays R10 and R22 reverses the two amplifier inputs. In normal operation relays R10 and R22 remain activated.

The phase detector comprises the multiplier (U1), its self zeroing circuitry (U1 and U5) and the output filter (U4 and U6). Prior to each Autozeroing cycle, relays RL12, RL24 and RL25 are closed which reduces the multiplier inputs to zero and simultaneously produces a feedback current from the self zeroing amplifiers which forces its output to zero. This feedback current is "held" by C42 when RL25 is opened during the remainder of the Autozero function and during normal operation. The input offset voltage in the Reference and Variable channel is adjusted to zero manually during calibration with P1 and P2 respectively.

The output filter is a third order filter with three identical poles at 53Hz. One pole is obtained from U4 which also converts the multiplier output current to an output voltage, while the other two poles are obtained from the unity gain amplifier U6. With these poles the detector settles to the required accuracy after a sudden change in input in less than 48msec.

The parameters of the multiplier have been chosen such that with the min-

imum input of 533mV in both channels, the sensitivity at the filter output is 1mV/m°. As the input levels are increased the sensitivity at the filter output also increases in a nonlinear fashion. This effect is compensated for by the multiplying DAC (U11), which is controlled by the microprocessor via latches U16 and U18, in such a fashion that the sensitivity at the DAC output remains essentially constant for all input amplitudes to the multiplier. In particular, after a gain of 5, the sensitivity at the output of U9 is approximately 5mV/m°.

The signal at the output of the multiplying DAC is sensed by the microprocessor by means of the second DAC U10 and the voltage comparator U8 whose output is fed back to the Microprocessor Board. The microprocessor via latches U16 and U17, in a binary search fashion, adjusts the output of U10 until the output of U9 is zero as indicated by a transition in the output of the comparator. The digital input to U10 at the null is a direct measure of the detector output. The sensitivity of U10 is adjusted such that the least significant bit of U10 corresponds to the least significant bit in phase or 1.37m°. This is accomplished by adjusting P3 such that the voltage at pin 17 of U10 is approximately 5.35V. P4 is adjusted such that the voltage at pin 18 is approximately 2.7V. This adjustment insures an equal plus and minus excursion for the DAC.

Neither adjustment of P3 or P4 is extremely critical. Since the output of the phase detector is computed from the difference of two readings, any offset from P4 is canceled in the subtraction. In addition, since the Autozero operation is repeated until the phase difference between the two channels is reduced to zero, slight sensitivity errors can in the worst case result in one or two additional Autozero cycles.

Table 2-5-7-2 illustrates the timing for a complete Autozero cycle. In the Table T is equal to -100msec for the first Autozero Cycle and equal to -40msec for all subsequent Autozero Cycles in a particular Autozero sequence. The activated relays indicated in the Table are those in addition to the ones shown in Table 2-5-7-1.

Table 2-5-7-2 Autozero Timing

Time(msec)	Phase	Activated Relays	Outputs	Description
T		RL3, RL4, RL11, RL12, RL13, RL16, RL23, RL24, RL25	Zero	Ground detector input Self zero U1 output
0		RL3, RL4, RL11, RL12, RL13, RL16, RL23, RL24	Zero	Open self zero relay
3.3	90°	RL11, RL23	Zero	Unground inputs
6.6	90°	RL11, RL23	Full	Bring up outputs
43.3	90°	RL11, RL23	Full	Store detector output

46.6	90°	RL3, RL4, RL10, RL12, RL13, RL16, RL22, RL24	Zero	Ground detector input
53.3	90°	RL10, RL22	Zero	Unground inputs
56.6	90°	RL10, RL22	Full	Bring up outputs
93.3	90°	RL10, RL20	Full	Store Detector output
93.6	270°	RL3, RL4, RL11, RL12, RL13, RL16, RL23, RL24	Zero	Ground detector input
103.3	270°	RL11, RL23	Zero	Unground inputs
106.6	270°	RL11, RL23	Full	Bring up outputs
143.3	270°	RL11, RL23	Full	Store detector output
153.3	270°	RL3, RL4, RL10, RL12, RL13, RL16, RL22, RL24	Zero	Ground detector input
156.6	270°	RL10, RL22	Zero	Unground inputs
193.3	270°	RL10, RL22	Full	Bring up outputs
196.6	270°	RL10, RL20	Full	Store Detector output

2-5-8 KEYBOARD (50008)

The Keyboard is a 4 x 8 matrix which is scanned by the microprocessor when the Standard is not in its REMOTE state or not performing any other operation such as Autozeroing. The microprocessor via the external bus, sequentially sets D0, D1, D2 and D3 in latch U2 with the result that the corresponding line in the switching matrix is driven to zero by U3 which performs the function of a Quad inverter. After each line is set, the microprocessor checks the matrix output via latch U1 to determine if a key has been pressed. If a key switch closure is detected, the microprocessor waits 10msec to let the switch debounce and then checks to see if the switch is still closed. If it is, the position on the matrix is decoded by the microprocessor and the appropriate action taken.

If the Standard is in its REMOTE state, only the LOCAL key switch is scanned.

2-5-9 BUSCARD (50006)

The Buscard comprises a General Purpose Bus Controller (U8), a set of bus driver modules (U9 and U10), a microprocessor (U6), a pair of optical isolators (U2 and U3) and their associated drivers (U1 and U5), and a 5V regulator (U4) to supply isolated power to the board.

The Bus Controller implements all of the required IEEE-488 interface functions required by the Standard and communicates with the bus via the driver modules. The microprocessor provides an interface between the isolated 300 baud serial link to the Standard (DATOUT and DATIN lines) and the Bus Controller. It also provides the initialization for the Bus Controller, including the address set with SW1, when power is applied. In addition, the microprocessor screens the incoming data for the proper format. If it is not correct it does not transmit it to the Standard.

The microprocessor uses an XON - XOFF (DC1 - DC3) handshake with the Standard. Any time XOFF is transmitted from the Standard to the Buscard, the microprocessor inhibits further reception of data from the Bus Controller and indicates this condition by activating bit 5 of the Serial Poll. This condition which prevents handshaking with the IEEE-488 interface persists until an XON is received from the Standard. The Standard always sends XOFF prior to executing an Autozero function and XON immediately following it.

2-5-10 DISPLAY

The Display is a complete assembly produced by the IEE Corporation. Their Data Sheet for the device is included at the end of this Section. The microprocessor communicates with the Display over the external bus.

FLIP 2x16 DOT MATRIX VACUUM FLUORESCENT

36X1-32-032

IEE INDUSTRIAL PRODUCTS DIVISION

FLIP 2 LINE x 16 CHARACTER 5x7 DOT MATRIX VACUUM FLUORESCENT DISPLAY MODULE

FEATURES

- 32-character format displays extra-large 0.44 in. (11.3mm) characters for easy reading at a distance
- 5x7 dot matrix for bright, clear display of upper and lower case characters
- High brightness — up to 300 fL — with software-controlled dimming
- Enter data from left to right, scroll from right to left, or randomly at any character address
- On-board microprocessor controller supports many ASCII control functions including carriage return, line feed, advance or backspace cursor
- 8-bit bidirectional bus requires minimum hardware to interface to most microprocessors
- Jumper-selectable TTL or RS-232 serial operation at 1200 baud
- Requires only +5VDC power supply
- Pleasant blue-green display spectrum is filterable to blue, green, aqua or yellow
- Underwriters Laboratories, Inc. Recognized Component
- Scientific or ECMA General European, German or Scandinavian font alternates under software control (ASCII Standard)
- Extended operating temperature (−40 to +185°F, −40 to +85°C) model available (3611-3200)

APPLICATIONS

- Numerical control machine tools
- Telecommunications devices
- Medical equipment
- Copiers
- Automatic labeling equipment
- Mobile communications
- Automated banking terminals
- Point-of-sale terminals
- Remote data entry terminals
- Alarm, safety and security systems
- Simulators
- Automatic test equipment
- Automotive diagnostic equipment
- Energy management systems
- Customer information
- Retail advertising

DESCRIPTION

The FLIP 36X1-32-032 is a Vacuum Fluorescent Alphanumeric Display Module arranged as 2 lines of 16 characters. The characters are formed using a large 0.44 inch (11.3mm) 5x7 dot matrix which allows easy viewing from a distance and over a wide viewing angle, while displaying upper and lower case characters. The full 96-character ASCII font can be displayed and it can be altered to include the characters necessary to produce ECMA General European, German or Scandinavian fonts, as well as a selection of scientific characters, all under software control. The 32-character format and large character size make the 36X1-32-032 ideal for applications in equipment where distance readability is important such as point-of-sale terminals, process control, alarm and security systems, automatic test equipment, and mobile communications.

The FLIP 2x16 characters are a BRIGHT blue-green color which is filterable to blue, green, aqua or yellow, and they are easily read at a distance and over a wide viewing angle.

All control, refresh and display functions of the module are executed by a dedicated on-board microprocessor, and a miniature on-board DC to DC voltage converter provides all the voltages necessary to light the vacuum fluorescent display while allowing the FLIP 2x16 module to operate from a SINGLE 5 VOLT POWER SUPPLY.

Data interfacing is via an 8-bit bidirectional TTL-ASCII data bus or serial data input using 1200 baud jumper-selectable TTL or RS-232 serial data formatted as an ASCII word. By use of simple commands or ASCII control codes, data can be selectively written to or read from any character location, alternate fonts can be selected, or the status of the data latch can be determined.

For over 30 years IEE has been known as a reliable, responsive, quality conscious supplier of displays of various technologies. Every IEE customer is important customer. We are certain after you have reviewed the following information and evaluated our FLIP 2x16 module you will understand how we earned our reputation as "The Display Makers".

FLIP™

OPERATION

Interfacing with FLIP Displays is very simple and requires a minimum of handshaking. Data entry to the module can be either parallel or serial, providing maximum flexibility. Parallel data can be bidirectional or unidirectional depending on character load rate and system requirements.

Data bus signals are formatted in accord with standard ASCII which allows control functions to be included in the character code matrix table. Functions such as locating the cursor position or selecting the end-of-line mode are implemented with a single 8-bit control word.

Characters may be randomly entered at any position on the character field by first sending the module a command to set the cursor at the desired character location and then entering an ASCII character code. This character location address is only required when it is desired to load the next character at other than the next sequential location. In the case of end-of-line data entry, the end-of-line mode selected determines the location of the "overflow" characters.

PARALLEL OPERATION

Operation in the parallel mode requires little, if any, extra hardware to interface with a host processor bus. Characters sent on the data bus are entered at the cursor position addressed, and are latched by the display module upon receiving a $\overline{\text{WRITE}}$ pulse. The cursor then automatically advances to the next character position.

The display module is addressed as two RAM memory locations in a memory map I/O configuration. User address lines A_1 through A_{15} may be decoded to provide a low enable for the $\overline{\text{DEVICE SELECT}}$ ($\overline{\text{CS}}$) input to allow communication with the module. The least significant address bit is connected to A_0. When A_0 is low, ASCII control or character data presented on the 8-bit data bus can be written to or read from the display by means of a $\overline{\text{WRITE}}$ or $\overline{\text{READ}}$ pulse from the host microprocessor. When A_0 is high, pulsing $\overline{\text{READ}}$ low allows the user to check the input/output buffer status, and pulsing $\overline{\text{WRITE}}$ low allows the user to input various additional commands.

When parallel data is placed on the data bus and a $\overline{\text{WRITE}}$ pulse is applied to the $\overline{\text{WR}}$ input, the data is entered into an input buffer in the microprocessor controller. The microprocessor then examines this data to determine its nature, (i.e. to see if it is a control code, a character, etc.) and if it is a character it is stored in the display refresh memory. The time required to execute this process and prepare for a new character determines the display's Character Rate (see execution times).

To obtain the maximum parallel loading rate, the status of the input buffer should be read and new data sent when the buffer is empty. Therefore, with bidirectional bus operation, maximum loading rate is achieved by first writing the character to the display and then reading the input buffer status to determine when the next character can be sent. Input buffer status is also available as a hardware output on J2-4. This output may be used to interrupt the host computer.

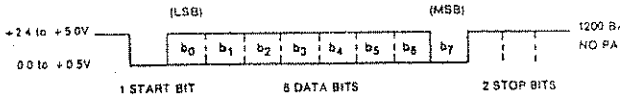
Character loading at the maximum rate can sometimes cause random blank spots or flashes. However, the problem can be corrected by monitoring the status register, which reports the status of the "Low Flicker Window" and the input buffer. When both data bits 1 and 4 of the status register are low, the data input is synchronized with the display's internal refresh. The window is typically open 40 μs and opens approximately once every 700 μs. (See the operating chart.) Character loading can also be accomplished while ignoring the status of the input buffer (at a slight loss in loading rate) by setting character data at a rate determined by the user to be less than the FLIP Display Module's character loading rate.

Bidirectional operation allows the user to read informati from the display. Input and output buffer status is read direc by setting address line A_0 and the $\overline{\text{WR}}$ line high, and then pu ing the $\overline{\text{RD}}$ line low. Reading character data or cursor locati must be preceded by a "PREPARE TO READ..." command.

SERIAL OPERATION

Included as a standard feature in the FLIP 2x16 is a serial as chronous receiver with a jumper-selectable input (T_0) wh allows for either TTL or RS-232 input levels. This input is, course, unidirectional. The display is shipped from the fact with E2 jumpered to E3 for TTL level operation. For RS-2 level input, remove the jumper from E3 and jumper E1 to E

A logic high represents a "mark" and a logic low represent "space" with data formatted as an 11-bit word of one start eight data bits and two stop bits. The data is input at a fi rate of 1200 baud. NOTE: The eighth bit (MSB) must always low, not parity, in order for data to be received properly. (RS-232 input, levels are of course different; but data is form ted similarly with respect to data start and stop bits, M LSB, etc.)



STANDARD TTL SERIAL INPUT

For remote serial operations, an optional FLIP Serial D Converter Module may be obtained. Available from IEE, this terface card is programmable to accept various baud rat data word arrangements, and serial signal level interfaces, cluding EIA RS-232.

SELF TEST

Self test is a very useful feature and can be activated by m taining a logic low (or high, if strapped for RS-232) on the se input (T_0) for a period longer than 4 seconds. ASCII charact from 20 (HEX) to 7F (HEX) will be displayed advancing throu the character field at approximately a 3-character per sec rate. This self test capability can be used to speed up both field fault isolation, and incoming receiving inspection.

POWER-UP, RESET, AND DEFAULT

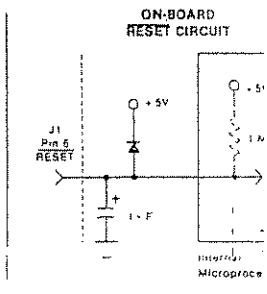
Upon power-up the FLIP Modules go through an initializa routine. This power-up period lasts approximately 500 m the unit is given a software reset command, it execute re-initialization routine that takes approximately 660 Therefore, no data should be written to the FLIP Module 500 ms after power-up or for 660 μs after a software reset. N that for the power-up reset circuit to work properly, the po supply's rise time must be less than 100 ms.

The model 36X1-32-032 has a $\overline{\text{RESET}}$ pin (J1 [power] pi which duplicates the power-up reset sequence when brou to ground.

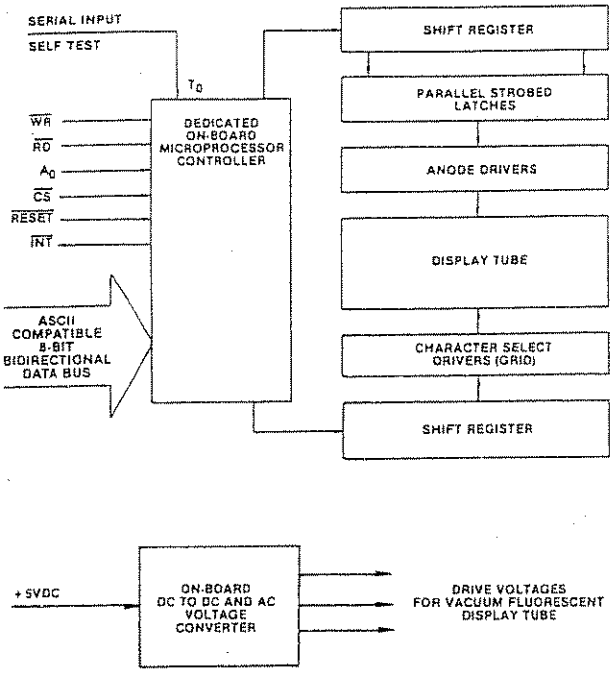
DEFAULT CONDITIONS

The following is a list of default states that the FLIP Module selects on power-up or reset:

- Cursor location in upper left-hand position ("CURSOR HOME")
- English font
- Cursor indicator ON
- Automatic carriage return (End-of-line mode)
- [illegible]
- Display brightness @ "DIMMEST"



BLOCK DIAGRAM



ASCII CHARACTER SET

DATA BITS	b7	0	0	0	0	1	1	1	1
	b6	0	0	1	1	0	0	1	1
	b5	0	1	0	1	0	1	0	1
	b4	0	1	0	1	0	1	0	1
b3 b2 b1 b0	HEX	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	'	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	A	LF	SUB	*	:	J	Z	j	z
1 0 1 1	B	VT	ESC	+	;	K	[	k	{
1 1 0 0	C	FF	FS	,	<	L	\	l	|
1 1 0 1	D	CR	GS	-	=	M	]	m	}
1 1 1 0	E	SO	RS	.	>	N	^	n	~
1 1 1 1	F	SI	US	/	?	O	_	o	▒

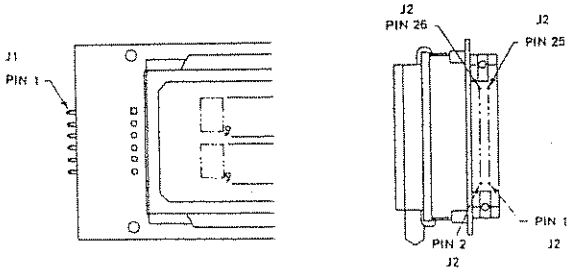
NOTES:
ASCII control words (00 through 1F HEX) are not displayed by FLIP Modules. Refer to operating chart to determine codes implemented, and their respective functions.

OPTICAL CHARACTERISTICS (2 lines of 16 characters)

PARAMETER	RATINGS
Viewing angle	150°
Brightness	200 fL (min.), 300 fL (typ.)—at brightest setting
	Software dimming to approximately 10% of full brightness
Color	Blue-green, peak at 5,000 angstroms (filterable to blue, green, aqua, yellow or red*)
Character height	0.44 in (11.3mm) + comma
Character width	0.29 in (7.25mm) + comma
Character pitch	0.43 in (10.9mm) (center to center)
Character format	5x7 dot matrix + comma
Character set	96-character ASCII + ECMA and scientific alternates

*NOTE: Red is recommended for low light applications only.

CONNECTOR PIN ASSIGNMENTS



J1 (POWER) CONNECTOR PIN ASSIGNMENTS

PIN NO.	FUNCTION
J1-1	+5VDC @ 1.75 AMPS (MAX.)
J1-2	NO CONNECTION
J1-3	NO CONNECTION
J1-4	COMMON
J1-5	NO CONNECTION
J1-6	RESET

J2 (DATA) CONNECTOR PIN ASSIGNMENTS

PIN NO.	FUNCTION	INPUT DESIGNATIONS
J2-1	SERIAL IN/SELF TEST	(T_0)
J2-2	COMMON	
J2-3	DEVICE SELECT	(CS)
J2-4	INTERRUPT*	(INT)
J2-5	READ	(RD)
J2-6	COMMON	
J2-7	ADDRESS ZERO BIT	(A_0)
J2-8	COMMON	
J2-9	WRITE	(WR)
J2-10	COMMON	
J2-11	DATA 2^0 (LSB)	
J2-12	COMMON	
J2-13	DATA 2^1	
J2-14	COMMON	
J2-15	DATA 2^2	
J2-16	COMMON	
J2-17	DATA 2^3	
J2-18	COMMON	
J2-19	DATA 2^4	
J2-20	COMMON	
J2-21	DATA 2^5	
J2-22	COMMON	
J2-23	DATA 2^6	
J2-24	COMMON	
J2-25	DATA 2^7 (MSB)	
J2-26	COMMON	

*When INT is low (0) the display is ready to accept new data. This is the hardware equivalent to reading the Input Buffer Status (See READ INPUT BUFFER STATUS in the operating chart.)

FUNCTION	DATA BUS SIGNALS	INPUT LOGIC LEVEL A_0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	T_0	FUNCTION AVAILABLE IN SERIAL MODE
WRITE ASCII DATA TO DISPLAY	ASCII DATA FROM HOST SYSTEM	0	0	PULSE LOW	1	1	YES
PREPARE TO READ DATA AT PRESENT CURSOR LOCATION* (same as 42 HEX)	04 HEX	0	0	PULSE LOW	1	1	NO
PREPARE TO READ CURSOR LOCATION VALUE* (same as 41 HEX)	05 HEX	0	0	PULSE LOW	1	1	NO
BACK SPACE CURSOR LOCATION ONE POSITION	08 HEX	0	0	PULSE LOW	1	1	YES
ADVANCE CURSOR LOCATION ONE POSITION	09 HEX	0	0	PULSE LOW	1	1	YES
LINE FEED (vertical scroll from bottom line)	0A HEX	0	0	PULSE LOW	1	1	YES
BEGIN CHARACTER BLINK FIELD	0B HEX	0	0	PULSE LOW	1	1	YES
END CHARACTER BLINK FIELD	0C HEX	0	0	PULSE LOW	1	1	YES
CARRIAGE RETURN (returns cursor to left-most character position; does not clear display)	0D HEX	0	0	PULSE LOW	1	1	YES
MAKE CURSOR INDICATOR INVISIBLE (the cursor location counter continues to function but there is no visible indicator of next character location)	0E HEX	0	0	PULSE LOW	1	1	YES
† MAKE CURSOR INDICATOR VISIBLE (this is a blinking indicator of where the next character will be located)	0F HEX	0	0	PULSE LOW	1	1	YES
END-OF-LINE MODES:							
BOTTOM LINE DATA ENTRY WITH AUTOMATIC CARRIAGE RETURN & LINE FEED (data enters beginning at the left-hand character position of the bottom row)	10 HEX	0	0	PULSE LOW	1	1	YES
† NORMAL DATA ENTRY WITH AUTOMATIC CARRIAGE RETURN AND LINE FEED (data enters beginning at the upper left-hand character position)	11 HEX	0	0	PULSE LOW	1	1	YES
OVERWRITE OF RIGHT-MOST CHARACTER/ AUTOMATIC CARRIAGE RETURN OFF	12 HEX	0	0	PULSE LOW	1	1	YES
HORIZONTAL SCROLL MODE (from right to left on bottom line only, after line has been filled)	13 HEX	0	0	PULSE LOW	1	1	YES
RESET (same as 40 HEX)	14 HEX	0	0	PULSE LOW	1	1	YES
† DISPLAY CLEAR (puts cursor at left side bottom row in Mode 10 HEX, & home in Modes 11 HEX, 12 HEX and 13 HEX)	15 HEX	0	0	PULSE LOW	1	1	YES
† CURSOR HOME	16 HEX	0	0	PULSE LOW	1	1	YES
A_0 HIGH FOR NEXT BYTE ONLY (available in both parallel and serial modes)	19 HEX	0	0	PULSE LOW	1	1	YES
SELECT SCIENTIFIC CHARACTERS	1A HEX	0	0	PULSE LOW	1	1	YES
† SELECT ENGLISH FONT (US ASCII-7)	1C HEX	0	0	PULSE LOW	1	1	YES
SELECT GENERAL EUROPEAN FONT (ECMA-7)	1D HEX	0	0	PULSE LOW	1	1	YES
SELECT SCANDINAVIAN FONT (ECMA-7)	1E HEX	0	0	PULSE LOW	1	1	YES
SELECT GERMAN FONT (ECMA-7)	1F HEX	0	0	PULSE LOW	1	1	YES
RESET (same as 14 HEX)	40 HEX	1	0	PULSE LOW	1	1	YES**
PREPARE TO READ DATA AT POSITION XX XXXX* (Location in binary—0 is left most position, upper line)	10XX XXXX	1	0	PULSE LOW	1	1	NO
PREPARE TO READ CURSOR LOCATION VALUE* (same as 05 HEX)	41 HEX	1	0	PULSE LOW	1	1	NO
PREPARE TO READ DATA AT PRESENT CURSOR LOCATION* (same as 04 HEX)	42 HEX	1	0	PULSE LOW	1	1	NO
PREPARE TO READ DATA AT PRESENT CURSOR LOCATION AND INCREMENT CURSOR*	43 HEX	1	0	PULSE LOW	1	1	NO
† DISPLAY DIMMEST	4C HEX	1	0	PULSE LOW	1	1	YES**
DISPLAY DIM	4D HEX	1	0	PULSE LOW	1	1	YES**
DISPLAY BRIGHT	4E HEX	1	0	PULSE LOW	1	1	YES**
DISPLAY BRIGHTEST				PULSE LOW			

OPERATING THE 36X1-32-032 2x16 FLIP (continued)

FUNCTION	DATA BUS SIGNALS	INPUT LOGIC LEVEL A_0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	T_0	FUNCTION AVAILABLE IN SERIAL MODE
NEXT CHARACTER WILL HAVE PERIOD ATTACHED	50 HEX	1	0	PULSE LOW	1	1	YES**
NEXT CHARACTER WILL HAVE COMMA ATTACHED	51 HEX	1	0	PULSE LOW	1	1	YES**
MOVE CURSOR TO LOCATION XX XXXX*** (Location in binary—0 is left most position, upper line)	00XX XXXX	1	0	PULSE LOW	1	1	YES**
MOVE CURSOR TO LOCATION XX XXXX*** (Location in binary—left most location is zero. L = 0 Upper line, L = 1 Lower line)	1LXX XXXX	0	0	PULSE LOW	1	1	NO
MOVE CURSOR TO FOLLOWING POSITION*** (2 byte instruction to locate cursor in serial (or parallel) mode)	1B HEX	0	0	PULSE LOW	1	1	YES
SECOND BYTE (location in binary—left-most location is zero. L = 0 Upper line, L = 1 Lower line)	0LXX XXXX	0	0	PULSE LOW	1	1	YES
READ DATA FROM DISPLAY MODULE (Performed after a prepare to read function)	ASCII DATA OR CURSOR LOCATION VALUE	0	0	1	PULSE LOW	1	NO
READ OUTPUT BUFFER STATUS (Data may be read from the display module when the output buffer is full)							
DATA BIT 0 = 1: OUTPUT BUFFER FULL	XXXX XXX1 OR	1	0	1	PULSE LOW	1	NO
DATA BIT 0 = 0: OUTPUT BUFFER EMPTY	XXXX XXX0						
†† READ INPUT BUFFER STATUS (Data may be written to the display module when the input buffer is empty)							
DATA BIT 1 = 1: INPUT BUFFER FULL	XXXX XX1X OR	1	0	1	PULSE LOW	1	NO
DATA BIT 1 = 0: INPUT BUFFER EMPTY	XXXX XX0X						
READ LOW FLICKER STATUS (When both data bits 1 and 4 are low, writing data to the display will not cause blank spots or bright flashes to occur)							
DATA BIT 4 = 1: LOW FLICKER WINDOW CLOSED	XXX1 XXXX OR	1	0	1	PULSE LOW	1	NO
DATA BIT 4 = 0: LOW FLICKER WINDOW OPEN	XXX0 XX0X						
DISABLE DISPLAY DATA INPUT		DON'T CARE	1	DON'T CARE	DON'T CARE	DON'T CARE	NO
SELF TEST (ASCII characters appear from left to right at 3 per second rate)		DON'T CARE	DON'T CARE	DON'T CARE	DON'T CARE	HOLD LOW (TTL) OR HIGH (RS-232) FOR 4 SEC.	YES
SERIAL ENTRY (11-bit serial word at 1200 baud rate 1 start bit, 8 data bits, 2 stop bits)		DON'T CARE	DON'T CARE	DON'T CARE	DON'T CARE	TTL OR RS-232 LEVEL SERIAL DATA	YES

†Display automatically defaults to these conditions after power-up and reset.
††Input buffer status is also available on J2-4 of the data connector as $\overline{INT}$. When $\overline{INT}$ is low (0), the input buffer is empty and the display is ready to accept new data.

***"PREPARE TO READ..." commands should be followed with a "READ DATA FROM DISPLAY MODULE" operation.
**These functions are available in the SERIAL mode when preceded by an "A_0 HIGH FOR NEXT BYTE ONLY" command (19 HEX).
***The three "MOVE CURSOR" commands perform the same function and are offered for programming convenience.

NOTE: CARE SHOULD BE TAKEN NOT TO SEND UNDEFINED CONTROL OR COMMAND CODES TO THE FLIP DISPLAY MODULE AS THIS MAY CAUSE A SOFTWARE MALFUNCTION OF THE MODULE.

ALTERNATE FONT CODES

All FLIP models access the English font (U.S. ASCII-7) on POWER-UP and allow the user to convert to any one of several alternate fonts. Font choice is a mutually exclusive latched function of the last font control code sent to the display model. The alternate characters accessed are as follows:

FONT SET	CONTROL CODE (HEX)
Scientific	1A
U.S. ASCII-7	1C
General European ECMA	1D
Scandinavian ECMA	1E
German ECMA	1F

CONTROL CODES (HEX)	ASCII LOC (HEX)	DISPLAYS
1A	5B	≠
1A	5C	Σ
1A	5D	Ü
1A	5F	Ñ
1A	60	ä
1D, 1E, 1F	23	£
1E, 1F	5B	Ä
1E, 1F	5C	Ö
1E	5D	Å
1F	5D	Ü

ELECTRICAL CHARACTERISTICS

POWER ON OR OFF SEQUENCE. There are no deleterious effects associated with power ON or OFF of this display. However, rapid ON/OFF sequencing is not recommended. Neither data nor power connectors should be connected/disconnected while power is applied.

CAUTION: Do not apply data or strobe signals unless logic power is also applied. Otherwise, input circuits may be damaged.

POWER REQUIREMENTS +4.75 — +5.25VDC @ 1.75 AMPS (8.75 WATTS) MAX., at brightest setting. RISE TIME: Must be less than 100 ms in order for power-on reset circuit to function properly.

INTERFACE SIGNALS Logic assignment: All logic signals discussed in conjunction with this unit abide by the convention of logic "1" is high (>2.4V); logic "0" is low (<0.5V). All interface lines have on-board 10K pull-up resistors (connected to the +5V supply).

UL RECOGNITION

All FLIP Alphanumeric Display Modules have achieved "Recognized Component Status" with Underwriters Laboratories, Inc. [File #E71053 (S)]. A yellow recognition card may be obtained on request from IEE.

ENVIRONMENTAL CHARACTERISTICS

PARAMETER	RATINGS
Projected life at rated operating conditions	80,000 to 100,000+ hours (depending on application and environment)*
Standard operating temperature range - Model 3601-32-032	+32 to 130°F (0 to 55°C)**
Extending operating temperature range - Model 3611-32-032	−40° to +185°F (−40° to +85°C)**
Non-operating temperature range (storage temperature)	−58°F to +185°F (−50°C to +85°C)
Relative humidity (operating and non-operating)	(0 to 95%) non-condensing
Mechanical shock (operating and non-operating)	20G (3 axis)
Vibration (operating and non-operating)	10 to 50 Hz 2mm (peak) (3 axis)
Weight	11.9 oz. (337 gm.)

*NOTE: End-of-life is reached when display tube brightness has decreased to 50% of its initial value.
**NOTE: Normal enclosure design precautions should be taken to ensure reasonable air flow over entire module.

EXTENDED TEMPERATURE RANGE MODELS

Selected FLIP models are available in extended temperature range versions. These models operate from −40 to +185°F (−40 to +85°C) and are suited for applications such as outdoor terminals, field test equipment and other uses in harsh environments. They are designated by a model number beginning with 361X or 371X as opposed to 360X or 370X. The rest of the model number is the same as for the standard temperature version of the display. Thus, the wide temperature version of a 3601-32-032 is 3611-32-032. The two displays are interchangeable, except for their operating temperature range specifications. Consult the factory for availability of specific extended temperature models.

ABSOLUTE MAXIMUM RATINGS

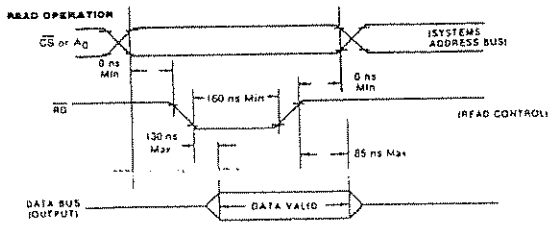
Absolute maximum ratings define stress limitations, which, if exceeded, may permanently damage the FLIP Display Module. These are not continuous duty ratings. For continuous operation the module should be operated within the parameters given under POWER REQUIREMENTS.

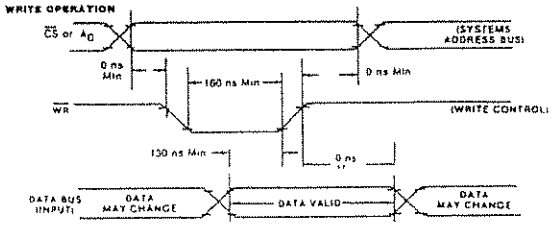
Primary voltage	+5.5VDC
Logic range	−0.5V through +5.5V
RS-232 levels	+15VDC to +3VDC/ −1VDC to −15VDC

EXECUTION TIMES

Character entry	155 μs
Line feed	1 ms
Horizontal scroll	430 μs
Control code entry	115 μs
Reset (Software)	660 μs
Reset (Power-up)	500 ms
Clear	840 μs

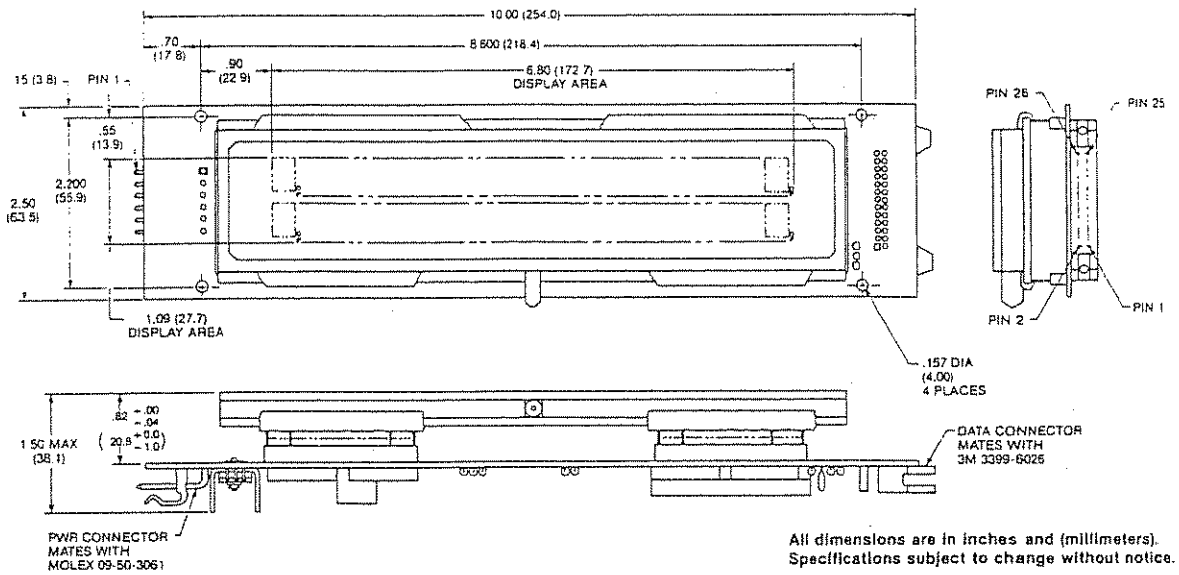
TIMING DIAGRAM





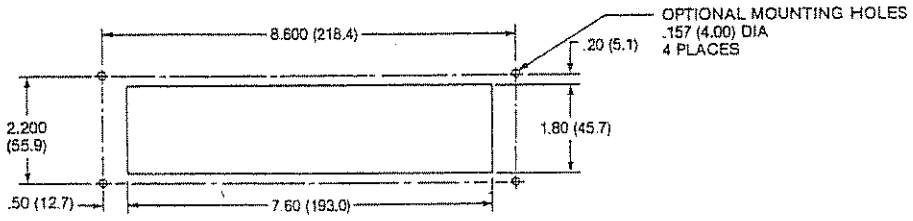
DIMENSIONAL DRAWING

MODEL 36X1-32-032
(2 x 16)



All dimensions are in inches and (millimeters).
Specifications subject to change without notice.

MOUNTING CUTOUT DIMENSIONS



ORDERING INFORMATION

Model 3601-32-032 (standard operating temperature range; +32 to +130 °F, 0 to +55 °C)

Model 3611-32-032 (extended operating temperature range; −40 to +185 °F, −40 to +85 °C)

2 lines of 16 characters

CABLES/CONNECTORS	PART NUMBER
Power connector with cable	25387-XX
Power connector only	25387-99
Data connector with cable	26160-XX
Data connector only	26160-99

XX = length in inches. Standard cable lengths are 18 inches (46cm) and 36 inches (92cm)

FILTERS	PART NUMB
Neutral Gray	28429-01
Blue	28429-02
Aqua	28429-03
Neon Yellow-Orange	28429-04
Green	28429-07
Neutral Gray (circular polarized)	28429-09
Yellow (circular polarized)	28429-10

THE DISPLAY MAKERS

INDUSTRIAL PRODUCTS DIVISION

INDUSTRIAL ELECTRONIC ENGINEERS, INC.
7740 Lemona Ave., Van Nuys, CA 91405
(818) 787-0311 • TWX 910-495-4586 IEE IPD VAN

1. Turn the POWER OFF so that the fan is not operating.

2. Remove the screen by pulling it away from the rear panel. The filter should now be easily removable.

3. Clean the filter and the screen and wipe off the fan blades. (A brush may be helpful in cleaning the filter element)

4. Reinsert the filter and then the screen.

3-3-2 CLEANING

On a six months basis, it may be desirable to remove the top cover and visually inspect the power supply components and to blow out the interior using clean, dry, low pressure air. If the instrument is operating properly it is probably wise NOT to remove the printed circuit boards or to otherwise disturb the interior of the instrument.

3-4 PERFORMANCE CHECKS

The performance of the Phase Standard can be checked on two levels. The first level ensures that the Standard and all of its components are operating properly and in all probability, because of its digital nature, is operating within all of its specifications. The second level is more comprehensive and checks the Standard against all of its detailed specifications. In general, the only equipment required for the first level is an oscilloscope. The second level requires all of the equipment specified in Sub Section 3-4-2.

The level 1 performance checks should be performed when the Phase Standard is first turned on after not having been used for awhile. The level 2 performance checks should be employed for incoming inspection and on an annual basis thereafter to certify its calibrated status. No calibration adjustments should be required during any of these checks. The adjustments, referred to in the latter portions of this section, are to be made only if a repair has been made to the printed circuit board containing the control for the particular adjustment.

3-4-1 BASIC PERFORMANCE OF THE PHASE STANDARD (LEVEL 1)

When the instrument is turned on it goes though its Self Test routine and comes up in the state with 500 Hz, 60° and a 1V output from each channel. If each of the outputs is connected to the input of a dual channel oscilloscope - the two channels in the oscilloscope should be really equal in both amplitude and phase - then using the incrementing controls in the PHASE numeric field, one can get a rapid indication that the Model 5000 is operating correctly.

If the Phase Standard is connected to the oscilloscope to produce a Lissajous pattern, that is one Phase Standard output drives the X axis and the other drives the Y axis, then as the phase is increased from 0° to 360° in 10° increments the pattern should go from a line at 0°, to a circle at 90°, to a line with opposite slope from the original line at 180°, to a circle at 270° and finally back to the original line at 360°. Now if the scales on the oscilloscope are increased one can use 1° phase increments from the Phase Standard and watch the original line expand into an ellipse. In its normal swept mode

the oscilloscope should also indicate that low distortion sine waves of the correct amplitude are present at both Phase Standard outputs.

By varying the amplitude above and below 7.2V one can verify that both the HIGH and the LOW amplifiers are operating. By varying the frequency above and below 6250Hz one can verify that both the HIGH and the LOW filter sections are operating. For frequencies above 5000Hz many oscilloscopes begin to introduce appreciable phase shift between their supposedly well matched channels. Feeding one output from the phase standard to both channels of the oscilloscope will indicate whether any unexpected phase shifts are being produced in it at the frequency in question.

3-4-2 EQUIPMENT REQUIRED (LEVEL 2)

1. Voltmeter, ac/dc, 1mV to 200V, 0.1% accuracy from dc to 100kHz, 1Mohm or greater input impedance.

2. Distortion Analyzer, 0 to -100dB, 10Hz to 100kHz

3. Oscilloscope, dual channel 1MHz minimum bandwidth, 20mV/cm minimum resolution

4. Frequency Counter, 10ppM accuracy, 6 digit resolution, 1Hz to 1MHz

5. Phase Meter, 100mV to 100V, 20Hz to 50kHz, 10m° resolution, 50m° accuracy. Analog output.

6. Tuneable Voltmeter or Wave Analyzer, 1microV sensitivity, 20Hz to 50kHz, 50kohm or greater input impedance

7. Low Loss Capacitors (D less than 50 x 10^{-6} or Q greater than 20,000) over the frequency range of 1kHz to 50kHz, ±5% accuracy. The following approximate capacitance values are required: 3-8pF (variable), 10pF, 100pF, 996pF, and 1000pF.

Multilayer Ceramic Capacitors are recommended for the fixed capacitors since these capacitors generally have sufficiently low losses over the required frequency range. An air dielectric capacitor is recommended for the variable capacitor. The 996pF does not have to have the exact value specified but does need to be 3-4pF smaller than the nominal 1000pF capacitor such that when the variable capacitor is placed in parallel with it, the combined capacitors may be adjusted to equal the 1000pF capacitor.

3-4-3 AMPLITUDE FLATNESS CHECK (LEVEL 2)

If the the AC voltmeter has sufficient accuracy then it may be used to verify that the two outputs are both within their required amplitude tolerances of ±0.5% above 1V rms or ±5mV for outputs between 250mV and 1V over the frequency range from 1Hz to 50000Hz. It may also be used to verify that the two outputs are both within their required amplitude tolerances of ±2.5% above 1V rms or ±25mV for outputs between 250mV and 1V over the frequency range from 50kHz to 100kHz.

Examination of the accuracy specifications for many of the most recently released AC voltmeters indicates that their accuracy varies with the range setting, with the frequency and with the reading. Furthermore outside some frequency range such as 200Hz to 20000Hz their amplitude accuracy specifications are often little if any better than those of the Phase Standard. Therefore, apparent deviations of the Phase Standard from its amplitude specifications must be treated with caution unless one is absolutely sure that the measurement equipment accuracy for the particular range setting and frequency band are at least three times tighter than those of the Phase Standard itself.

More accurate amplitude versus frequency measurements can be obtained by using a Thermal Voltage Converter of the appropriate rating, coupled with a dc voltmeter or with a low drift dc amplifier and a voltmeter. Thermal Voltage Converters are available from Fluke, Ballantine, or Julie Research. The Fluke A-55 series, with its 0.001% ac/dc difference to 1MHz, provides an example of a thermal converter type that, within limits indicated in the next paragraph, may be driven directly by the Model 5000. Since the converter output is proportional to the square of the input, the actual ac amplitude variations are only half of the dc output variations.

Most thermal converters have impedances of 200 ohms/volt. Thus they require a drive current of 5mA. For outputs below 20V the Model 5000 should supply this without difficulty. Thermal converters with voltage ratings below 7V (with impedance below 1400 ohms) should not be used since this low impedance will combine with the effectively reactive output impedance of the Model 5000 to give load induced amplitude variations with frequency that exceed ±0.1%.

Table 3-4-3-1 indicates a number of amplitude and frequency settings for the Phase Standard for which each output should be measured. These measurements should be sufficient to determine that the instrument is operating within its specifications. For each case the specified limits on the measurement are given. With a Thermal Converter use a dc equivalent or convert to percentages.

Table 3-4-3-1 Amplitude Flatness Measurement Points

Voltage Setting	Frequency Setting	Measurement Limits
0.500V	1000Hz	0.495V - 0.505V
0.500V	10000Hz	0.495V - 0.505V
0.500V	50000Hz	0.495V - 0.505V
0.500V	100000Hz	0.475V - 0.525V
7.000V	1000Hz	6.965V - 7.035V
7.000V	10000Hz	6.965V - 7.035V
7.000V	50000Hz	6.965V - 7.035V
7.000V	100000Hz	6.825V - 7.175V
100.0V	1000Hz	99.50V - 100.5V
100.0V	10000Hz	99.50V - 100.5V
100.0V	50000Hz	99.50V - 100.5V
100.0V	100000Hz	97.50V - 102.5V

3-4-4 DISTORTION CHECK (LEVEL 2)

The Phase Standard's sine waves are generated digitally in such a way that their distortion should be both low and constant. The specification limit for the Phase Standard varies from 0.02% (-74dB) from 1 Hz to 500Hz to 0.5% (-46dB) between 75kHz and 100kHz. For many combinations of amplitudes and frequencies the actual distortions may be two to four times (-6dB to -12dB) better than these limits.

Many existing distortion analyzers or spectrum analyzers do not have adequate, distortion free, dynamic range to measure these distortions. Furthermore some such instruments have a maximum input voltage that they can handle without introducing new distortion terms.

From a theoretical viewpoint one expects the type and amount of distortion to vary with both frequency and amplitude settings. For example, for amplitudes just above 7.2V the high voltage amplifier, with its gain of 14, is switched in and it applies this gain to the minimum signal output from the gain controlling DAC. This combination causes the output distortion to be noise like.

On the other hand, at 7.1V the maximum output from the low voltage amplifier exists, and while the measured distortion may be more than 6dB lower, it is apt to have a visible 2nd or 3th harmonic term. As one increases the amplitude above 7.2V, the noise level tends to stay constant while the signal increases so that the percentage distortion falls with increasing signal until eventually harmonic distortion appears and limits the decrease. As the signal level approaches 100V the percentage harmonic distortion terms may increase faster than the signal so that the percentage distortion gets worse with further increases in signal.

In addition to the changes in distortion when the high voltage amplifier is switched in, the distortion changes in level and composition when the Standard switches from the low to the high filter at 6250Hz and, to a lesser extent, when number of increments per cycle are changed. (See Table 2-5-3). Some of the expected changes from these boundary crossings are reduced by other factors. For example, the increased distortion that might be expected from the reduced number of increments in the 50-100kHz region is somewhat reduced by the increased high frequency filtering caused by the high voltage amplifier in the 3.2 to 6.4MHz region where these distortion components occur.

Table 3-4-4-1 indicates the typical distortion and the specified distortion limit for a comprehensive set of amplitude and frequency settings of the Phase Standard. Verification of the items in this table for both the reference and the variable output should be sufficient to determine that the Standard is operating within its distortion specification.

3-4-5 FREQUENCY CHECK (LEVEL 2)

The frequency for the Phase Standard is obtained from a crystal controlled frequency synthesizer. To verify that the Standard is conforming to its frequency specification it is generally sufficient to check a few frequencies in the low band and a few frequencies in the high band via the reference output which should be set to 7.000V. Table 3-4-5-1 indicates a set of frequencies and the measurement limits for each.

Table 3-4-4-1 Distortion Measurement Points

Voltage Setting	Frequency Setting	Distortion Typical	Distortion Limit
1.000V	1000Hz	-80dB	-74dB
1.000V	10000Hz	-72dB	-66dB
1.000V	50000Hz	-66dB	-56dB
1.000V	100000Hz	-66dB	-46dB
7.000V	1000Hz	-82dB	-74dB
7.000V	10000Hz	-74dB	-66dB
7.000V	50000Hz	-70dB	-56dB
7.000V	100000Hz	-64dB	-46dB
10.00V	1000Hz	-76dB	-74dB
10.00V	10000Hz	-72dB	-66dB
10.00V	50000Hz	-70dB	-56dB
10.00V	100000Hz	-66dB	-46dB
100.0V	Same frequencies and distortions as 7.000V		

Table 3-4-5-1 Frequency Measurement Points

Frequency	Limits
111Hz	111.01Hz - 110.99Hz
222Hz	222.02Hz - 221.98Hz
3333Hz	3333.3Hz - 3332.7Hz
5555Hz	5555.6Hz - 5554.4Hz
6250Hz	6250.6Hz - 6249.4Hz
10000Hz	10001Hz - 9999.0Hz
25000Hz	25003Hz - 24997Hz
99980Hz	99990Hz - 99970Hz

3-4-6 PHASE CHECK (LEVEL 2)

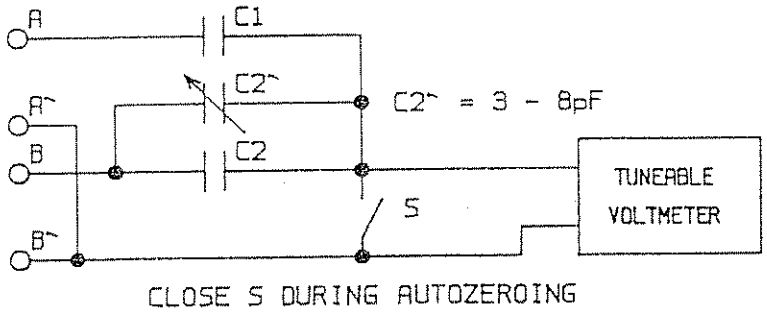
The distortion checks of both outputs indicates that two pure sinewaves are being generated by the Phase Standard. In addition, the internal point by point check of the sine generating ROMs during the SELF TEST mode at turn on indicates that the digital portion of the generation circuitry is functioning properly. This is further confirmed by the observation on the oscilloscope of the phase variation with the phase setting which is outlined in Sub Section 3-4-1.

To further verify that the phase variation with phase setting is correct, set both the reference and the variable outputs to 7.000V, the frequency to 1000Hz and connect the outputs to the Phase Meter which has a dc voltmeter connected to its analog output so as to increase the available resolution. Select a number of phase settings separated by 10m° and verify that the Meter increments 10m° each time the Standard increments 10m°. This should be done on

the vicinity of 10°, 20°, 30°, etc. With the higher resolution meter on the Phase Meter output, verify that the meter reading changes monotonically with 1m° increments of the Standard. As noted in Section 2-3-4, the actual phase increment in the Phase Standard is 1.37 m°; hence about every three m° there will be a pair of adjacent phase setting which should produce the same phase output, for example 1m° and 2m° and then 5m° and 6m°. The normal noise at the Phase Meter output may cause ±1m° of jitter in these reading however they should be adequate to show that the phase incrementing circuitry in the Phase Standard is working correctly.

The absolute phase accuracy now needs to be verified. For any given amplitude settings for the outputs and any frequency setting, it is sufficient to measure the phase difference between the reference and variable outputs at a single phase setting. Since the AUTOZERO function compares the outputs at ±90°, the measurement should be done at a different phase setting to prevent a duplication of errors. For this reason and also for the reason of circuit simplicity, the measurement is performed at 180°.

Figure 3-4-6-1 illustrates the test set-up for performing the measurement. In this set-up, the higher voltage output of the Phase Standard is connected to input A-A' and the lower voltage output is connected to input B-B'. The Tuneable voltmeter is set in frequency to track the Standard. If such a circuit is operated correctly with the Phase Standard, then the phase shift caused by the circuit alone should be less than (D1- D2) microradians. D1 is the dissipation factor of C1 and D2 is the dissipation factor of C2. Thus to ensure that the circuit phase shift is less than 2m° (35 microradians) the difference between the dissipation factors must be less than 35 x 10^{-6}. If both capacitors have Q values above 10,000 (D less than 10^{-4}), then matching of the dissipation factors need only be within 50%. The necessary values of D or Q must be assured over the frequency range of interest, 1kHz to 50 kHz. No special care need be taken in positioning the capacitors since stray capacitance will not upset the phase balance.



AMPLITUDE RATIO	C1	C2
1 : 1	1000pF	996pF
10 : 1	100pF	996pF
100 : 1	10pF	996pF

Figure 3-4-6-1 Phase Measurement Test Set-up

As shown in Fig. 3-4-6-1, different values of C1 must be used for amplitude ratios between the reference and variable outputs of 1:1, 10:1 and 100:1. In each case, the measurement is performed by setting the OFFSET of the Standard to 180°, the PHASE to 0°, the amplitudes to the proper ratio and then incrementing the lower output amplitude slightly, adjusting C2' and incrementing the phase in 1m° steps until a minimum is obtained on the Tuneable Voltmeter (or Wave Analyzer). (In some cases it may be easier to read the same

point on either side of the "valley",perhaps 20-30m° away from the apparent minimum on the selective voltmeter, and then to take the average rather than to determine the minimum directly.) The phase indication on the display is the phase error. At higher frequencies the smaller amplitude may have to be reduced several percent from its nominal value because of the effect of stray capacitance. (The stray capacitance has no effect on the phase measurement.)

NOTE

When the above measurement is performed and the null is obtained, no voltage appears at the input terminals of the tuneable voltmeter; hence, the Phase Standard outputs "see" these terminals as a virtual ground. Consequently, the higher voltage output is loaded by C1 to ground while the lower voltage output is loaded by C2 and C2' to ground. THE MODEL 5000 MUST HAVE THE SAME LOADING WHEN IT IS AUTOZEROING. To accomplish this the switch S has been provided in the test set-up. Switch S should be closed and the Standard should be autozeroed prior to adjusting C2' and incrementing the phase to produce a null. Either the switch must be closed during every amplitude change (the instrument automatically auto-zeros with every amplitude change) or it must be closed after every amplitude adjustment and the AUTO-ZERO button depressed. This will insure the correct internal phase correction process.

To verify that the Standard is operating within its phase specification it is sufficient to check it at a frequency near the top of the low band and a frequency near the top of the high band. 5kHz and 50kHz seem to be reasonable choices. At each frequency, ratios between the reference and the variable output of approximately 1:100, 1:10, 1:1, 10:1 and 100:1 should be checked. If, in addition, the 1:1 ratio is checked with the four combinations of 3.200V and 3.198V, all the capacitors on the autozero board and the cables to the autozero board are also checked.

Table 3-4-6-1 presents a sufficient set of points at which to measure the phase to insure that the Standard is functioning within its phase specification. In each case the specified limits for the measurement as well as typical values are given. If the phase errors exceed these limits the problem can either lie with the Standard or the low loss capacitors in the test set-up. In particular, if the 10:1 case yields an equal but opposite phase error from the 1:10 case, dissipation factor unbalance between the test capacitors is almost a certainty.

Table 3-4-6-1 Phase Measurement Points

Reference Voltage	Variable Voltage	Frequency	Phase Error Limit	Phase Error Typical
3.198V	3.198V	5000Hz	±10m°	±2m°
3.200V	3.198V	5000Hz	±10m°	3±2m°
3.200V	3.200V	5000Hz	±10m°	±2m°
3.198V	3.200V	5000Hz	±10m°	-3±2m°
7.000V	70.00V	5000Hz	±19m°	±5m°
70.00V	7.000V	5000Hz	±19m°	±5m°
1.000V	100.0V	5000Hz	±109m°	±10m°
100.0V	1.000V	5000Hz	±109m°	±10m°

Table 3-4-6-1 Phase Measurement Points (Continued)

3.198V	3.198V	50000Hz	±25m°	±10m°
3.200V	3.198V	50000Hz	±25m°	±10m°
3.200V	3.200V	50000Hz	±25m°	±10m°
3.198V	3.200V	50000Hz	±25m°	±10m°
7.000V	70.00V	50000Hz	±28m°	±15m°
70.00V	7.000V	50000Hz	±28m°	±15m°
1.000V	100.0V	50000Hz	±100m°	±50m°
100.0V	1.000V	50000Hz	±100m°	±50m°

3-5 CALIBRATION ADJUSTMENTS

The adjustments described in the following sub sections are in general not required unless a repair has been made to one of printed circuit boards containing an adjustable potentiometer or capacitor. In such a case, only those controls involved in the repair should be readjusted.

3-5-1 POWER SUPPLY/BACKPLANE MEASUREMENTS AND ADJUSTMENTS (50010: P1)

Section 4-3 lists the various power supply levels and locations. There should be no need to measure these various power supplies unless one suspects trouble with the instrument or unless one wishes reference set of values from the properly working instrument to compare with a latter case where some malfunction is suspected. If these measurements are made then observe all of the precautions of Section 3-2, 4-2 and 4-3.

Only one potentiometer exists on the backplane and its function is to adjust the ±150V supplies. To make this adjustment, set the voltmeter on its 200V dc range, connect it between the case of Q2 and the lead on the left (facing the front) end of C23 and then turn P1 until a reading of 150.0V ±0.1V is obtained.

3-5-2 AUTOZERO BOARD ADJUSTMENTS (50014: C1, C18, P1, P2, P3, P4)

The adjustment of C1 and C18 sets the precise attenuation ratio of the 32 to 1 attenuator in the Reference and Variable channels respectively. These capacitors are set at the factory and should never have to be readjusted unless they themselves are replaced.

To adjust C1, set the voltmeter on its 2V ac range and connect it between the right hand side of R24 and the right hand (GND) test point with the POWER OFF. Now apply POWER, set the Reference Amplitude to 0.199V and press the OPERATE button. Record the reading of the voltmeter which should be approximately 1.04V. Now set the Reference Amplitude to 6.369V and adjust C1 to obtain the value recorded within ± 2%. An exact match may not be possible.

To adjust C18, set the voltmeter on its 2V ac range and connect it between the right hand side of R3 and the right hand (GND) test point with the POWER OFF. Now apply POWER, set the Variable Amplitude to 0.199V and press the OPERATE button. Record the reading of the voltmeter which should be approximately 1.04V. Now set the Variable Amplitude to 6.369V and adjust C18 to obtain the

The adjustment of P1 and P2 reduces the input offset to zero in the Reference and the variable channels respectively. This is accomplished by taking advantage of the property of a multiplier which insures that the output is zero when either input is zero.

To adjust P1 turn the POWER OFF, connect a short circuit across R28, set the oscilloscope on its 20mV/cm ac range and connect it between the test points (GND on the right). Now apply POWER and press the OPERATE button. Adjust P1 until the signal on the oscilloscope is minimized.

To adjust P2 turn the POWER OFF, connect a short circuit across R29, set the oscilloscope on its 20mV/cm ac range and connect it between the test points (GND on the right). Now apply POWER and press the OPERATE button. Adjust P2 until the signal on the oscilloscope is minimized.

The adjustment of P3 and P4 set the full scale gain and the offset of the DAC employed for Analog to Digital conversion. Neither of these adjustments is particularly critical because of the method of Autozeroing. Even if they were significantly out of adjustment, the only effect would be perhaps an additional cycle of Autozeroing.

To adjust P3 turn the POWER OFF, set the voltmeter on its 20V dc range and connect it between the left hand side of R20 and the right hand test point (GND). Now apply POWER, set the Phase at 90.000° and adjust P3 until a voltage reading of -5.35V is obtained within ± 5%.

To adjust P4 turn the POWER OFF, set the voltmeter on its 20V dc range and connect it between the left hand side of R23 and the right hand test point (GND). Now apply POWER, set the Phase at 90.000° and adjust P4 until a voltage reading of 2.68V is obtained within ± 5%.

3-5-3 OUTPUT BOARD ADJUSTMENTS (50007: P1, P2, P3, P4, P5, P6, P7, P8)

There are two Output Boards in each instrument. In general they have identical adjustments. For the purposes of trouble shooting they may be interchanged; however since the instrument was factory calibrated with them in there present positions, best performance is obtained if these positions are maintained.

Potentiometers P1 through P4 are associated with the two signal generating DACs that exist on each Output Board. P1 and P3 are located closest to the DAC and are the full scale adjustments. P2 and P4 are located away from the DAC and are the dc offset controls. Unless one of the DACs is replaced, none of these controls should ever require adjustment.

There are three further dc offset controls, P6, P7 and P8, and two further full scale gain controls, P5 and P9.

P5 is located physically near the top of the board and electrically in the first output amplifier. With the frequency set at 400Hz and the amplitude entered as 7.000V, then P5 may be used to adjust the board's front panel output to 7.000V. At the same frequency, one may now enter an amplitude of 100.0 V and use P9 to adjust the high voltage amplifier gain until the front panel

output is exactly 100.0V. P9 is located below the output amplifier heat sink. Once P9 is located it may be adjusted through one of the slots in the heat sink. The heat sink is at ground potential; however an insulated screwdriver is still recommended.

While P8 and P7 are dc offset controls they are located in the LOW and in the HIGH filter sections respectively; hence one must enter the appropriate frequencies to gain access to them. To remove the offset from the LOW filter, enter 7.000V and 1000Hz and adjust P8 until the dc output at the appropriate front panel output connector reads zero. If the dc meter being used for the measurement operates correctly with the ac signal present then one may make the adjustment in this configuration. If this operation is questionable, then after the entry, one should switch from OPERATE to STANDBY. This removes the ac output by turning off the DAC's but leaves the amplifier and filter configuration that existed in the OPERATE position.

To remove the offset from the high voltage amplifier, enter 7.200V and adjust P6 (at the top of the board) for a dc output value near zero.

To remove the offset from the HIGH filter, enter 7.000V and 7000Hz and adjust P7 (just under the front end of the shield) until the dc output at the appropriate front panel output connector reads zero. There is some variation of the dc offset with frequency (this originates in the DAC's); hence if there is some frequency of particular interest, the HIGH filter dc offset adjustment should be made there. An adjustment to near zero volts should always be possible for the case of 7.000V and 7000Hz. For any combination of higher frequencies and higher ac voltages it should always be possible to adjust the output dc so that it is less than ±0.5% of the rms ac reading; however it may not be possible to adjust the output dc to exactly zero.

IV TROUBLE SHOOTING

4-1 INTRODUCTION

In normal usage none of the defects outlined in this section should ever occur. The procedures for locating possible troubles have been added to cover those rare cases where some accident does occur and immediate restoration of operation is desirable.

If the trouble cannot be eliminated through the use of these service instructions, please write or telephone our Service Department giving the instrument type number, the serial number, the trouble and the steps taken to remedy it. By return mail, or on the telephone, you will receive simple instructions as to the cause and repair of the defect, or authorization to return the instrument for repair or replacement.

Instruments no longer covered by warranty will be repaired or recalibrated after proper customer authorization is received to cover the estimated costs.

After some general servicing considerations, this Section will concern itself with the solution to some of the most common problems which possibly could occur with the Phase Standard.

4-2 GENERAL PRECAUTIONS

One of the most important considerations before attempting to calibrate the Phase Standard is that of SAFETY. It should be constantly kept in mind that the Model 5000 contains both a positive and a negative 150V power supply that runs to several places within the instrument. An interlock, which automatically removes power from the Model 5000 when the top cover is removed, is provided to prevent any accidental contact with the high voltage. The interlock is mounted on the top rear trim directly above the line cord receptacle. When the instrument must be operated with the cover off, the interlock may be bypassed by pushing up the white button which is normally depressed by the closed cover.

In the case where an internal voltage must be measured with the interlock bypassed, the meter or the oscilloscope should be connected with the POWER OFF. The POWER should then be turned ON only after the operator is clear of the interior of the instrument. This is particularly true if the measurement is to be made on a printed circuit board in the card rack. The board should be lifted, the connection made, and the board reinserted, ALL WITH THE POWER OFF. (To remove a board the retention bar must first be removed by removing the two screws holding it in place.)

To make such voltage measurements, it is recommended that the test leads be fashioned with insulated "Easy Hooks" so that they stay firmly in place once they are connected to a component. Alligator clips are not recommended since they have a tendency to "pop off" a component with the possible result of causing a short circuit or bringing an undesired voltage out of the instrument.

4-3 GENERAL APPROACH

If it has been determined that the Phase Standard is not functioning properly, the first thing to do is to try to localize the problem to a particular printed circuit board and then replace the board if this is possible. If it is not possible, then the quickest route to board repair is the systematic replacement of the integrated circuits which are all in sockets. If this approach is taken, care should be exercised not to bend any of the integrated circuit pins when inserting them. This could cause a secondary problem which did not exist at the outset.

Before all the circuits are replaced however, it is sometimes possible to locate the defective component on a board by "feeling it" immediately after the POWER has been turned OFF. Many high speed CMOS circuits fail in such a way that they draw a reasonable amount of power and become HOT. Bipolar integrated circuits which normally run warm should not be checked in this fashion.

If a complete supply of replacement integrated circuits is not available, it is almost always possible to find an identical circuit for any one that is suspect somewhere else in the instrument. If the problem travels when the two identical integrated circuits are interchanged, then the culprit has been uncovered.

In the Phase Standard trouble shooting is made a little easier by the fact that there are two identical channels. If either channel fails while the other is still functioning, then a comparison between the channels usually locates the source of the problem at least to within a particular printed circuit board. In particular, if a channel malfunction exists, the two Output boards (50017) should be interchanged. If the problem moves the board causing the problem has been located. Interchanging integrated circuits between the boards should then narrow it down to a component. If the output boards are not causing the problem, then the trouble most likely exists on the Sine Generator board (50013) or the Timing Generator board (50012). If the problem is in the Variable channel, the simplest thing to do is check the 20bit adder which generates the Variable Phase Output on the Timing Generator Board (see Dwg. No.- 50002). This adder comprises U2, U8, U13, U17 and U22. If the problem still persists the corresponding circuits for the two channels on the Sine Generator board should be systematically interchanged.

In the following Sub Sections a list of possible problems occurring with the Phase Standard are outlined and their solution suggested.

4-3 POWER SUPPLY FAILURE

In response to almost any malfunction the first items to check are the power supply voltages. If any voltage is found to more than 5% different from its nominal value a malfunction should be suspected. If the voltage is low the problem may be with one of the boards and not the power supply. In this case all of the boards in the card rack should be removed (with the POWER OFF) and the supply voltage remeasured. If it returns to its correct value, replace the boards one by one until the offending board is found. It should be noted that

when the boards are removed from the card rack, 5V and the 15V supplies no longer have a common ground; hence a jumper should be placed between the ground (left facing rear) side of C22 and C23.

The low voltages may be measured directly on the corresponding regulator pin which is closest to the Front Panel of the Phase Standard. Table 4-3-1 indicates the regulator for each voltage (see Dwg. No. 50010). The +150V supply may be measured directly on the case of Q2 while the -150V supply may be measured directly on the case of Q1. If a problem exists only with the Buscard, its isolated 5V regulator should be checked. To gain access to the Buscard the rear panel can be dropped by removing the four screws fastening it to the main chassis.

Table 4-3-1 Regulator Voltages

Regulator	Voltage	Boards Used On
U1	+15V	Output, Autozero, Timing Generator
U2	-15V	Output, Autozero
U3	+5V	All but Sine Generator
U4	+5V	Sine Generator
U5	+5V	Display
U6	-5V	Output

If a low voltage supply is found to be in error the most probable culprit is the corresponding regulator. If both the +150V supply and the -150V supply are defective the problem most probably lies with U8, Q2 or Q4. If only the -150V supply is defective, U7, Q1 and Q3 are suspect.

4-4 DISPLAY MALFUNCTION

If the Display does not come on when POWER is applied to the Phase Standard, the first thing to check is the fuse (see 1-4 (15)). If the fuse is not the problem, reapply the POWER, press the OPERATE key and determine whether or not a 1V, 500Hz signal appears at both of the Output terminals. If the signals exist and both the power and the signal connector to the Display are securely in place, the problem most likely exists with the Display. It should be replaced and returned to Clarke-Hess or IEE for repair.

4-5 NO OUTPUT FROM EITHER CHANNEL-ANY FREQUENCY SETTING

If only a large dc voltage and no other output exists at both the Reference and the Variable output terminals the most probable culprits are the VCO in the frequency synthesizer and the gate following it (U23 and U26, Dwg. No. 50002) which produce the CLKLF signal, the divide by two circuits (U32, U35 and U36, Dwg. No. 50003) which produce not CLK, and the various inverters which convert not CLK into CLK (U33, Dwg. No. 50003 and U25, Dwg. No. 50002). These integrated circuits should by checked in the above order and replaced if necessary.

4-6 NO OUTPUT FROM EITHER CHANNEL BELOW 6250Hz

If output signals exist only for frequency settings above 6250Hz the problem lies with either the counter (U24) or the following gate (U26) on the Timing Generator board (Dwg. No. 50002).

4-7 NO FINE CONTROL OF FREQUENCY

If 1Hz steps in frequency cannot be obtained below 6250Hz from the Standard, but output signals exist at both channel outputs which are within a factor of two of the correct frequency, trouble with the frequency synthesizer PLL is indicated. U3, U4 and U15 (Dwg. No. 50002) should be checked and replaced if necessary. If this does not cure the problem the 6.5V at pin 1 of U4 should be checked. If it is not within ±10%, Q1 should be replaced.

4-8 OTHER FREQUENCY PROBLEMS

For any other problems with frequency, U10, U18 and U20 on the Timing Generator board (Dwg. No. 50002) should be checked and replaced if necessary.

4-9 PHASE ANGLE PROBLEMS-NO OTHER SYMPTOMS

If large Phase errors suddenly appear, it must be determined whether they are relative errors or absolute errors. To do this increment the Standard in 1° steps and monitor the output phase angle on a Phase Meter. If the Phase Meter reading changes by 1° with each increment, even though the actual angle is in error, then the error is an absolute one. If the phase meter does not change by 1°, then the error is a relative one.

Relative errors are most likely caused by a failure of one of the circuits which produce the phase shift. These include U2, U8, U9,U13, U14, U17, U20 and U22 on the Timing Generator board (Dwg. No. 50002). If these are not the cause of trouble however, the problem probably exists on the Sine Generator board in one of the channels. In this case, interchanging modules between the two channels until the phase error changes sign, usually leads to the offending circuit.

Absolute phase errors are usually a result of a failure on the Autozero board or the latch U13 on the Microprocessor board. This latch should be checked first and replaced if it is found defective. If in addition to the error, the NOT AUTOZEROED message occurs continuously regardless of amplitude setting, the problem probably lies with one of the DAC's or their drivers (U10, U11, U16, U17 and U18, Dwg. No. 50004). If the message does not occur and the Standard appears to AUTOZERO quickly, then the analog circuits (U1, U2, U3, U4, U5, U6, U7, U8 and U9) should be checked and replaced if necessary. If the effect varies with amplitude setting then the relay drive circuits (U12, U13, U14, U15, U19, U20 and U21) should be checked. If this still does not cure the problem the individual relays (RL1 - RL25) should be checked on the bench. This is best accomplished by removing the relay drivers, applying 5V dc in the proper direction across each coil, and measuring across the switch contacts with an ohmmeter to determine whether or not closure has occurred.

4-10 EXCESS DISTORTION-BOTH CHANNELS

If large amounts of distortion suddenly appear in both channels the problem probably lies with the phase angle generation circuitry on the Timing Generator board. Consequently, U1, U6, U7, U11, U12, U16, U19 and U21 (Dwg. No. 50002) should be checked and replaced if necessary.

V IEEE-488 INTERFACE OPERATION

5-1 INTRODUCTION

This Section deals with the important hardware and software aspects of the IEEE-488 interface operation. In particular, after the interconnection of the instrument with the bus is discussed, the general bus commands, the device dependent commands, the Serial Poll status byte, and the Service Request procedure are considered in detail. In each case examples are given using the Hewlett-Packard Model 85 BASIC.

5-2 HARDWARE CONSIDERATIONS

The Model 5000 is connected to the bus via its 24 pin rear panel connector which conforms to the IEEE-488 1978 standard. Two or more bus cables can be fastened in parallel to the connector such that a number of instruments may be "Daisy chained" onto the bus. Each cable connector should be tightened in place with its knurled screws when it is applied. A maximum of 15 instruments may be connected to the bus and the maximum length of the cable between each instrument is 15 meters. Because of mechanical considerations, a maximum of three cable connectors should be fastened to the rear of any one instrument.

5-3 ADDRESS SELECTION

Each instrument on the bus must be assigned a unique address between 0 and 30 for proper bus operation (31 is used by the bus controller for UNTALK and UNLISTEN commands). The Phase Standard is shipped with its address set to 4 (see Fig. 1-4-2); however, any other address may be set via the ADDRESS switch on the rear panel. Table 5-3-1 indicates the binary settings of the individual positions of the switch for any of the allowed addresses. In the table U implies that the switch section should be up, and D implies that the switch section should be down. It should be noted that the address is read from the switch by the microprocessor on the interface Buscard when power is applied to the Phase Standard; hence each time a new address is set into the ADDRESS switch, the POWER should be turned off for 10 seconds and then reapplied.

5-4 BUS HARDWARE

The bus connector comprises 24 lines of which one is a shield, six are ground connections, eight are data lines (DI01 - DI08), and eight are the control lines (see J2 on Dwg. No.50006). Of the eight control lines, three are for handshaking. These comprise DAV (Data AVailable), NRFD (Not Ready For Data) and NDAC (Not Data ACcepted). The other five lines employed for bus management comprise IFC (InterFace Clear), ATN (ATteNtion), SRQ (Service ReQuest), REN (Remote ENable), and EOI (End Or Identify). For a more detailed discussion of the handshaking lines the reader is referred to IEEE Standard 488-1978. The digital signal on each of the bus lines is inverted such that low is true and high is false. In the Sub Sections to follow a 1 refers to a true situation and thus a low voltage on the bus line.

Table 5-3-1 Switch Settings for Required Addresses

Address	Switch Setting					Address	Switch Setting				
	A0	A1	A2	A3	A4		A0	A1	A2	A3	A4
0	D	D	D	D	D	16	D	D	D	D	U
1	U	D	D	D	D	17	U	D	D	D	U
2	D	U	D	D	D	18	D	U	D	D	U
3	U	U	D	D	D	19	U	U	D	D	U
4	D	D	U	D	D	20	D	D	U	D	U
5	U	D	U	D	D	21	U	D	U	D	U
6	D	U	U	D	D	22	D	U	U	D	U
7	U	U	U	D	D	23	U	U	U	D	U
8	D	D	D	U	D	24	D	D	D	U	U
9	U	D	D	U	D	25	U	D	D	U	U
10	D	U	D	U	D	26	D	U	D	U	U
11	U	U	D	U	D	27	U	U	D	U	U
12	D	D	U	U	D	28	D	D	U	U	U
13	U	D	U	U	D	29	U	D	U	U	U
14	D	U	U	U	D	30	D	U	U	U	U
15	U	U	U	U	D						

5-5 GENERAL BUS COMMANDS

The bus commands which must be implemented by the bus controller (the HP 85 in the examples to follow), fall into three general categories.

1. Uniline commands
2. Multline commands
3. Device dependent commands

The Uniline commands are those commands which are sent over the bus by activating a single bus management line. The multiline commands are those sent as a byte over the eight data lines while the ATN line is True. The device dependent commands are those sent as a byte over the eight data lines while the ATN line is False. Both the multiline and the device dependent commands require proper Handshaking via the three handshaking lines prior to placing a byte on the data lines. Table 5-5-1 summarizes these commands. Only those commands which pertain to the Phase Standard are covered in this Section. In the Table UL indicates Uniline, MU indicates Universal Multiline and MA indicates Multiline Addressed. In the Sub Sections to follow these commands are outlined in more detail and wherever one exists, the corresponding H-P 85 BASIC statement is presented.

5-5-1 UNILINE COMMANDS

The ATN, IFC and the REN commands are sent by the system controller. The SRQ command is requested by any external device. The EOI command may be sent by the controller or the external device, usually with the final data byte. A brief description of each command follows.

1. IFC (Interface Clear). This command sets the bus to a known initial state. In particular the Model 5000 is set to its power on Talker and Listener states. The H-P 85 statement for this command is ABORTIO 7. (7 is the general designation for the bus.) The RESET 7 command also sets

the IFC line true; however it also sets the REN line false which causes all instruments on the bus to exit their REMOTE states.

2. ATN (Attention). This command (true) indicates the presence of a multiline command on the data lines. The absence of this command indicates the presence of a device dependent command on the data lines.

3. SRQ (Service Request). This command is sent by a device requesting service. A Serial Poll is then performed by the controller to determine which device has activated the line.

4. REN (Remote Enable). This command is sent by the controller to set up the interface for remote operation. Generally this command should be sent to the Phase Standard before attempting to program over the bus. It should be noted that this command does not put the instrument in its REMOTE state. The H-P 85 statement for this command is REMOTE 7.

5. EOI (End or Identify). This command is usually sent with the final byte of a multibyte data transmission.

Table 5-5-1 Summary of Bus Commands

Type	Command	Data Line Byte (hex)	ATN Line	Comments
U	IFC (Interface Clear)			Clears Interface
U	ATN (Attention)		True	
U	SRQ (Service Request)			Sent by Device
U	REN (Remote Enable)			Remote Operation
U	EOI (End or Identify)			EOI line True
MA	GTL (Go to Local)	01	True	Local Control
MA	SDC (Selective Device Clr)	04	True	Initializes Device
MA	LLO (Local Lock Out)	11	True	Inhibits Local Sw.
MU	DCL (Device Clear)	14	True	Initializes Device
MU	SPE (Serial Poll Enable)	18	True	Enables S Polling
MU	SPD (Serial Poll Disable)	19	True	Disables S Polling
MU	UNL (Unlisten)	3F	True	Removes Listeners
MU	UNT (Untalk)	5F	True	Removes Talkers
MA	MLA (My Listen Address)	40 + AD*	True	Device Listens

*AD is the address of the instrument in hex (04 for the factory setting of the Phase Standard).

5-5-2 UNIVERSAL COMMANDS (MULTILINE)

Universal Commands are multiline commands which require no addressing and are sent over the data lines with the ATN line true. A brief description of the pertinent commands follows.

1. DCL (Device Clear). This command performs the same function as a hardware RESET. Upon receipt of this command the Phase Standard performs its complete initialization routine as described in Section 1. The H-P 85 statement for this command is CLEAR 7.

2. SPE (Serial Poll Enable). This command is the first step in the serial polling sequence which returns the status byte to the controller.

3. SPD (Serial Poll Disable). This command is sent by the controller to remove all instruments on the bus from the serial poll mode. The H-P 85 statement for the complete Serial Poll procedure is N = SPOLL(704) where N is the status byte returned and 04 is the address of the instrument being polled.

4. UNL (Unlisten). This command simultaneously removes all listeners from the bus. The H-P 85 statement for this command is SEND 7; UNL

5. UNT (Untalk). This command simultaneously removes all talkers from the bus. The H-P 85 statement for this command is SEND 7; UNT

5-5-3 ADDRESSED COMMANDS (MULTILINE)

Each of these commands must be preceded by a Listen command such that only the addressed instrument responds. The Listen command is sent over the bus by sending MLA (My Listen Address) over the data lines with the ATN line true. The Listen command places the addressed instrument in its REMOTE state. The following commands are germane to the Phase Standard.

1. GTL (Go to Local). This command removes the addressed instrument from its REMOTE state. In the Model 5000 it is equivalent to pressing the front panel LOCAL switch except in the case where the Local Lockout state exists. In this case only the GTL command has an effect. The H-P 85 statement for this command is SEND 7;UNL LISTEN04 CMD01 where 04 is the instrument address and 01 is the decimal equivalent of the multiline command. A somewhat more compact statement which performs the same sequence of commands is LOCAL 704.

2. SDC (Selective Device Clear). This command has the same effect on the Phase Standard as the DCL command. The H-P 85 statement for this command is CLEAR 704 where 04 is again the instrument address.

3. LLO (Local Lockout). This command inhibits the front panel LOCAL switch of the Phase Standard from returning the instrument to its local state. The H-P 85 statement for this command is SEND7; UNL LISTEN04 CMD17. To remove the Standard from the LLO state the REN line must be set false. The H-P 85 accomplishes this with the statement RESET 7 which sets the IFC line true and the REN line false. The Standard responds by exiting the REMOTE state.

The H-P 85 contains an addressable REMOTE 704 statement which addresses a particular instrument to listen before setting the REN line true. This command has the effect of setting both the bus and the Phase Standard in its REMOTE state. For this reason this statement is preferable to the REMOTE 7 statement.

5-6 DEVICE DEPENDENT COMMANDS

The device dependent commands are a sequence of bytes sent to the Phase Standard over the data lines with the ATN line false. If these bytes have the

Data Formats outlined below, the Standard responds in exactly the same way it would if the corresponding data entry had been made via the keyboard to set Phase, Frequency, etc. Any number of commands may be grouped together in a single string and sent over the bus at the same time. The Phase Standard however, deals with each entry it receives in sequence and holds off subsequent handshaking with the bus until it has completed all required internal operations. For example if it receives a command to set the Reference Output and the Phase in a single string, it will handshake in the complete set of bytes required for the amplitude command and then stop handshaking with the bus until the actual Reference Output has been set and the Standard has been Autozeroed. It will then handshake in the Phase bytes. If it is desired to expedite this procedure as far as the bus is concerned, the Standard should be placed in STANDBY prior to entering long strings of data, and then placed in OPERATE where a single Autozero operation will occur.

To send a device dependent command over the bus the controller must perform the following sequence.

1. Set ATN true.
2. Address the Model 5000 to Listen.
3. Set ATN false.
4. Send the command string over the data lines one byte at a time.

The H-P 85 handles this sequence in two ways. First is with the BASIC statement SEND 7; UNL LISTEN04 DATA "STRING" where STRING represents the string of command bytes to set the Phase, etc. Second is with the single more compact statement OUTPUT 704; "STRING". The only difficulty with the second form is that the H-P 85 sends a carriage return-line feed at the end of the data sequence and these characters are not recognized by the Phase Standard. The only effect however, is that bit 4 is set in the Status byte returned by the Serial Poll.

5-7 DATA FORMATS

The formats that the data must take to set the various functions of the standard are now considered.

PHASE: P-XXX.XXX where X represents any digit from 0 to 9 inclusive. The - sign may be omitted or replaced by a + sign but all of the digits must be included even if they are 0. Entries are in degrees.

OFFSET: O-XXX.XXX where X represents any digit from 0 to 9 inclusive. The - sign may be omitted or replaced by a + sign but all of the digits must be included even if they are 0. Entries are in degrees.

FREQUENCY: FXXXXX. where X represents any digit from 0 to 9 inclusive. In this case all but one of the X's may be omitted however the decimal point at the end is essential. Entries are in Hertz.

AMPLITUDE: RXXX.X (REFERENCE) or VXXX.X (VARIABLE) where X represents any digit from 0 to 9 inclusive. In this case none of the X's may be omitted even if they are zero but the decimal point may be moved one, two or three places to the left. Entries are in Volts.

STANDBY: S

OPERATE: N

AUTOZERO: Z

SRQ MASK: See 5-9 below.

As an example, consider the case where it is desired to set both the Reference and the Variable Amplitude to 10V, the Frequency to 50Hz, and the Phase to 20°. This can be accomplished with the H-P 85 statement

```
OUTPUT 704; "SR10.00V10.00F50.P020.000N".
```

The leading S and the trailing N are sent to keep the Standard in STANDBY while the string is being sent such that only a single Autozero operation occurs at the end.

5-8 SERIAL POLL

The Status byte returned when the Phase Standard responds to a Serial Poll has the following format.

Bit 0 being set indicates that a hardware error with the keyboard or Buscard exists.

Bit 1 being set indicates that the Standard could not AUTOZERO after an AUTOZERO operation has been performed.

Bit 2 being set indicates that a BOARD OUT error was encountered during initialization.

Bit 3 being set indicates that the initialization Sine Table check of the both channels has failed.

Bit 4 being set indicates that a message was received by the Phase Standard which it did not recognize. This could result if valid data are sent followed by a Carriage Return, Line Feed or both. The data are accepted but the additional bytes are unrecognized.

Bit 5 being set indicates that the Phase Standard is "busy" and is not prepared to handshake. This condition results when the Standard is in the AUTOZERO mode or when it has been sent a Device Clear command and is reinitializing.

Bit 6 being set indicates that the Phase Standard has requested service by activating the SRQ line. This condition results when a bit in the SRQ mask has been set and the corresponding bit in the Status byte occurs.

Bit 7 is not used.

bit 0 through bit 4 are reset when the next valid message is received by the Phase Standard except when the SRQ line has been asserted. In this case the bits are reset following the next Serial poll received by the Standard. Bit 5 is reset at the point that the Standard is no longer "busy", and bit 6 is reset following the next Serial poll request received by the Standard.

As an example consider the following H-P 85 subroutine which AUTOZEROs the Phase Standard, waits for the AUTOZEROING to be complete, checks whether the AUTOZEROING has been successful and then returns to the calling program. If the AUTOZEROING is not successful the subroutine loops and tries again. The looping is continued until a successful AUTOZERO operation has been achieved.

```
10 OUTPUT 704; "Z"
20 N = SPOLL(704)
30 IF BINAND(N,32) = 32 THEN GO TO 20
40 IF BINAND(N,2) = 2 THEN GO TO 10
50 RETURN
```

In the subroutine the instruction on line 10 AUTOZEROs the Standard. The instruction on line 30 checks for a busy condition (bit 5 set) which indicates that the Standard is AUTOZEROING and then loops until this condition no longer exists. The instruction on line 40 checks for the NOT AUTOZEROED condition (bit 1 set) and loops back to 10 to try to AUTOZERO again if it exists.

5-9 SRQ MASK

The SRQ Mask is set by sending MY over the interface to the Standard. In this case Y is a byte whose bits correspond to the bits in the Status byte. Only bit 0 through bit 4 may be masked by placing a 1 in the appropriate bit positions. When the mask is set to recognize a particular bit in the Status byte and this bit is set by the Standard two things occur. Bit 6 in the Status byte is also set and the SRQ line is set true. There is no change in the Status byte until it is cleared by a Serial Poll which also sets the SRQ line false. With the aid of this mask and a controller that responds to a SRQ interrupt, there is no chance of missing a desired bit setting in the Status word.

The following H-P 85 statement sets the SRQ mask to recognize bit 4 in the Serial Poll. In the statement 16 is the decimal equivalent of bit 4 which is converted to a string and combined with "M" to obtain the required MY format.

```
OUTPUT 704; "M" & CHR$(16)
```

6-1 INTRODUCTION

This section contains a list of replacement parts for the Model 5000 Phase Standard and the names of typical manufacturers of such parts. Any of these replacement parts may be obtained from CLARKE-HESS. To obtain a part include:

a. The circuit reference number of the part.

b. The printed circuit board number which contains the part.

c. A brief description of the part.

d. The instrument model and serial number.

e. The quantity desired.

Send the order to CLARKE-HESS at the address on the front of the Instruction Manual.

The parts list is broken up into Sub Sections comprising the chassis parts and the individual printed circuit board parts. In each case circuit reference numbers start from one; hence it is important to include the board number as well as the part number when specifying parts.

6-2 LIST OF MANUFACTURERS

The following list contains the key to the abbreviations in the parts list. The list presents both the name and the address of the manufacturer as well as the code numbers (where available) for the manufacturers as listed in the Federal Supply code for Manufacturers Cataloging Handbooks H4-1 (Name to Code). The list order is Abbreviations/Federal Supply Code Number/Company Name/ Company Address.

Abb.	Code	Company Name	Company Address
AB	01121	Allen-Bradley Corp.	Milwaukee, WI
AM	00779	AMP Inc.	Philadelphia, PA
AD	24355	Analog Devices Inc.	Norwood, MA
AP	60024	Apex Microtechnology Corp.	Tucson, AZ
AR	51167	Aries Electronics Inc.	Hopewell, NJ
BE	70903	Belden Mfg. Company	Chicago, IL
BK	73138	Beckman Instruments Corp. Division of E.I. DuPont	Fullerton, CA

Abb	Code	Company Name	Company Address
BG	22526	Berg Electronics	Camp Hill, PA
BV	30010	Bicc-Vero Electronics Inc.	Trumbull, CT
BB	13919	Burr Brown	Tucson, AZ
BU	71400	Bussman Mfg. Div of McGraw Co.	St. Louis, MO
BY	21604	Buckeye Stamping Co.	Columbus, OH
CH	34423	Clarke-Hess Comm. Res. Corp.	New York, NY
CN	18310	Concord Electronics Corp.	New York, NY
CD	14655	Cornell-Dublier Electric Co.	Newark, NJ
CU	81640	Cutler-Hammer	Los Angeles, CA
DA	91637	Dale Electronics Inc.	Columbus, NE
EM	17117	Electronic Molding Corp.	Woonsocket, RI
FR	07263	Fairchild Camera & Inst. Corp. Semiconductor Division	Mountainview, CA
FX	61429	Fox Electronics	Cape Coral, FL
GE	03508	G.E. Semiconductor Prod. Div.	Syracuse, NY
GY	19112	Garry Div Of Brand-Rex Co.	N.Brunswick, NJ
GO	95348	Gordos Arkansas Inc.	Rogers, AR
HS	83330	Herman H. Smith Inc.	Brooklyn, NY
IE	05464	IEE Inc.	Van Nuys, CA
IC	-	Illinois Capacitor Inc.	Lincolnwood, IL
IN	03674	Intel Corp.	Santa Clara, CA
IF	-	Interfan Inc.	Burlingame, CA
KE	31433	Kemet Capacitors Div. Union Carbide Corp.	Greenville, SC
KY	91833	Keystone Electronics Corp.	New York, NY
MA	37942	P.R. Mallory & Co.,Inc.	Indianapolis, IN
PM	06665	Precision Monolithics Inc.	Santa Clara, CA

Abb	Code	Company Name	Company Address
ME	71590	Mepco-Centralab	West Palm Beach,FL
MX	27264	Molex Inc. Division of E.I. DuPont	Wellington, CT
MO	04713	Motorola Inc.,Semiconductor Prod.	Phoenix, AZ
MW	32897	Murata-Erie North America Inc.	Kingston, CT
NA	27014	National Semiconductor Corp.	Santa Clara, CA
NT	-	National Tel-Tronics	Meadville, PA
OK	-	OKI Mfg. Co.	Japan
QT	-	Quantum Thayer	Houston, TX
RA	02735	RCA Semiconductor Division	Sommerville, NJ
RN	06776	Robinson Nugent Inc.	New Albany, IN
SF	01467	Schaffner EMC Inc.	Union, NJ
SI	08779	Signal Transformer Inc.	Inwood, NY
SG	18324	Signetics Corporation	Sunnyvale, CA
SP	56289	Sprague Electric Co.	North Adams, MA
SW	82389	Switchcraft Inc.	Chicago, IL
TI	01295	Texas Instruments Transistor Products	Dallas, TX
TK	24227	Tek National Inc.	Rochester, NY
TM	18778	Thompson CSF	Canoga Park, CA
TO	-	Toshiba	Japan
TR	84411	TRW Capacitor Division	Ogallala, NE
UC	05397	Union Carbide Corp., Elect. Div.	New York, NY
WE	-	Westlake Capacitor Corp.	Westlake Village,CA

6-3 CHASSIS ASSEMBLY (CH50100)

Circuit Ref.	Description	Mfr.	Part Number
MP1	Case (Flexi-Pak Case)	BY	FP-70-4-16WRM
MP2	Lateral Guide (4/Unit)	BY	MP 40439

Circuit Ref.	Description	Mfr.	Part Number
	Mounting Hardware (L Guides):		
	6-32 x 5/16 BHS Screw (16 Each)	CH	CH50049
	#6 Nuts (16 Each)	CH	CH50058
	#6 Internal Washers (16 Each)	CH	CH50063
	Card Guides (4/Unit)	BY	BPG 45-RN
	Mounting Hardware (C Guides):		
	4-40 x 1/4 BHS Screw (24 Each)	CH	CH50043
	#4 Int. Washer (24 Each)	CH	CH50062
	Rear Panel	CH	CH50021
	Mounting Hardware (Panel):		
	6-32 x 5/16 BHS Screw (4 Each)	CH	CH50049
	3/8" Hex Spacers (4 Each)	KY	1892
	4-40 x 1/4 BHS Screw (4 Each)	CH	CH50043
	Line Cord Receptacle	SF	FN376-2/22
	Mounting Hardware:		
	4-40 x 3/8 BHS Screw (2 Each)	CH	CH50045
	#4 Internal Washer (2 Each)	CH	CH50062
	#4 Nut (2 Each)	CH	CH50057
F1	3/4 A Slow Blow Fuse	BU	3/4MDL
	Line Cord	BE	17251B
	Wiring Harness Assembly	CH	CH50066
	Heat Sink Bracket	CH	CH50023
	Mounting Hardware (Bracket):		
	6-32 x 1/4 RHP Screw (10 Each)	CH	CH50048
X1	Transformer (5V/150V)	CH	CH50028
X2	Transformer (15V/5V)	CH	CH50029
	Mounting Hardware (X1,X2):		
	8-32 x 3/8 BHS Screw (6 Each)	CH	CH50054
	#8 Internal Washer (6 Each)	CH	CH50064
	#8 Nut (6 Each)	CH	CH50059
	Circuit Card Support Bar	CH	CH50038
	Mounting Hardware (Bar):		
	6-32 x 3/8 FHS Screw (2 Each)	CH	CH50046
	Front Panel	CH	CH50019
	3/4" Hex Spacers (9 Each)	KY	1895
	7/8" Hex Spacers (4 Each)	KY	1896
	IEE Display	IE	03601-32-03
	Filter	IE	28429-04
	Display Shield	CH	CH50039
	Mounting Hardware (Shield):		
	1/2" Fiber Spacers (4 Each)	HS	2337
	4-40 x 1 RHS Screw (4 Each)	CH	CH50047
	#4 Intermal Washer (4 Each)	CH	CH50062
	Display Cable Assembly	CH	CH50068

Circuit Ref.	Description	Mfr.	Part Number
	BNC Connectors (2/Unit)	AN	31010
	Output Cable Assembly (2/Unit)	CH	CH50037
SW1	Power on/off switch	SW	PS 670602
	Mounting Hardware:		
	#4 Internal Washer (2 Each)	CH	CH50062
	#4 Nut (2 Each)	CH	CH50057
	Switch Cable Assembly	CH	CH50067
	Interlock switch	CU	SS12ET10-20Y3
	Mounting Hardware (Switch):		
	6-32 x 1/4 BHS Screw (2 Each)	CH	CH50053
	#6 Internal Washer (2 Each)	CH	CH50063
B1	Fan	IF	PM058-115-4B
	Mounting Hardware (Fan):		
	6-32 x 1 1/8 RHS Screw (4 Each)	CH	CH50052
	#6 Int. Washer (4 Each)	CH	CH50063
	#6 Nut (4 Each)	CH	CH50058
	Bracket (Fan)	IF	5501
	Mounting Hardware (Bracket):		
	6-32 x 3/8 RHS Screw (4 Each)	CH	CH50050
	#6 Internal Washer (4 Each)	CH	CH50063
	#6 Nut (4 Each)	CH	CH50058
	Filter (Fan)	IF	5502
	Screen (Fan)	IF	5503

PRINTED CIRCUIT BOARD ASSEMBLIES (CH50100)

Circuit Ref.	Description	Mfr.	Part Number
	Power Supply/Backplane Assembly	CH	CH50110
	Microprocessor Board Assembly	CH	CH50111
	Timing Generator Board Assembly	CH	CH50112
	Sine Generator Board Assembly	CH	CH50113
	Autozero Board Assembly	CH	CH50114
	Buscard Board Assembly	CH	CH50116
	Output Board Assembly	CH	CH50117
	Keyboard Assembly	CH	CH50118

INTERCONNECTING CABLES (CH50100)

	10 Conductor Ribbon Cable (Buscard)	CH	CH50025
	20 Conductor Ribbon Cable (Keyboard)	CH	CH50027
	24 Conductor Ribbon Cable (Display)	CH	CH50026

6-4 POWER SUPPLY/BACKPLANE BOARD ASSEMBLY (CH50110)

BOARD, CONNECTORS AND SOCKETS (CH50110)

Circuit Ref.	Description	Mfr.	Part Number
	Backplane Circuit Board	CH	CH50010
J1	6 Pin Molex Connector	MX	09-67-1063
J2	10 Pin Berg Socket	BG	65863-301
J6	26 Pin Berg Socket	BG	65863-305
J7	20 Pin Berg Socket	BG	65863-019
J8	64 Pin Socket(Female)	BV	905-72185
J9	64 Pin Socket(Female)	BV	905-72145
J10	64 Pin Socket(Female)	BV	905-72185
J11	64 Pin Socket(Female)	BV	905-72185
J12	64 Pin Socket(Female)	BV	905-72185
J13	64 Pin Socket(Female)	BV	905-72185
J14	64 Pin Socket(Female)	BV	905-72185
	14 Pin Socket (1 Each)	RN	ICN-143-S3T
	8 Pin Socket (1 Each)	RN	ICN-083-S3T

RESISTORS (CH50110)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	3,320	1%	1/4W	DA	RN55D
R2	301,000	1%	1/4W	DA	RN55D
R3	4,020	1%	1/4W	DA	RN55D
R4	301,000	1%	1/4W	DA	RN55D
R5	301,000	1%	1/4W	DA	RN55D
R6	3,320	1%	1/4W	DA	RN55D
R7	301,000	1%	1/4W	DA	RN55D
R8	4,020	1%	1/4W	DA	RN55D
R9	11,000	1%	1/4W	DA	RN55D
R10	499	1%	1/4W	DA	RN55D
R11	13,700	1%	1/4W	DA	RN55D
R12	301,000	1%	1/4W	DA	RN55D
R13	499	1%	1/4W	DA	RN55D
R14	11,000	1%	1/4W	DA	RN55D
R15	100,000	5%	1/2W	AB	RC02GF104J
R16	100,000	5%	1/2W	AB	RC02GF104J

CAPACITORS (CH50110)

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C1	0.1uF	25V	20%	Disk	ME	UK25-104
Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C2	0.1uF	25V	20%	Disk	ME	UK25-104
C3	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C4	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C6	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C7	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C8	2200uF	16V	20%	Elect	IC	228RMR016M
C9	1000uF	35V	20%	Elect	IC	108RSM035M
C10	1000uF	35V	20%	Elect	IC	108RSM035M
C11	1000uF	35V	20%	Elect	IC	108RSM035M
C12	1000uF	35V	20%	Elect	IC	108RSM035M
C13	2200uF	16V	20%	Elect	IC	228RMR016M
C15	0.01uF	50V	20%	Disk	ME	CK50-103
C16	300pF	100V	5%	Mica	CD	DM15F301J
C17	0.01uF	250V	10%	Disk	ME	DD103
C18	0.01uF	250V	10%	Disk	ME	DD103
C19	0.22uF	250V	10%	Film	TM	MC224
C20	0.22uF	250V	10%	Film	TM	MC224
C21	100uF	250V	20%	Elect	IC	107TTA250A
C22	100uF	250V	20%	Elect	IC	107TTA250A
C23	15,000uF	16V	20%	Elect	IC	159TTA016A
C24	15,000uF	16V	20%	Elect	IC	159TTA016A
C25	470pF	100V	5%	Mica	CD	DM15F471J
C26	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C27	22uF	25V	20%	Tant	KE	T362B226M025AS
C28	10uF	20V	20%	Tant	SP	196D106X0020JA1
C29	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S

POTENTIOMETERS (CH50110)

Circuit Ref.	Description	Mfr.	Part Number
P1	5,000 Ohm Single Turn Trimmer	BK	72PMR5K

TRANSISTORS AND DIODES (CH50110)

Circuit Ref.	Description	Mfr.	Part Number
Q1	High Voltage Transistor	MO	2N3738
Q2	High Voltage Transistor	MO	2N6424
	Mounting Hardware (Q1,Q2):		
	6-32 x 3/8 RHS Screw (4 Each)	CH	CH50050
	#6 Washer (4 Each)	CH	CH50060
	#6 Internal Washer (4 Each)	CH	CH50063
	#6 Nut (4 Each)	CH	CH50058
Q3	High Voltage Transistor	MO	2N5416
Q4	High Voltage Transistor	MO	2N3439
D1	Power Diode	MO	1N4004
D2	Power Diode	MO	1N4004
D3	Power Diode	MO	1N4004
D4	Power Diode	MO	1N4004
D5	Power Diode	MO	1N4004
D6	Power Diode	MO	1N4004
D7	Power Diode	MO	1N4005
D8	Power Diode	MO	1N4005
D9	Power Diode	MO	1N4005
D10	Power Diode	MO	1N4005
D11	Power Diode	MO	1N5400
D12	Power Diode	MO	1N5400
D13	Power Diode	MO	1N4004
D14	Power Diode	MO	1N4004
D15	Power Diode	MO	1N4004
D16	Power Diode	MO	1N4004
D17	Power Diode	MO	1N4004
D18	Power Diode	MO	1N4004

INTEGRATED CIRCUITS (CH50110)

Circuit Ref.	Description	Mfr.	Part Number
U1	+15V Regulator	MO	MC7815CT
U2	-15V Regulator	MO	MC7915CT
U3	+5V Regulator	MO	MC7805CT
U4	+5V Regulator	MO	MC7805CT
U5	+5V Regulator	MO	MC7805CT
	Mounting Hardware (Regulators):		
	Insulating Strip (5 Each)	TK	SR07-54
	Shoulder Washer (5 Each)	CH	CH50069
	4-40 x 3/8 BHS Screw (5 Each)	CH	CH50045
	#4 Internal Washer (5 Each)	CH	CH50062
	#4 Nut (5 Each)	CH	CH50057

Circuit Ref.	Description	Mfr.	Part Number
U6	-5V Regulator	MO	MC7905CT
U7	General Purpose Operational Amplifier	FR	uA741
U8	Voltage Regular	FR	uA723

6-5 MICROPROCESSOR BOARD ASSEMBLY (CH50111)

BOARD, CONNECTORS AND SOCKETS (CH50111)

Circuit Ref.	Description	Mfr.	Part Number
	Microprocessor Circuit Board	CH	CH50011
J1	64 Pin Edge Connector	BV	905-72184
	Mounting Hardware (Connector):		
	2-56 x 1/2 RHS Screw (2 Each)	CH	CH50042
	#2 Internal Washer (2 Each)	CH	CH50061
	#2 Nut (2 Each)	CH	CH50056
	14 Pin Socket (1 Each)	RN	ICN-143-S3T
	16 Pin Socket (4 Each)	RN	ICN-163-S3T
	20 Pin Socket (4 Each)	RN	ICN-203-S3T
	24 Pin Socket (5 Each)	RN	ICN-246-S4T
	40 Pin Socket (1 Each)	RN	ICN-406-S4-G

RESISTORS (CH50111)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	100	1%	1/4W	DA	RN55D
R2	10,000	1%	1/4W	DA	RN55D
R3	100,000	Resistor Pack		TR	C10-1-104G

CAPACITORS (CH50111)

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C1	22pF	100V	5%	Mica	CD	DM15F220J
C2	22pF	100V	5%	Mica	CD	DM15F220J
C3	2.2uF	16V	20%	Tant	KE	T368B225K050AS
C4	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C6	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C7	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C8	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C9	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C10	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C11	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C12	22uF	25V	20%	Tant	KE	T362B226M025AS

INTEGRATED CIRCUITS (CH50111)

Circuit Ref.	Description	Mfr.	Part Number
U1	Timer	OK	82C53
U2	Microprocessor	OK	80C85A
U3	Input Latch	NA	74HCT573
U4	EPROM A (Program)	CH	50031
U5	EPROM B (Program)	CH	50032
U6	EPROM C (Program)	CH	50033
U7	2k Static Ram	NA	6116
U8	Dual D Flip Flop	RA	CD74HCT74E
U9	3 to 8 Decoder	SG	74HCT138
U10	3 to 8 Decoder	SG	74HCT138
U11	3 to 8 Decoder	SG	74HCT138
U12	3 to 8 Decoder	SG	74HCT138
U13	Input Latch	NA	74HCT573
U14	Bus Driver	SG	74HCT541
U15	Bus Driver	SG	74HCT541

DIODES AND MISCELLANEOUS (CH50111)

Circuit Ref.	Description	Mfr.	Part Number
XL1	Crystal 5.1850MHz	FX	FOX 051
D1	High Speed Diode	TI	1N914B

6-6 TIMING GENERATOR BOARD ASSEMBLY (CH50112)

BOARD, CONNECTORS AND SOCKETS (CH50112)

Circuit Ref.	Description	Mfr.	Part Number
	Timing Generator Circuit Board	CH	CH50012
	64 Pin Edge Connector	BV	905-72185
	Mounting Hardware (Connector):		
	2-56 x 1/2 RHS Screw (2 Each)	CH	CH50042
	#2 Internal Washer (2 Each)	CH	CH50061
	#2 Nut (2 Each)	CH	CH50056
	8 Pin Socket (1 Each)	RN	ICN-083-S3T
	14 Pin Socket (4 Each)	RN	ICN-143-S3T
	16 Pin Socket (17 Each)	RN	ICN-163-S3T
	20 Pin Socket (4 Each)	RN	ICN-203-S3T

RESISTORS (CH50112)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	2000	1%	1/4W	DA	RN55D
R2	10,000	1%	1/4W	DA	RN55D
R3	12,100	1%	1/4W	DA	RN55D
R4	10,000	1%	1/4W	DA	RN55D
R5	10,000	1%	1/4W	DA	RN55D
R6	1,000	1%	1/4W	DA	RN55D
R7	10,000	1%	1/4W	DA	RN55D
R8	12,100	1%	1/4W	DA	RN55D
R9	49,900	1%	1/4W	DA	RN55D

CAPACITORS (CH50112)

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C1	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C2	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C3	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C4	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C6	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C7	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C8	300pF	200V	5%	Mica	CD	DM15-301J
C9	33pF	200V	5%	Mica	CD	DM15-330J
C10	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C11	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C12	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C13	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C14	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C15	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C16	1uF	100V	10%	Film	QT	MPC13 1.0
C17	1uF	100V	10%	Film	QT	MPC13 1.0
C18	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C19	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C20	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C21	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C22	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C23	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C24	33pF	100V	5%	Mica	CD	DM15-330J
C25	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C26	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C27	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C28	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C29	0.01uF	50V	10%	Disk	ME	CK50-103
C30	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C31	22uF	25V	20%	Tant	KE	T362B226MO25AS
C32	22uF	25V	20%	Tant	KE	T362B226MO25AS

TRANSISTORS, DIODES AND MISCELLANEOUS (CH50112)

Circuit Ref.	Description	Mfr.	Part Number
Q1	General Purpose Transistor	MO	2N3904
D1	High Speed Diode	TI	1N914B
XL1	2.3040MHz Crystal	CH	CH50070
BP1	Beeper	MA	MCP320B2

INTEGRATED CIRCUITS (CH50112)

Circuit Ref.	Description	Mfr.	Part Number
U1	4 Bit Adder	TI	74LS283
U2	4 Bit Adder	TI	74LS283
U3	8 Bit Latch	SG	74HCT574
U4	Frequency Syntehsizer	TO	TC9125bp
U5	Dual D Flip Flop	RA	CD74HCT74E
U6	6 Bit Latch	SG	74HCT174

Circuit Ref.	Description	Mfr.	Part Number
U7	4 Bit Adder	TI	74LS283
U8	4 Bit Adder	TI	74LS283
U9	8 Bit Latch	SG	74HCT574
U10	3 to 8 Decoder	SG	74HCT238
U11	4 Bit Adder	TI	74HLS283
U12	6 Bit Latch	SG	74HCT174
U13	4 Bit Adder	TI	74LS283
U14	8 Bit Latch	SG	74HCT574
U15	FET Input Operational Amplifier	PM	OP17GZ
U16	4 Bit Adder	TI	74LS283
U17	4 Bit Adder	TI	74LS283
U18	3 to 8 Decoder	SG	74HCT238
U19	6 Bit Latch	SG	74HCT174
U20	8 Bit Latch	SG	74HCT574
U21	4 Bit Adder	TI	74LS283
U22	4 Bit Adder	TI	74LS283
U23	Voltage Controlled Oscillator	TI	74LS624N
U24	Divide By Ten Counter	MO	74F160
U25	Hex Inverter	SG	74HCT04
U26	Triple 3 Input NAND Gate	MO	MC74F10N

6-7 SINE GENERATOR BOARD ASSEMBLY (CH50113)

BOARD, CONNECTORS AND SOCKETS (CH50113)

Circuit Ref.	Description	Mfr.	Part Number
	Sine Generator Circuit Board	CH	CH50013
J1	64 Pin Edge Connector	BV	905-72184
J2	64 Pin Edge Connector	BV	905-72184
	Board Shield	CH	CH50040
	Mounting Hardware (Connector):		
	2-56 x 1/2 RHS Screw (4 Each)	CH	CH50042
	#2 Internal Washer (4 Each)	CH	CH50061
	#2 Nut (8 Each)	CH	CH50056
	14 Pin Socket (4 Each)	RN	ICN-143-S3T
	16 Pin Socket (10 Each)	RN	ICN-163-S3T
	20 Pin Socket (W/Cap)(16 Each)	GY	619-20-CC-D.1
	24 Pin Socket (6 Each)	RN	ICN-246-S4T

RESISTORS (CH50113)

Circuit Ref.	Ohms	Description Percent	Power	Mfr.	Part Number
R1	499	1%	1/4W	DA	RN55D
R2	499	1%	1/4W	DA	RN55D
R3	4,750	1%	1/4W	DA	RN55D
R4	4,750	1%	1/4W	DA	RN55D
R5	100	1%	1/4W	DA	RN55D
R6	100	1%	1/4W	DA	RN55D

CAPACITORS (CH50113)

Circuit Ref.	Value	Description Voltage	Percent	Type	Mfr.	Part Number
C1	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C2	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C3	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C4	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C6	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C7	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C8	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C9	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C10	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C11	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C12	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C13	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C14	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C15	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S

TRANSISTORS (CH50113)

Circuit Ref.	Description	Mfr	Part Number
Q1	High Speed PNP Transistor	MO	MPS 3640
Q2	High Speed PNP Transistor	MO	MPS 3640

INTEGRATED CIRCUITS (CH50113)

Circuit Ref.	Description	Mfr.	Part Number
U1	8 Bit Latch	SG	74HCT574
U2	8 Bit Latch	SG	74HCT564

Circuit Ref.	Description	Mfr.	Part Number
U3	8 Bit Latch	SG	74HCT574
U4	8 Bit Latch	SG	74HCT564
U5	PROM (MSB Sine Data)	CH	CH50034
U6	PROM (LSB Sine Data)	CH	CH50035
U7	PROM (Sine Correction)	CH	CH50036
U8	4 Bit Adder	TI	74LS283
U9	4 Bit Adder	TI	74LS283
U10	4 Bit Adder	TI	74LS283
U11	4 Bit Adder	TI	74LS283
U12	8 Bit Latch	SG	74HCT574
U13	8 Bit Latch	SG	74HCT564
U14	8 Bit Latch	SG	74HCT574
U15	8 Bit Latch	SG	74HCT564
U16	8 Bit Latch	SG	74HCT574
U17	8 Bit Latch	SG	74HCT564
U18	8 Bit Latch	SG	74HCT574
U19	8 Bit Latch	SG	75HCT564
U20	PROM (MSB Sine Data)	CH	CH50034
U21	PROM (LSB Sine Data)	CH	CH50035
U22	PROM (Sine Correction)	CH	CH50036
U23	4 Bit Adder	TI	74LS283
U24	4 Bit Adder	TI	74LS283
U25	4 Bit Adder	TI	74LS283
U26	4 Bit Adder	TI	74LS283
U27	8 Bit Latch	SG	74HCT574
U28	8 Bit Latch	SG	74HCT564
U29	8 Bit Latch	SG	74HCT574
U30	8 Bit Latch	SG	74HCT564
U31	Quad D Flip Flop	SG	74HCT175
U32	Quad N and Gate	SG	74F00
U33	Hex Inverter	SG	74HCT04
U34	Quad D Flip Flop	SG	74HCT175
U35	Quad Nor Gate	SG	74HCT02
U36	Dual D Flip Flop	RA	CD74HCT74E

6-8 AUTO ZERO BOARD ASSEMBLY (CH50114)

BOARD, CONNECTORS AND SOCKETS (CH50114)

Circuit Ref.	Description	Mfr.	Part Number
	Auto Zero Circuit Board	CH	CH50014
J1	Phone Jack	NT	333-51
J2	Phone Jack	NT	333-51

Circuit Ref.	Description	Mfr.	Part Number
TP1	Test Point	CN	09-9094-1-04
TP2	Test Point	CN	09-9094-1-04
J3	64 Pin Edge Connector	BV	905-72184
	Mounting Hardware (Connector):		
	2-56 x 1/2 RHS Screw (2 Each)	CH	CH50042
	#2 Internal Washer (2 Each)	CH	CH50061
	#2 Nut (2 Each)	CH	CH50056
	Capacitor Shield	CH	CH50041
	Mounting Hardware (Shield):		
	3/8" Hex Spacer	KY	1892
	#6 Washer	CH	CH50060
	#4 Internal Washer (2 Each)	CH	CH50062
	4-40 x 1/4 RHS Screw (2 Each)	CH	CH50044
	8 Pin Socket (8 Each)	RN	ICN-083-S3T
	14 Pin Socket (4 Each)	RN	ICN-143-S3T
	16 Pin Socket (1 Each)	RN	ICN-163-S3T
	18 Pin Socket (2 Each)	RN	ICN-183-S3T
	20 Pin Socket (6 Each)	RN	ICN-203-S3T

RESISTORS (CH50114)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	100,000	1%	1/4W	DA	RN55D
R2	499,000	1%	1/4W	DA	RN55D
R3	6,980	1%	1/4W	DA	RN55D
R4	499,000	1%	1/4W	DA	RN55D
R5	316	1%	1/4W	DA	RN55D
R6	316	1%	1/4W	DA	RN55D
R7	1,910	1%	1/4W	DA	RN55D
R8	10,000	1%	1/4W	DA	RN55D
R9	10,000	1%	1/4W	DA	RN55D
R10	499	1%	1/4W	DA	RN55D
R11	301,000	1%	1/4W	DA	RN55D
R12	1,000	1%	1/4W	DA	RN55D
R13	1,000	1%	1/4W	DA	RN55D
R14	88,700	1%	1/4W	DA	RN55D
R15	12,100	1%	1/4W	DA	RN55D
R16	1,910	1%	1/4W	DA	RN55D
R17	6,040	1%	1/4W	DA	RN55D
R18	301,000	1%	1/4W	DA	RN55D
R19	39,200	1%	1/4W	DA	RN55D
R20	15,000	1%	1/4W	DA	RN55D

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R21	301,000	1%	1/4W	DA	RN55D
R22	1,000	1%	1/4W	DA	RN55D
R23	40,200	1%	1/4W	DA	RN55D
R24	6,980	1%	1/4W	DA	RN55D
R25	100,000	1%	1/4W	DA	RN55D
R26	10,000	1%	1/4W	DA	RN55D
R27	100	1%	1/4W	DA	RN55D
R28	82 M	1%	1/4W	DA	RN55D
R29	82 M	1%	1/4W	DA	RN55D
R30	30.1	1%	1/4W	DA	RN55D

CAPACITORS (CH50114)

Circuit Ref.	Value	Description Voltage	Percent	Type	Mfr	Part Number
C1	2-8pF	200V	5 %	Ceramic	ME	MAV 02 D06
C2	91pF	200V	5 %	Ceramic	CD	DM15-910J
C3-C17	1,500pF	50V	5%	Ceramic	ME	MA67 152J
C18	2-8pF	200V	5%	Ceramic	ME	MAV 02 D06
C19	91pF	50V	5%	Ceramic	CD	DM15-910J
C20-C34	1,500pF	50V	5%	Ceramic	ME	MA67 152J
C35	0.01uF	50V	10%	Disk	ME	CK50-103
C36	0.1uF	25V	20%	Disk	ME	UK25-104
C37	0.1uF	25V	20%	Disk	ME	UK25-104
C38	0.1uF	25V	20%	Disk	ME	UK25-104
C39	0.1uF	25V	20%	Disk	ME	UK25-104
C40	0.1uF	25V	20%	Disk	ME	UK25-104
C41	0.1uF	25V	20%	Disk	ME	UK25-104
C42	1uF	100V	10%	Film	QT	MPC131.0
C43	0.1uF	25V	20%	Disk	ME	UK25-104
C44	0.1uF	25V	20%	Disk	ME	UK25-104
C45	0.01uF	50V	10%	Disk	ME	CK50-103
C46	0.01uF	50V	10%	Disk	ME	CK50-103
C47	0.01uF	50V	10%	Disk	ME	CK50-103
C48	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C49	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C50	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C51	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C52	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C53	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C54	0.01uF	50V	10%	Disk	ME	CK50-103
C55	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C56	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C57	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C58-C70	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S

POTENTIOMETERS (CH50114)

Circuit Ref.	Description	Mfr.	Part Number
P1	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P2	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P3	10,000 Ohm Ten Turn Trimmer	AB	85X10K
P4	10,000 Ohm Ten Turn Trimmer	AB	85X10K

TRANSISTORS AND MISCELLANEOUS (CH50114)

Circuit Ref.	Description	Mfr.	Part Number
Q1	General Purpose NPN Transistor	MO	2N3904
RL1-RL25	SPST Relay (25 Each)	GO	741-A-10

INTEGRATED CIRCUITS (CH50114)

Circuit Ref.	Description	Mfr.	Part Number
U1	General Purpose Operational Amplifier	FR	UA741
U2	FET Input Operational Amplifier	PM	OP17GZ
U3	Multiplier	MO	1594
U4	Operational Amplifier	FR	UA741
U5	FET Input Operational Amplifier	PM	OP17GZ
U6	Operational Amplifier	FR	UA741
U7	FET Input Operational Amplifier	PM	OP17GZ
U8	Comparator	FR	LM311N
U9	Operational Amplifier	PM	OP27GZ
U10	D/A Converter	AD	AD7541AKN
U11	D/A Converter	AD	AD7541AKN
U12	Relay Driver	TI	SN75492N
U13	Relay Driver	TI	SN75492N
U14	Relay Driver	TI	SN75492N
U15	Relay Driver	TI	SN75492N
U16	8 Bit Latch	SG	74HCT574
U17	8 Bit Latch	SG	74HCT574
U18	8 Bit Latch	SG	74HCT574
U19	8 Bit Latch	SG	74HCT574
U20	8 Bit Latch	SG	74HCT574
U21	8 Bit Latch	SG	74HCT574

6-9 BUS CARD ASSEMBLY (CH50116)

BOARD, CONNECTORS AND SOCKETS (CH50116)

Circuit Ref.	Description	Mfr.	Part Number
	Buscard Circuit Board	CH	CH50016
	Mounting Hardware (Board):		
	4-40 x 1/4 RHS Screw (4 Each)	CH	CH50044
	#4 Internal Washer (4 Each)	CH	CH50062
J1	10 Pin Berg Socket	BG	65496-055
J2	Amp (Champ) 24 Pin		
	Bus Connector	AM	552224-1
	Connector Hardware	AM	552862-1
	6 Pin Socket (2 Each)	RN	ICN-063-S3T
	14 Pin Socket	RN	ICN-143-S3T
	16 Pin Socket (2 Each)	RN	ICN-163-S3T
	20 Pin Socket (2 Each)	RN	ICN-203-S3T
	40 Pin Socket (2 Each)	EM	10640-01-446

RESISTORS (CH50116)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	10,000	1%	1/4W	DA	RN55D
R2	100,000	1%	1/4W	DA	RN55D
R3	332	1%	1/4W	DA	RN55D
R4	3,320	1%	1/4W	DA	RN55D
R5	332	1%	1/4W	DA	RN55D
R6	10,000	1%	1/4W	DA	RN55D
R7	100,000	1%	1/4W	DA	RN55D
R8	3,320	1%	1/4W	DA	RN55D

CAPACITORS (CH50116)

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C1	10uF	20V	20%	Tant	SP	196D106X0020JA1
C2	0.1uF	16V	20%	Disk	ME	DD310-L608Y58
C3	10uF	20V	20%	Tant	SP	196D106X0020JA1
C4	22pF	100V	5%	Mica	CD	DM15-220J
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C7	10uF	20V	20%	Tant	SP	196D106X0020JA1

MISCELLANEOUS (CH50116)

Circuit Ref.	Description	Mfr.	Part Number
XL1	Crystal 5.1850MHz	FX	5.1850MHz
SW1	5 Position Dip Switch	AR	1015-25

INTEGRATED CIRCUITS (CH50116)

Circuit Ref.	Description	Mfr.	Part Number
U1	Hex Inverter	MO	MC14049BCP
U2	Optical Isolator	TI	TIL 126
U3	Optical Isolator	TI	TIL 126
U4	5V Regulator	FR	MC7805CT
U5	Hex Inverter	MO	MC14049BCP
U6	Microprocessor	CH	CH50071
U7	Quad and GATE	MO	MC14081BCP
U8	Bus Controller	TI	TMS9914
U9	Bus Driver	TI	SN75161AN
U10	Bus Driver	TI	SN75160AN

6-10 OUTPUT BOARD ASSEMBLY (CH50117)

BOARD, CONNECTORS AND SOCKETS (CH50117)

Circuit Ref.	Description	Mfr.	Part Number
	Output Circuit Board	CH	CH50017
J1	64 Pin Edge Connector	BV	905-72184
	Mounting Hardware (Connector):		
	2-56 x 1/2 RHS Screw (2 Each)	CH	CH50042
	#2 Internal Washer (2 Each)	CH	CH50061
	#2 Nut (2 Each)	CH	CH50056
J2	Phone Jack	NT	333-51
	8 Pin Socket (6 Each)	RN	ICN-083-S3T
	14 Pin Socket (3 Each)	RN	ICN-143-S3T
	18 Pin Socket (1 Each)	RN	ICN-183-S3T
	20 Pin Socket (4 Each)	RN	ICN-203-S3T
	24 Pin Socket (2 Each)	RN	ICN-243-S3T

RESISTORS (CH50117)

Circuit Ref.	Description Ohms	Percent	Power	Mfr.	Part Number
R1	274,000	1%	1/4W	DA	RN55D
R2	10 M	1%	1/4W	DA	RN55D
R3	274,000	1%	1/4W	DA	RN55D
R4	10 M	1%	1/4W	DA	RN55D
R5	30.1	1%	1/4W	DA	RN55D
R6	619	1%	1/4W	DA	RN55D
R7	412	1%	1/4W	DA	RN55D
R8	649	1%	1/4W	DA	RN55D
R9	649	1%	1/4W	DA	RN55D
R10	100	1%	1/4W	DA	RN55D
R11	5,110	1%	1/4W	DA	RN55D
R12	4,220	1%	1/4W	DA	RN55D
R13	6,810	1%	1/4W	DA	RN55D
R14	4,530	1%	1/4W	DA	RN55D
R15	100	1%	1/4W	DA	RN55D
R16	4.7	5%	1/4W	AB	CB
R17	4.7	5%	1/4W	AB	CB
R18	15.0	1%	1/4W	DA	RN55D
R19	15.0	1%	1/4W	DA	RN55D
R20	49.9	1%	1/4W	DA	RN55D
R21	49.9	1%	1/4W	DA	RN55D
R22	15.0	1%	1/4W	DA	RN55D
R23	49.9	1%	1/4W	DA	RN55D
R24	49.9	1%	1/4W	DA	RN55D
R25	37.4	1%	1/4W	DA	RN55D
R26	200	1%	1/4W	DA	RN55D
R27	243	1%	1/4W	DA	RN55D
R28	13,700	1%	1/4W	DA	RN55D
R29	200,000	1%	1/4W	DA	RN55D
R30	10,000	1%	1/4W	DA	RN55D
R31	49.9	1%	1/4W	DA	RN55D
R32	4,020	1%	1/4W	DA	RN55D
R33	100	1%	1/4W	DA	RN55D
R35	100	1%	1/4W	DA	RN55D
R36	1,000	1%	1/4W	DA	RN55D
R37	10,000	1%	1/4W	DA	RN55D
R38	2,550	1%	1/4W	DA	RN55D
R39	130	1%	1/4W	DA	RN55D
R40	130	1%	1/4W	DA	RN55D
R41	10.0	1%	1/4W	DA	RN55D

Circuit Ref.	Ohms	Description Percent	Power	Mfr.	Part Number
R42	750	1%	1/4W	DA	RN55D
R43	10.0	1%	1/4W	DA	RN55D
R44	100	1%	1/4W	DA	RN55D

CAPACITORS (CH50117)

Circuit Ref.	Value	Description Voltage	Percent	Type	Mfr.	Part Number
C1	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C2	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C3	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C4	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C5	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C6	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C7	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C8	220pF	100V	5%	Mica	CD	DM15-221J
C9	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C10	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C11	10uF	35V	20%	Tant	SP	196D106X9035
C12	10uF	35V	20%	Tant	SP	196D106X9035
C13	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C14	0.1uF	25V	20%	Disk	ME	UK25-104
C15	0.1uF	25V	20%	Disk	ME	UK25-104
C16	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C17	10uF	16V	20%	Tant	SP	196D106X9035
C18	10uF	25V	20%	Tant	SP	196D106X9035
C19	10uF	25V	20%	Tant	SP	196D106X9035
C20	0.1uF	25V	20%	Disk	ME	UK25-104
C21	0.1uF	25V	20%	Disk	ME	UK25-104
C22	0.1uF	25V	20%	Disk	ME	UK25-104
C23	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C24	10uF	35V	20%	Tant	SP	196D106X9035
C25	10uF	35V	20%	Tant	SP	196D106X9035
C26	10uF	35V	20%	Tant	SP	196D106X9035
C27	0.1uF	25V	20%	Tant	ME	UK25-104
C28	0.1uF	25V	20%	Tant	ME	UK25-104
C29	1000pF	100V	5%	Mica	CD	DM15-102J
C30	620pF	100V	5%	Mica	CD	DM15-621J
C31	0.1uF	25V	20%	Disk	ME	UK25-104
C32	0.1uF	25V	20%	Disk	ME	UK25-104
C33A,B	1000pF	100V	5%	Mica	CD	DM15-102J
C34	180pF	100V	5%	Mica	CD	DM15-181J

Circuit Ref.	Description Value	Voltage	Percent	Type	Mfr.	Part Number
C35	0.1uF	25V	20%	Disk	ME	UK25-104
C36	0.1uF	25V	20%	Disk	ME	UK25-104
C37	1000pF	100V	5%	Mica	CD	DM15-102J
C38	820pF	100V	5%	Mica	CD	DM15-821J
C39	0.1uF	25V	20%	Disk	ME	UK25-104
C40	0.1uF	25V	20%	Disk	ME	UK25-104
C41A,B	1000pF	100V	5%	Mica	CD	DM15-102J
C42	270pF	100V	5%	Mica	CD	DM15-271J
C43	0.1uF	25V	20%	Disk	ME	UK25-104
C44	0.1uF	25V	20%	Disk	ME	UK25-104
C45	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C46	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C47	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C48	30pF	100V	5%	Mica	CD	DM15-300J
C49	10uF	35V	20%	Tant	SP	196D106X9035
C50	10uF	35V	20%	Tant	SP	196D106X9035
C51	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C52	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C53	0.22uF	250V	10%	Epoxy	TM	MC224
C54	0.22uF	250V	10%	Epoxy	TM	MC224
C55	39pF	100V	5%	Mica	CD	DM15-390J
C56	39pF	100V	5%	Mica	CD	DM15-390J
C57	270pF	100V	5%	Mica	CD	DM15-271J
C58	0.068uF	50V	10%	Film	QT	MLR 683F1
C59	0.1uF	16V	20%	Disk	ME	DD310-L608Y5S
C60	22pF	100V	5%	Mica	CD	DM15-220J
C61	620pF	100V	5%	Mica	CD	DM15-621J
C62	220pF	100V	5%	Mica	CD	DM15-221J
C63	1.2pF	1000V	20%	Disk	SP	TC1R2 1000NPO

POTENTIOMETERS (CH50117)

Circuit Ref.	Description	Mfr.	Part Number
P1	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P2	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P3	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P4	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P5	500 Ohm Ten Turn Trimmer	AB	85X500
P6	100,000 Ohm Ten Turn Trimmer	AB	85X100K
P7	10,000 Ohm Ten Turn Trimmer	AB	85X10K
P8	10,000 Ohm Ten Turn Trimmer	AB	85X10K
P9	500 Ohm Ten Turn Trimmer	AB	85X500

TRANSISTORS, DIODES AND MISCELLANEOUS (CH50117)

Circuit Ref.	Description	Mfr.	Part Number
Q1	High Speed PNP Transistor	MO	MPS 2369
Q2	High Speed PNP Transistor	MO	MPS 2369
Q3	High Speed PNP Transistor	MO	MPS 2369
Q4	High Speed PNP Transistor	MO	MPS 2369
Q5	High Speed NPN Transistor	MO	MPS 3640
Q6	High Speed NPN Transistor	MO	MPS 3640
D1	High Speed Diode	TI	1N914B
D2	High Speed Diode	TI	1N914B
D3	High Speed Diode	TI	1N914B
D4	High Speed Diode	TI	1N914B
D5	High Speed Diode	TI	1N914B
D6	High Speed Diode	TI	1N914B
D7	High Speed Diode	TI	1N914B
D8	High Speed Diode	TI	1N914B
RL1	SPST Relay	GO	741-A-10
RL2	SPST Relay	GO	741-A-10
RL3	SPST Relay	GO	741-A-10
RL4	SPST Relay	GO	741-A-10
RL6	SPST Relay	GO	741-A-10
RL7	SPST Relay	GO	741-A-10
L1	39uH Inductor	DA	IM-2-39-10%
L2	39uH Inductor	DA	IM-2-39-10%

INTEGRATED CIRCUITS (CH50117)

Circuit Ref.	Description	Mfr.	Part Number
U17	D/A Converter	BB	DAC 706KH
U18	D/A Converter	BB	DAC 706KH
U19	Quad Switch	SG	HCT4016E
U20	Low Noise Operational Amplifier	PM	OP37GZ
U21	Low Noise Operational Amplifier	PM	OP37GZ
U22	FET Input Operational Amplifier	PM	OP17GZ
U23	Low Noise Operational Amplifier	PM	OP37GZ
U24	FET Input Operational Amplifier	PM	OP17GZ
U25	FET Input Operational Amplifier	PM	OP17GZ
U26	D/A Converter	AD	AD7541AKN
U27	Low Noise Operational Amplifier	PM	OP37GZ
U28	High Voltage Operational Amplifier	AP	PA84S
	Mounting Hardware (PA84):		

Circuit Ref.	Description	Mfr.	Part Number
	Heat Sink	AP	HS-01
	6-32 x 1/2 RHS Screw (2 Each)	CH	CH50051
	#6 Washer (2 Each)	CH	CH50060
	#6 Internal Washer (2 Each)	CH	CH50063
	#6 Nut (2 Each)	CH	CH50058
U29	8 Bit Latch	SG	74HCT573
U30	8 Bit Latch	SG	74HCT573
U31	8 Bit Latch	SG	74HCT574
U32	8 Bit Latch	SG	74HCT574
U33	Relay Driver	NA	DS75492
U34	Hex Inverter	SG	74HCT04

6-11 KEYBOARD ASSEMBLY (CH50118)

BOARD, CONNECTORS AND SOCKETS (CH50118)

Circuit Ref.	Description	Mfr.	Part Number
	Keyboard Circuit Board	CH	CH50030
	Mounting Hardware (Board):		
	4-40 x 1/4 RHS Screw (9 Each)	CH	CH50044
	#4 Internal Washer (9 Each)	CH	CH50062
	14 Pin Socket (1 Each)	RN	ICN-143-S3T
	20 Pin Socket (2 Each)	RN	ICN-203-S3T
J1	20 Pin Berg (rear mounted)	BG	65863-019

RESISTORS (CH50118)

Circuit Ref.	Ohms	Description Percent	Power	Mfr.	Part Number
R1	100,000	Resistor Pack		TR	C10-1-104G
R2	270	5%	1/4W	AB	RC07GF271J

CAPACITORS (CH50118)

Circuit Ref.	Value	Description Voltage	Percent	Type	Mfr.	Part Number
C1	0.1uF	25V	20%	Disk	CE	UK25-104

DIODES AND MISCELLANEOUS (CH50118)

Circuit Ref.	Description	Mfr.	Part Number
LD1	Red Light Emitting diode	CM	CM4-43B
SW1 - SW26	Switchcraft Momentary DPST	SW	982A06

INTEGRATED CIRCUITS (CH50118)

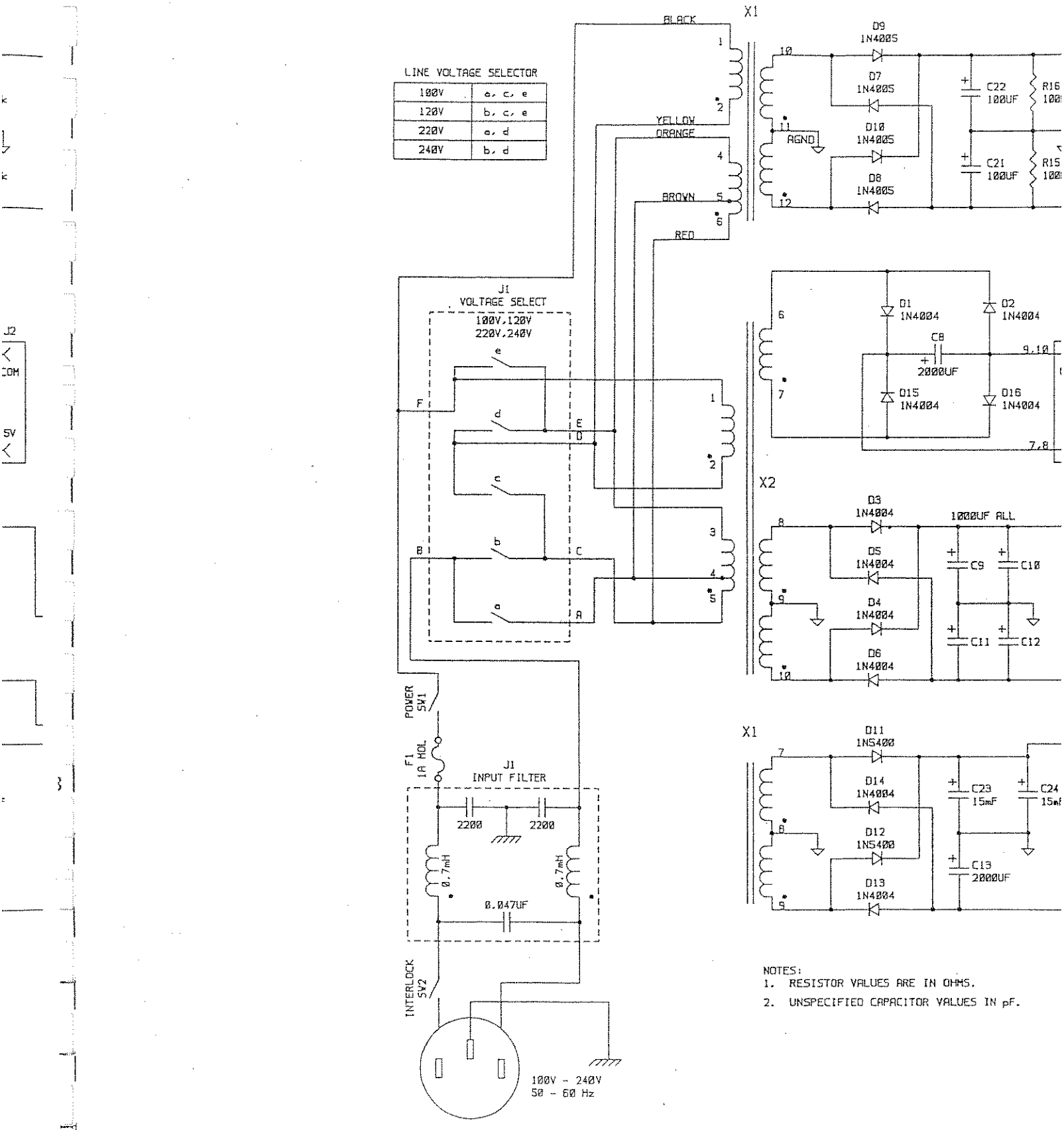
Circuit Ref.	Description	Mfr.	Part Number
U1	Quad NAND gate	TI	74LS03
U2	8 Bit Latch	SG	74HCT573
U3	8 Bit Latch	SG	74HCT574

7-1 INTRODUCTION

This Section contains the schematic diagrams and the component location diagrams for the Model 5000 Phase Standard. Table 7-1-1 provides a listing of these drawings.

Table 7-1-1. Listing of Drawings.

Drawing Number	Description
50000	Power Supply Schematic Diagram
50001	Microprocessor Schematic Diagram
50002	Timing Generator Schematic Diagram
50003	Sine Generator Schematic Diagram
50004	Autozero Board Schematic Diagram
50006	Buscard Schematic Diagram
50007	Output Board Schematic Diagram
50008	Keyboard Schematic Diagram
50009	Backplane Interconnections
50010	Power Supply/Backplane Board Layout
50011	Microprocessor Board Layout
50012	Timing Generator Board Layout
50013	Sine Generator Board Layout
50014	Autozero Board Layout
50015	Keyboard Board Layout
50016	Buscard Board Layout
50017	Output Board Layout
50018	Chassis Layout

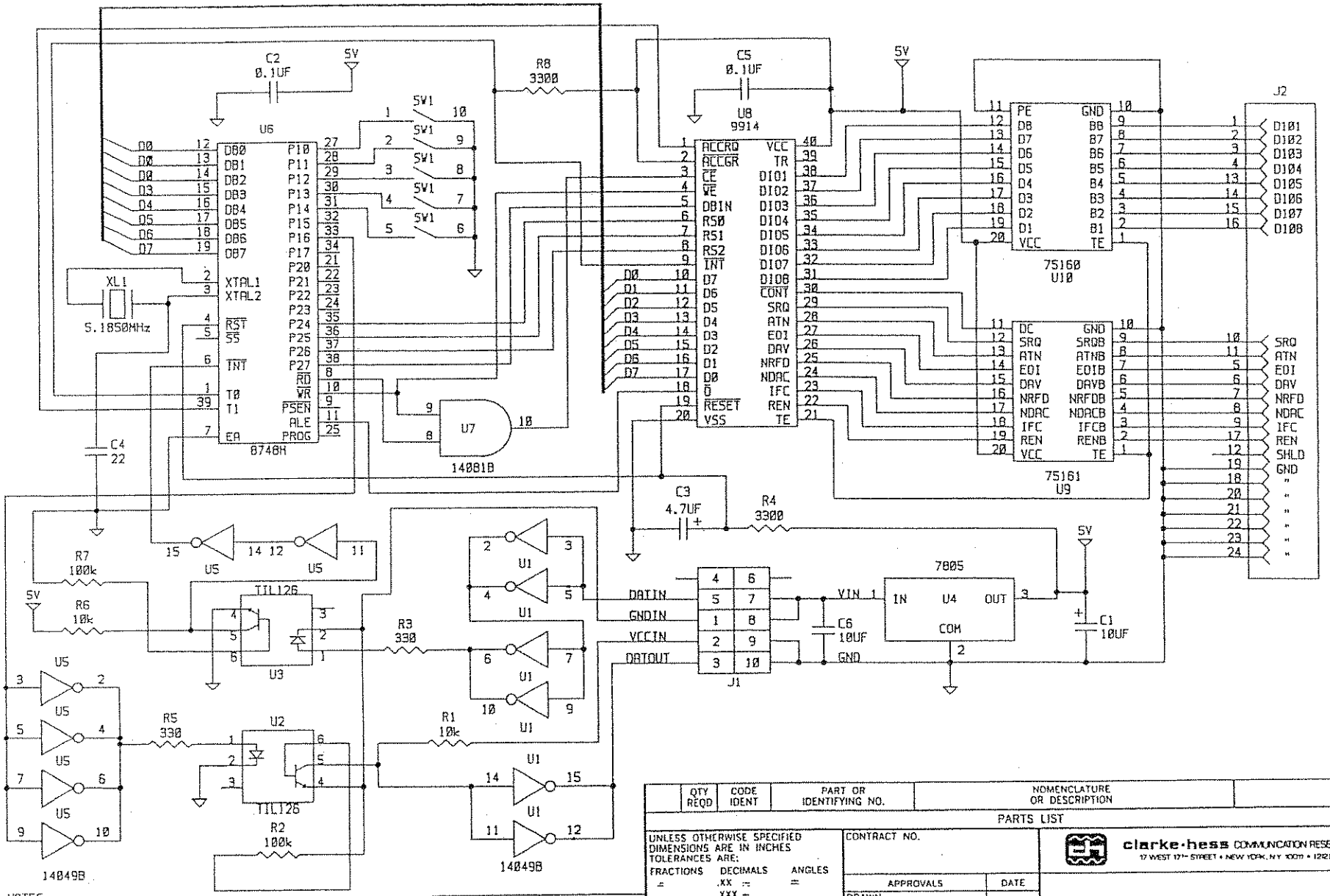


NOTES:
1. RESISTOR VALUES ARE IN OHMS.
2. UNSPECIFIED CAPACITOR VALUES IN pF.

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE | SHEET OF

ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:

1. RESISTOR VALUES ARE IN OHMS.
2. UNSPECIFIED CAPACITOR VALUES IN pF.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

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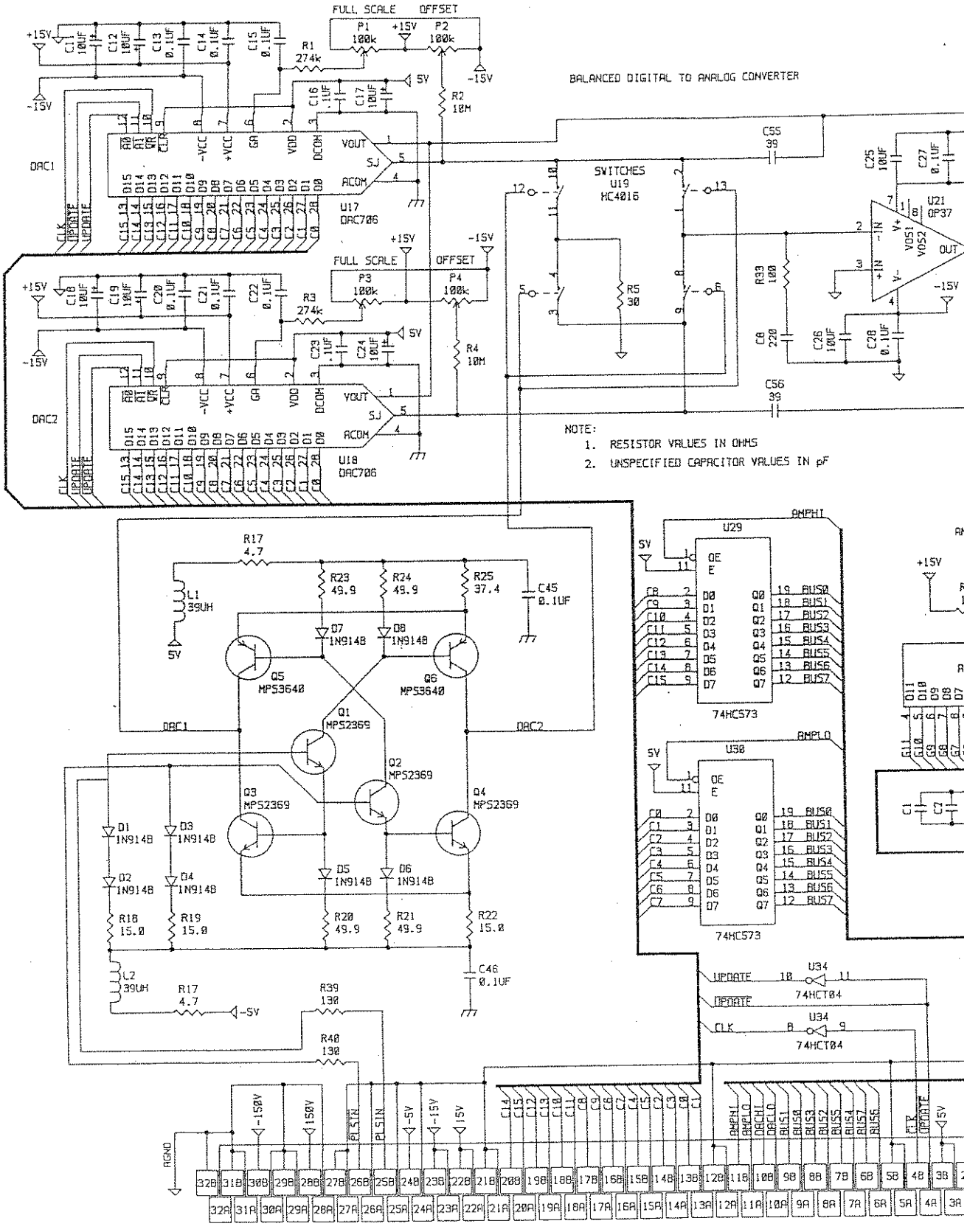
BUSCARD SCHEMATIC DIAGRAM

SIZE	CODE IDENT NO.	DRAWING NO.
C		50006


BALANCED DIGITAL TO ANALOG CONVERTER
FULL SCALE
OFFSET
P1 100k
P2 100k
P3 100k
P4 100k
R1 274k
R2 10M
R3 274k
R4 10M
R5 30
DAC1
DAC2
U17 DAC706
U18 DAC706
SWITCHES U19 HC4016
U21 OP37
C55 39
C56 39
R33 100
C8 220
C25 10UF
C26 10UF
C27 0.1UF
C28 0.1UF
NOTE:
1. RESISTOR VALUES IN OHMS
2. UNSPECIFIED CAPACITOR VALUES IN pF
R17 4.7
L1 39UH
R23 49.9
R24 49.9
R25 37.4
C45 0.1UF
D7 1N914B
D8 1N914B
Q5 MPS3640
Q6 MPS3640
Q1 MPS2369
Q2 MPS2369
Q3 MPS2369
Q4 MPS2369
D1 1N914B
D2 1N914B
D3 1N914B
D4 1N914B
D5 1N914B
D6 1N914B
R18 15.0
R19 15.0
R20 49.9
R21 49.9
R22 15.0
C46 0.1UF
L2 39UH
R39 130
R40 130
AMPHI
AMPLO
U29
U30
74HCS73
74HCT04
U34
UPDATE
CLK
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
AGND

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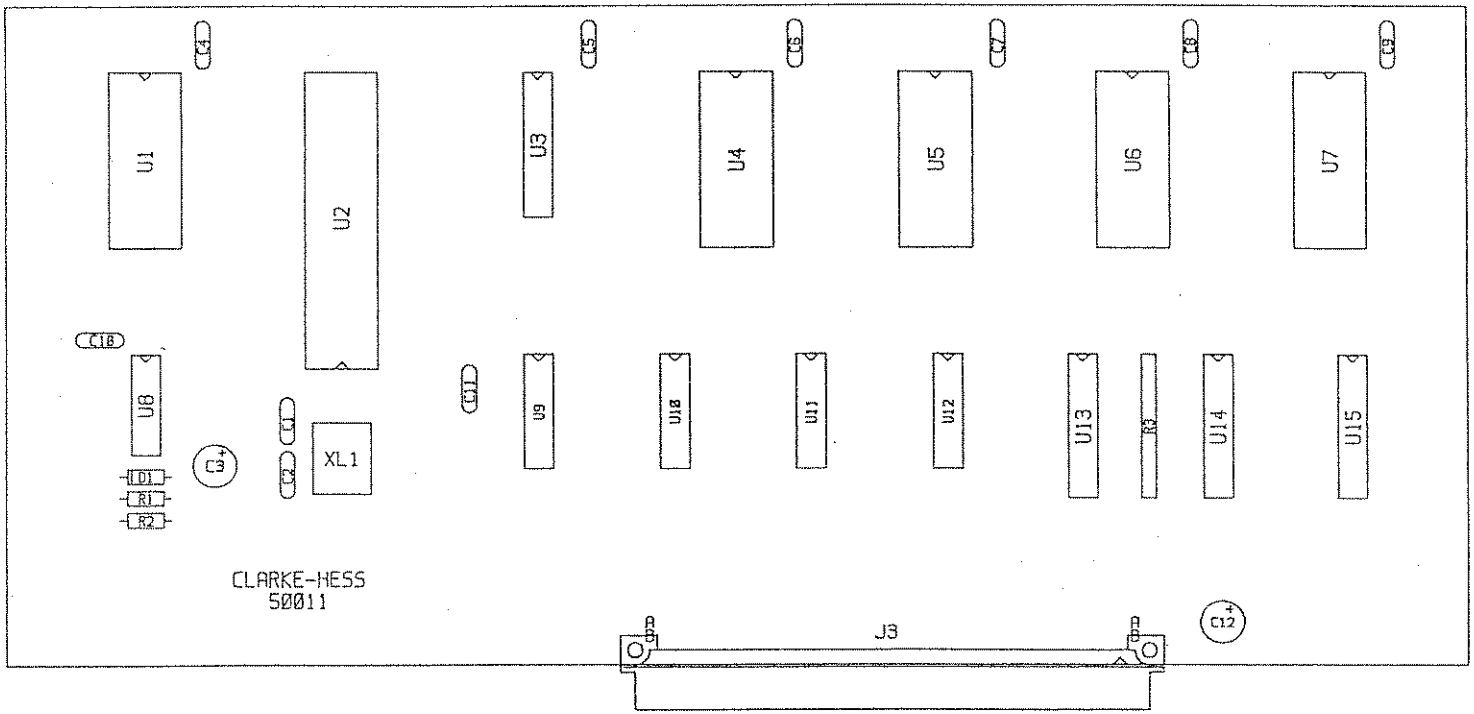
ZONE DESCR



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PARTS LIST

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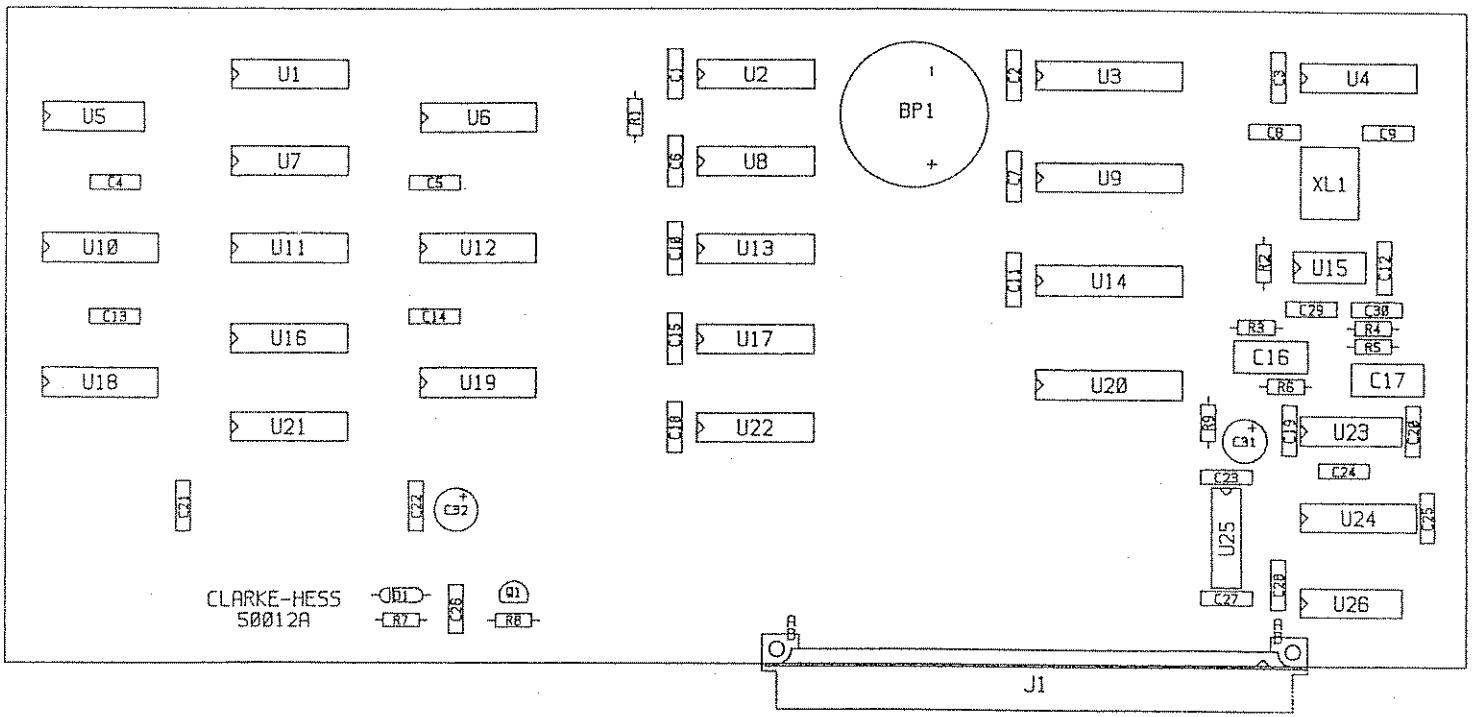
MICROPROCESSOR BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50011

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET OF

ZONE	DESCR.		D



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

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TOLERANCES ARE:
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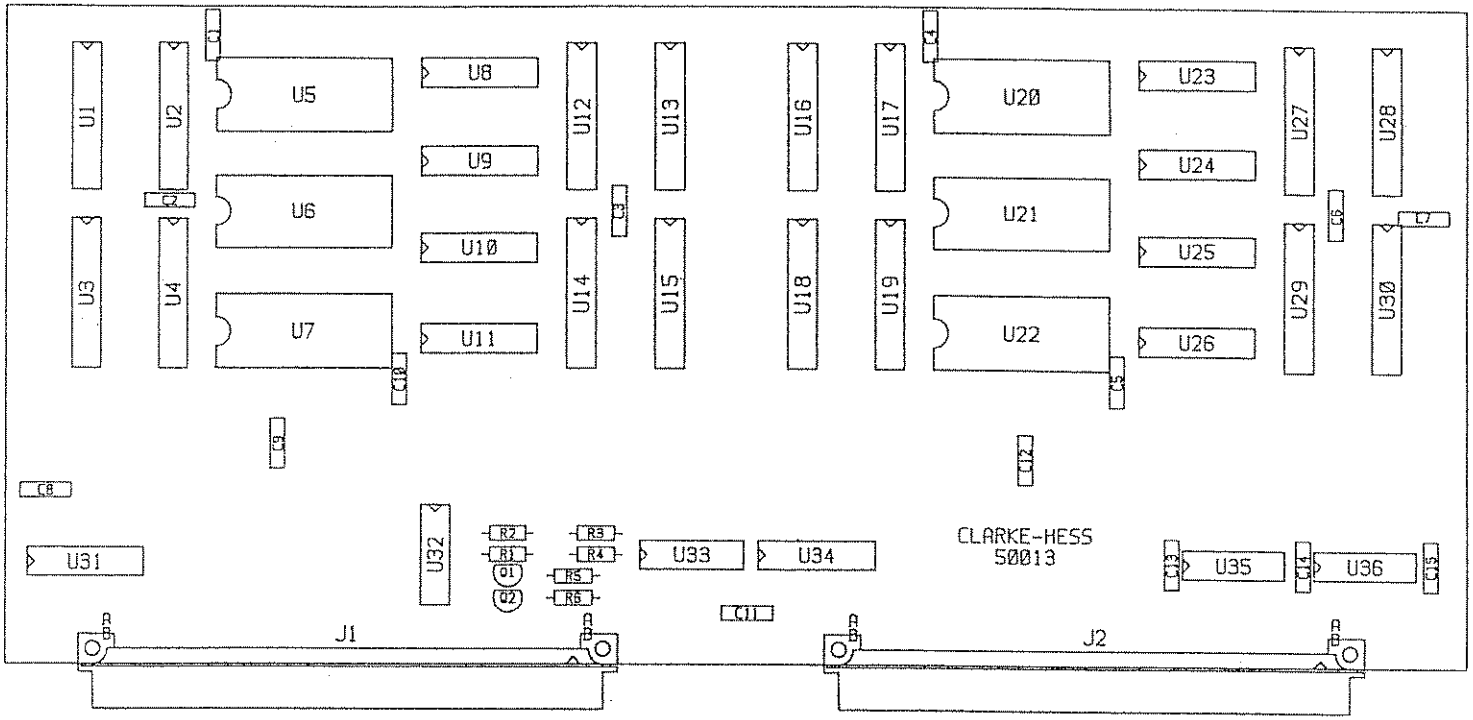
TIMING GENERATOR BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50012

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET OF

ZONE	LTR	REV DESCRIPTION	DATE	APPROVED



	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

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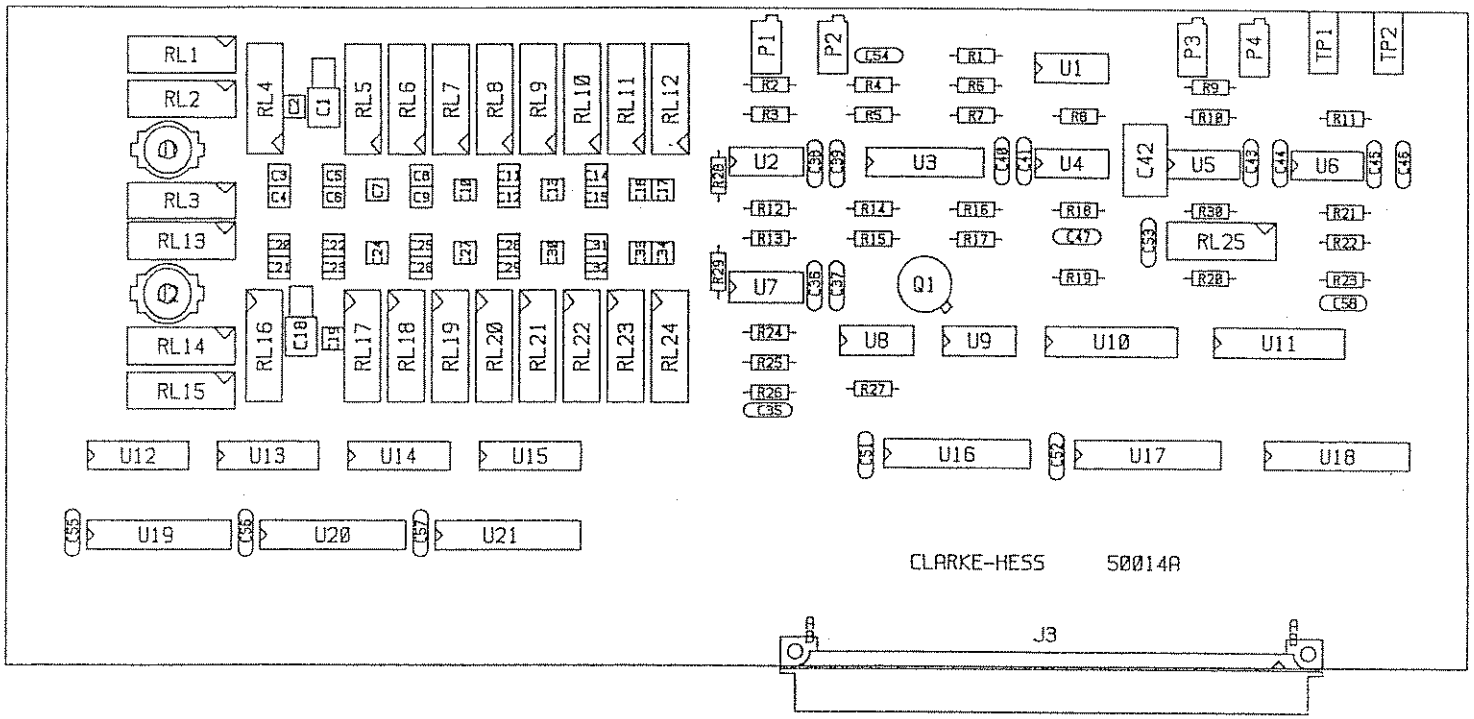
SINE GENERATOR BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50013

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE	SHEET OF

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

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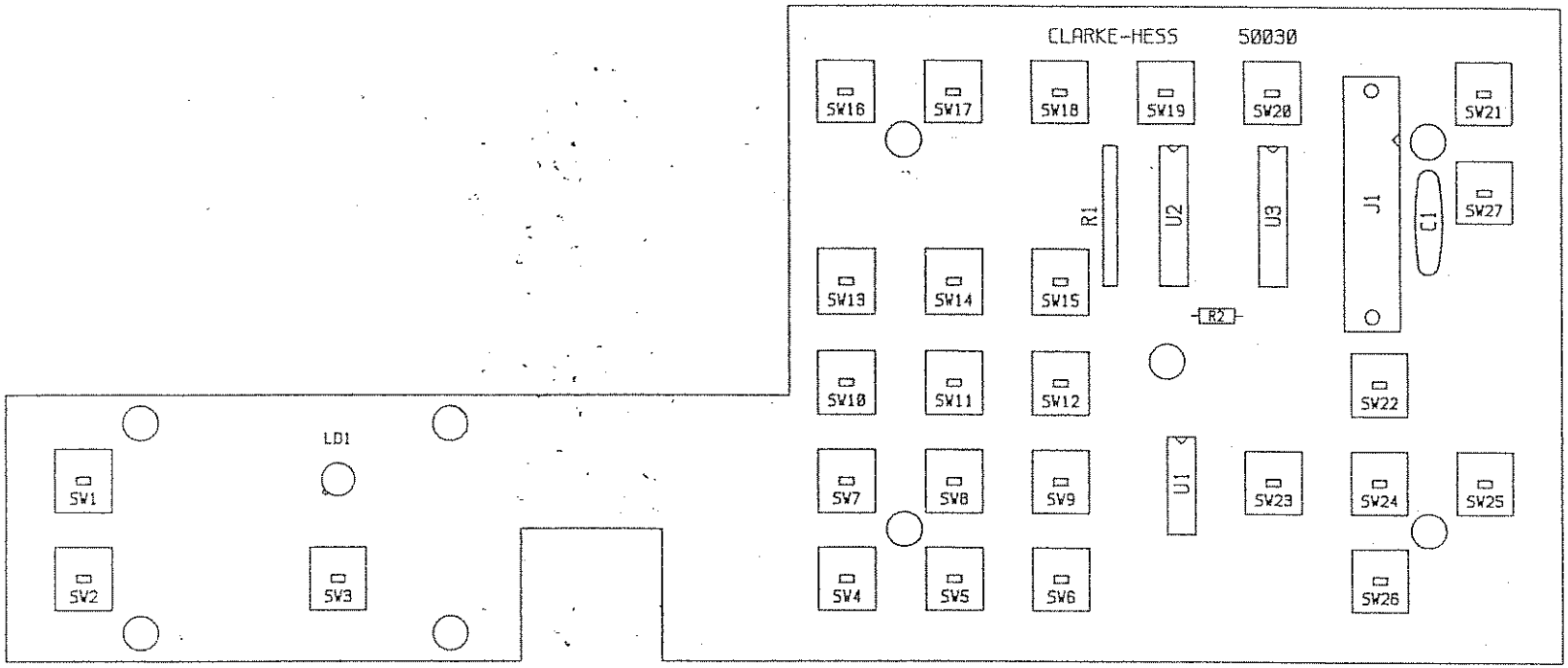
AUTOZERO BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50014

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE | SHEET OF

ZONE | DESCR.



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

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CONTRACT NO.

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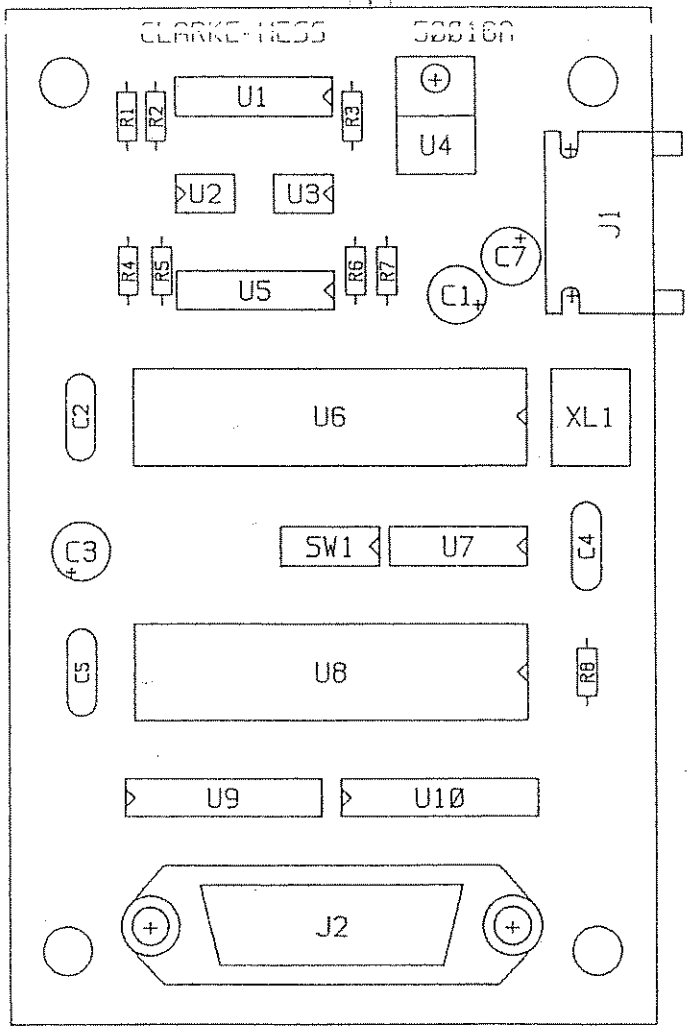
KEYBOARD
BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50015

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET	OF

ZONE	LTR	DESCRIPTION	DATE	APPROVED



	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS = DECIMALS .XX = .XXX = ANGLES =

MATERIAL

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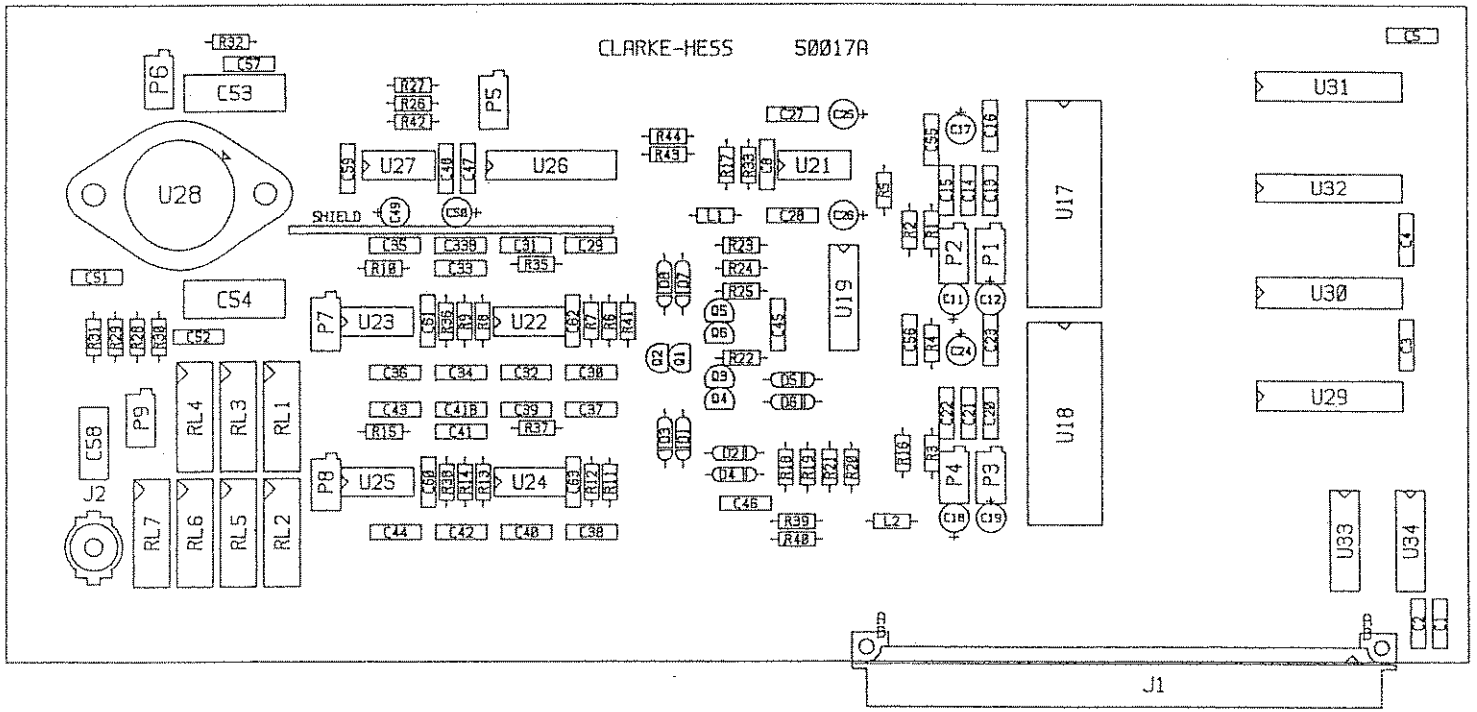
BUSCARD
BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50016

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET OF

ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

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CONTRACT NO.

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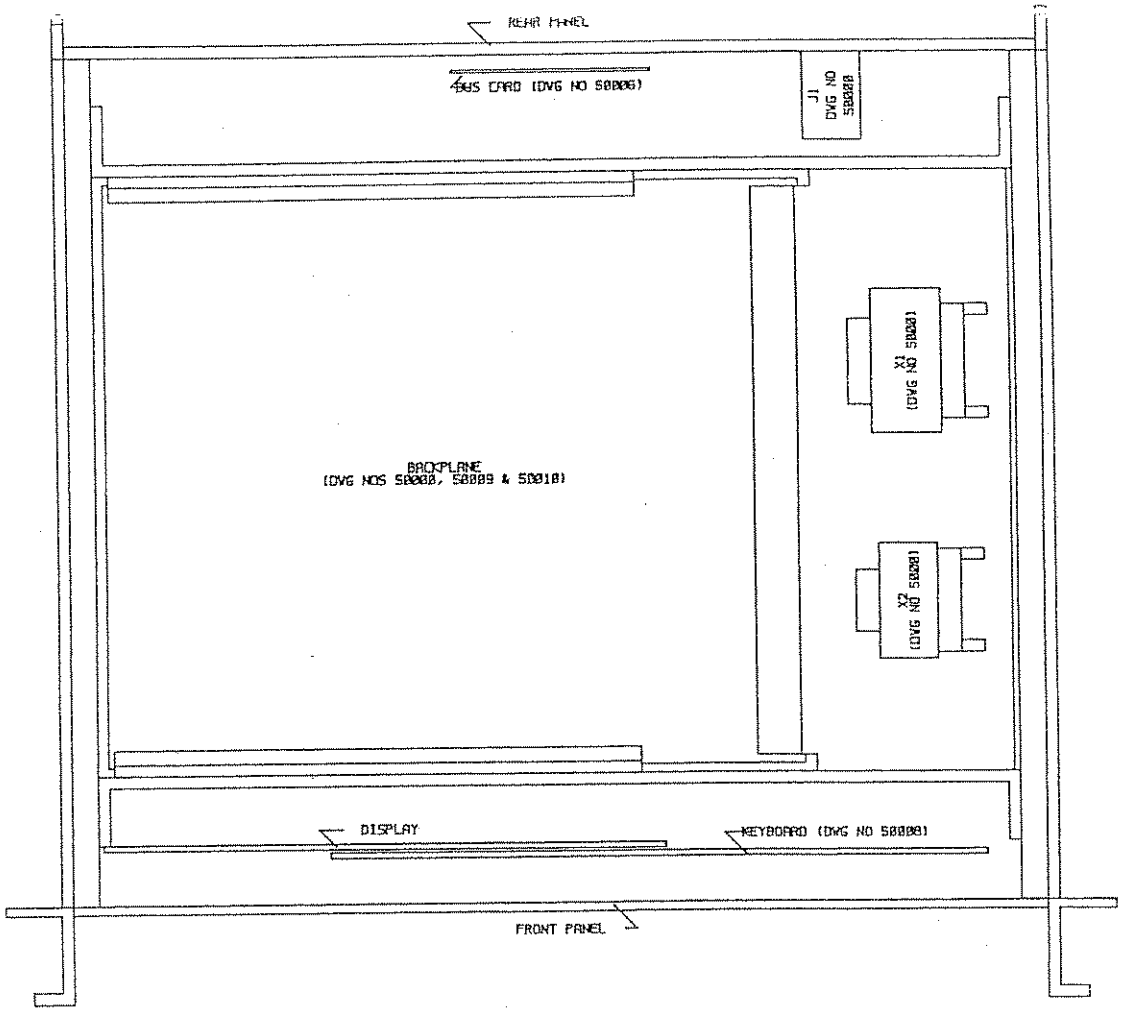
OUTPUT
BOARD LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
C		50017

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SCALE		SHEET OF

ZONE	LTR	DESCRIPTION	DATE	APPD
	A			



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

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CONTRACT NO.

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