tau-tron
A UNIT OF
GENERAL SIGNAL
Digital Instruments Division

MB-302

BERT RECEIVER

OPERATION MANUAL
FORM 0146-1282G

PART NO. 8200-0055

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(617) 692-5100 Telex 750245 1-800-TAU-TRON (Outside MA)

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If any signs of damage are noted on the outside of the carton, request that the carrier's agent be present during unpacking. If external damage is found on the instrument, follow Repair Returns procedure below.

Check the electrical performance of the instrument as soon as possible after receipt. If any malfunctions are observed, follow Repair Returns procedure below.

REPAIR RETURNS

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1. Call the Customer Service Department, (617) 692-5100, for a Repair Authorization Number. This will reduce administrative delays and ensure prompt return of your unit.

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3. Pack the unit in the original shipping carton and packing materials, if available. Otherwise use a double-walled carton (test strength of 350 lb; 159 kg) and shock-absorbing material such as bubblewrap to prevent the unit from moving in the carton during transit. Secure the carton by sealing with heavy paper tape.

4. Send to: Tau-tron Inc.
   10 Lyberty Way
   Westford, MA 01886
   Attn: Customer Service

The MB-302 BERT Receiver Operations Manual is provided in modular form so that it can be tailored to your particular system.

The manual for this module is complete in itself and contains information required to install and operate the module.

CONTENTS PAGE

5. MB-302 BERT RECEIVER

5.1 Description 5-1
5.2 Specifications 5-2
5.3 Installation 5-4
5.4 Front Panel 5-5
5.5 Operation 5-9

5.5.1 System Under Test Connection 5-9
5.5.2 Input Level Select 5-9
5.5.3 Reference Data Synchronization Modes 5-9

5.5.3.1 Auto 5-9
5.5.3.2 Manual Ref Data Select/Manual Sync 5-9
5.5.3.3 Manual Ref Data Select/EXT Command 5-10
5.5.3.4 Manual Ref Data Select/Burst Mode 5-10
5.5.3.5 External Ref Data 5-11

5.5.4 Counter Modes 5-13
5.5.5 Display Time 5-14
5.5.6 Printer Interface 5-15

5.6 Theory of Operation 5-16

5.6.1 Front-Panel Board 5-16

5.6.1.1 Input Clock and Data Amplifiers 5-16
5.6.1.2 6-Digit Display 5-16
5.6.1.3 Status, Ref Data, and other Indicators 5-17

5.6.2 Code ReSync Board 5-17

5.6.2.1 Clock Distribution 5-17
5.6.2.2 Reference Pattern Generator 5-17
5.6.2.3 Input Data Latch and Demultiplexer 5-17
5.6.2.4 Error Detector 5-18
5.6.2.5 Error Sampler 5-18
5.6.2.6 Frame Sync Counter 5-18
5.6.2.7 All Zero Detect 5-18
5.6.2.8 High Speed Error Counter 5-19

5.6.3 Counter Board 5-19

5.6.3.1 Error Threshold 5-19
5.6.3.2 Time Base Control and Counter 5-20
5.6.3.3 Error Counter 5-20
5.6.3.4 Display time 5-20

5.6.4 The Synchronization Process 5-20

5.6.4.1 Auto Sync Mode 5-21
5.6.4.2 Manual Sync Modes 5-21

5.6.5 The Counting Process 5-21

5.6.5.1 Bit Error Rate Auto 5-21
5.6.5.2 Bit Error Rate Manual 5-22
5.6.5.3 Totalize 5-22
5.6.5.4 Frequency 5-22

5.6.6 BCD Interface 5-23
5.6.7 Module Power Supplies 5-23

5.7 GPIB Option 5-24
5.8 Service 5-29

5.8.1 Routine Service 5-29
5.8.2 Repair Returns 5-29
5.8.3 Assistance 5-30
5.8.4 Trouble Analysis 5-30

7. PARTS

7.1 Repaceable Parts 7-1

8. DIAGRAMS

8.1 General 8-1

MB-302 ERROR RATE MODIFICATION S.N. 8111043

The MB-302 which carries the above listed serial number has a modification which allows measurement of error rates in the 10^{-1} through 10^{-8} ranges. This necessitated removal of the 10^{-9} range and modification to unblank 10^{-1} display and blank 10^{-9} display. Synchronization thresholds remain unchanged.

5. MB-302 BERT RECEIVER

5.1 DESCRIPTION

The Tau-Tron MB-302 BERT RECEIVER is a half-size TMI module that provides error-detection and error-measurement capabilities. It not only generates internal pseudorandom and fixed-word references but also allows the application of an externally applied reference for special requirements.

Four modes of operation are provided, including one that automatically selects the type of reference pattern being received and automatically synchronizes on it. Four different measurements are provided, each with switch selectable display times of 1 second, 10 seconds or hold. In one measurement, detected errors are counted and displayed as total errors up to six digits, plus overflow. Two measurements display the error-rate, one with and one without automatic range selection of 10^{-2} through 10^{-9}. The fourth measurement is that of the input clock frequency, in MHz with 1kHz resolution. All measurements are indicated on a large, bright, and easily-read display. The data are also available at a rear-panel connector for automatic logging.

The MB-302 requires the Tau-Tron MF-5 Mainframe for operating voltages and cooling.

5.2 SPECIFICATIONS

CLOCK Input	1kHz to 325MHz range with the following signal type selections: TMI-- 1V amplitude, input impedance is direct coupled 50 ohms to ground. For use with other TMI modules or signal source generating this type of signal. ECL-- 0.8V amplitude, input impedance is direct coupled 50 ohms to -2.0V. AC--- 1V amplitude, AC coupled 50-ohm load, 1MHz low frequency limit. The clock waveshape should be approximately 50% duty cycle.
DATA Input	Choice of TMI, ECL or AC coupling (see CLOCK Input), front-panel controlled, into front-panel BNC connector. Front-panel PHASE control selects additional 3 steps of delay of input data relative to clock for proper clock/data phasing, approximately 3ns max delay.
REFERENCE DATA Input	1kHz to 325MHz, ECL level of 0.8V into 50 ohms to -2V. Must be externally aligned, bit-by-bit, with data input.
COMMAND Input	TTL level of 2V min into 1k ohms to +5V; with burst-mode off, rising edge of this input triggers receiver synchronization. With burst-mode on, low level of this input inhibits error measurement and synchronization checking; and rising edge triggers synchronization (if necessary).
DATA Patterns	Pseudorandom, fixed word or external data. Pseudorandom at 2^7-1 (127), 2^{15}-1 (32,767), 2^{20}-1 (1,098,575), or 2^{23}-1 (8,388,607) bits. Fixed word of any 16-bit repetitive pattern. External data of external synchronized reference pattern.
Synchronization	Four modes are available; automatic, manual, external and external reference data, as selected by front-panel pushbuttons and indicated by front-panel LEDs.
Measurements	Four modes are available, as selected by front-panel pushbuttons and indicated by front-panel LEDs. Display times of 1s, 10s, or hold may be selected. An LED indicates when a measurement is in progress. The RESET pushbutton resets the counter, display and SYNC LOST LED.

Display	6-digit, high-brightness LED display, with 0.430 in. high digits and 0.280 in. high exponent provides measurement data.
Error Output	One pulse per bit error, width follows clock input width, at ECL level of 0.8V into 50 ohms to -2V, available at front-panel BNC connector.
Sync Output	Squarewave occurring once every 4 pseudorandom sequences or every 4 16-bit fixed words, TTL level of 2.4V min into standard TTL load.
Printer Output	TTL compatible I/O lines, positive true outputs and negative true input, available at rear-panel 50-pin D-connector for use with external printer.
Options	OP-02 IEEE-488 Interface (GPIB)
Power	+17V nominal at 0.2A, -17V nominal at 6.0A, unregulated and supplied by mainframe.
Cooling	Forced air, supplied by mainframe.
Mechanical	TMI half-size module. DIMENSIONS: 6.375 in. high x 8 in. wide x 11 in. deep. WEIGHT: 12 lb net, 14 lb shipping.

5.3 INSTALLATION

Module Insertion

1. Pull out the Mainframe Module Lock knob.
2. Insert the module as required.
3. Push in the Mainframe Module Lock knob.

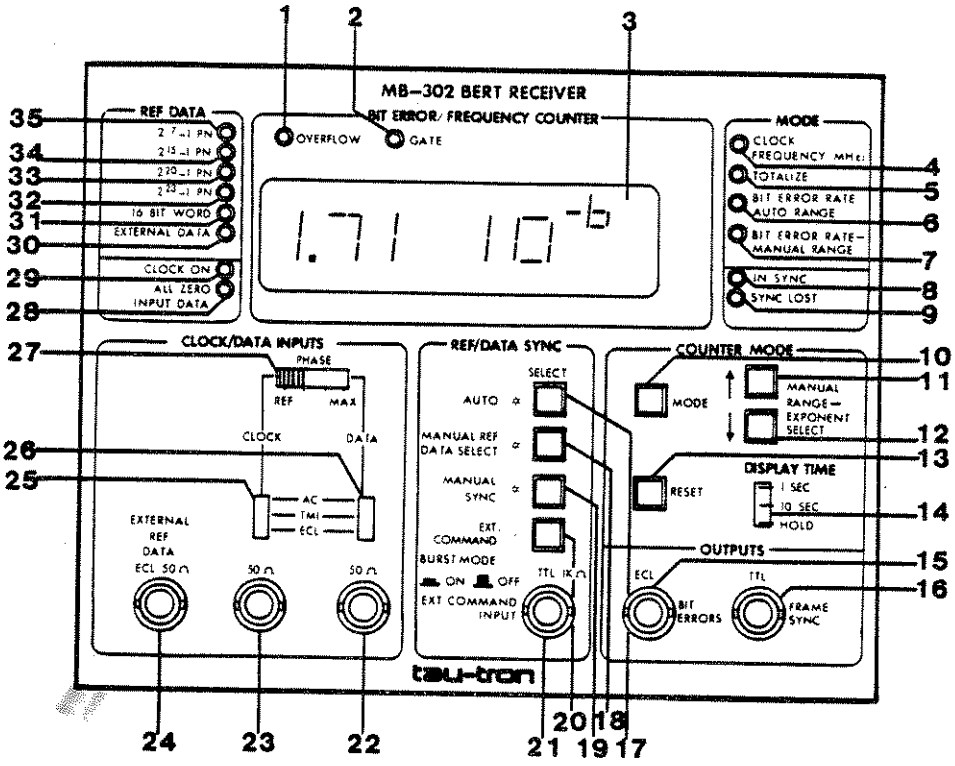
The module(s) can be inserted in any position desired. In general, systems shipped by Tau-Tron have modules inserted in the following order:

Position 1...Clock
Position 2...Transmitter
Position 3...Receiver

Module Removal

1. Pull out the Module Lock knob.
2. Grasp the module to be removed by its front-panel thumbscrews and pull to remove.
3. Push in the Module Lock knob to prevent the remaining modules from accidentally falling out.

5.4 FRONT PANEL



1 OVERFLOW — LED lights when BIT ERROR/FREQUENCY COUNTER overflows.

History vs Current Status — The original design of the MB-302 implemented the overflow indication as a "History Status"; i.e., once the display overflows, it is necessary to push the RESET button on the front panel to extinguish the OVERFLOW LED. The newer MB-302 provides for both History and Current Status OVERFLOW LEDs. In the Current Status overflow indication, the OVERFLOW LED lights if the current displayed measurement had not overflowed.

In the newer MB-302, the Counter PCB includes a shorting connector and programming pins along the edge of the board next to the front panel. As shipped from the factory the shorting connector is installed for a History indication but can be moved in the field for Current indication.

MB-302s shipped prior to October 1981, can be modified for a Current Status overflow indication. Consult factory for further details.

2 GATE — LED lights while the measurement of CLOCK FREQUENCY, TOTAL ERRORS, ERROR RATE AUTO, and ERROR RATE MANUAL are in progress.

3	Display	Indicates the number of total errors accumulated, up to 6 digits plus overflow, and the frequency in MHz, up to 6 digits plus overflow with 1kHz resolution.
4	CLOCK FREQUENCY (MHz)	LED lights when the MODE button is pushed. This button must be continuously pushed until the CLOCK FREQUENCY LED lights. The display indicates the frequency.
5	TOTALIZE	LED lights when the MODE button is pushed. This button must be continuously pushed until the TOTALIZE LED lights. The display indicates the number of total errors accumulated after the RESET button is pushed.
6	BIT ERROR RATE AUTO RANGE	LED lights when the MODE button is pushed. This button must be continuously pushed until the BIT ERROR RATE AUTO RANGE LED lights. In this mode, the display indicates the error-rate up to 3 digits plus overflow with a 2-digit exponent.
7	BIT ERROR RATE MANUAL RANGE	LED lights when the MODE button is pushed. This button must be continuously pushed until the BIT ERROR RATE MANUAL RANGE LED lights and the two MANUAL RANGE EXPONENT SELECT buttons light. The display indicates the error-rate up to 3 digits plus overflow with a 2-digit exponent.
8	IN SYNC	LED lights when sync is acquired automatically and then synchronized.
9	SYNC LOST	LED lights when, at any time during a measurement, sync is lost.
10	MODE	Illuminated button is used to select CLOCK FREQUENCY, TOTAL ERRORS, ERROR RATE AUTO, and ERROR RATE MANUAL postions as required.
11 12	MANUAL RANGE EXPONENT SELECT	Two illuminated buttons light when the MODE button is pushed continuously until the BIT ERROR RATE MANUAL RANGE indicator lights. Push the upper MANUAL RANGE EXPONENT SELECT button to increase the exponent indicated on the display, or push the lower button to decrease it, until the desired range of from 10^{-2} to 10^{-9} is selected.
13	RESET	Illuminated button is used to help display TOTAL ERRORS, to stop error measurement, and to reset the display to zero while in HOLD time so that a new measurement can be initiated.

14	DISPLAY TIME	Vertical three-position slide switch selects three different display times: 1 SEC, 10 SEC or HOLD.
15	BIT ERRORS/ ECL	BNC output connector indicates a one pulse per bit error, width follows clock input width, at ECL level of 0.8V into 50 ohms to -2V.
16	FRAME SYNC/ TTL	BNC output connector indicates a squarewave occurring once every 4 pseudorandom sequences or every four 16-bit fixed words.
17	AUTO/SELECT	Illuminated button automatically selects reference data and displays by means of REF DATA LEDs. Sync is also acquired automatically and a synchronized condition illuminates the IN SYNC LED.
18	MANUAL REF DATA/SELECT	Illuminated button lights when the AUTO button is pushed. This button must be continuously pushed until the MANUAL REF DATA SELECT button lights. Push the MANUAL REF DATA SELECT button for the desired range (2^7-1 PN thru 2^{23}-1 PN, or 16-BIT word).
19	MANUAL SYNC/ SELECT	Illuminated button lights when AUTO button is pushed. This button must be continuously pushed until the MANUAL SYNC button lights. Push the MANUAL SYNC button to synchronize; a synchronized condition illuminates the IN SYNC LED.
20	EXT COMMAND/ SELECT	Illuminated button lights when the AUTO button is pushed. This button must be continuously pushed until the EXT COMMAND button lights. Same as MANUAL SYNC operation except sync attempt is initiated by a signal applied to the EXTERNAL COMMAND INPUT BNC connector.
21	EXT COMMAND INPUT/BURST MODE	BNC connector to connect to an external sync signal. The BURST MODE is used in conjunction with the AUTO button being pushed until the MANUAL REF DATA SELECT and EXT COMMAND buttons light. The EXT COMMAND button must be pushed in for the BURST MODE operation to function.
22	Data	BNC connector indicates a choice of coupling (TMI, ECL or AC).
23	Clock	BNC connector indicates a choice of coupling (TMI, ECL or AC).
24	EXTERNAL REF DATA	BNC connector input for a 1kHz to 325MHz, ECL level of 0.8V into 50 ohms to -2V signal. This input must be externally aligned bit-by-bit, with the data input.

25	CLOCK Input Level	Vertical three-position slide switch indicates a sinewave or square-wave in a choice of coupling (TMI, ECL or AC). The AC, TMI inputs range from 1kHz to 325MHz with 1V into 50 ohms to ground; AC and DC coupled respectively. The ECL input ranges from 1kHz to 325MHz with 0.8V into 50 ohms to -2V, DC coupled. An LED indicates when clock input is detected.
26	DATA Input Level	Vertical three-position slide switch indicates a choice of coupling (TMI, ECL or AC). The AC, TMI inputs range from 1kHz to 325MHz with 1V into 50 ohms to ground; AC and DC coupled respectively. The ECL input ranges from 1kHz to 325MHz with 0.8V into 50 ohms to -2V, DC coupled. An LED indicates when the data are all zeros (not present).
27	PHASE	Horizontal three-position slide switch selects additional three steps of delay input data relative to clock for proper clock/data phasing, approximately 3ns maximum delay.
28	ALL ZERO INPUT DATA	LED lights when data are all zeros (not present).
29	CLOCK ON	LED lights when clock signal is present.
30	EXTERNAL DATA	LED lights when the AUTO button is pushed. This button must be continuously pushed until the EXTERNAL DATA LED lights.
31	16-BIT WORD	LED lights when the MANUAL REF DATA SELECT button is pushed for 16-BIT WORD.
32	Pseudorandom Sequence	LED Lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{23}-1.
33	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{20}-1.
34	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{15}-1.
35	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{7}-1.

5.5 OPERATION

5.5.1 SYSTEM UNDER TEST CONNECTION

The MB-302 requires a clock and data signal, both at the same rate, in order to synchronize and perform error measurements. These connections must be made with a 50-ohm coaxial cable using BNC connectors.

5.5.2 INPUT LEVEL SELECT

The front-panel CLOCK and DATA input levels must be selected prior to starting the test. The TMI and ECL signals are DC coupled 50-ohm inputs with the reference termination voltage at ground and -2V, respectively. The AC input is a capacitively coupled 50-ohm input impedance.

5.5.3 REFERENCE DATA SYNCHRONIZATION MODES

There are five modes of synchronization possible with the MB-302, the modes are chosen by the SELECT pushbutton, which is also the AUTO mode LED, in the REF DATA/ SYNC section of the front panel. Each time this SELECT button is pushed, the appropriate LED should light which shows the selected mode.

5.5.3.1 AUTO

In this mode, the MB-302 Reference Data is automatically selected to match the incoming data at the front panel. In addition, synchronization is acquired automatically once the receiver has determined the correct pattern. If, at any time during the measurement, synchronization is lost, the SYNC LOST LED will light; the receiver will automatically initiate a resynchronization sequence and, if synchronization is reacquired, both the IN SYNC and SYNC LOST LEDs will be on. The RESET pushbutton will extinguish the SYNC LOST LED.

5.5.3.2 MANUAL REF DATA SELECT/MANUAL SYNC

When this mode is chosen, via the SELECT pushbutton, both of these LEDs will light. Push the MANUAL REF DATA SELECT button and watch the REF DATA LEDs, in the upper left-hand corner, sequence through the patterns until the REF DATA pattern agrees with the MN-302 pattern.

Once the patterns are matched, push the MANUAL SYNC, if the input data error-rate is within the acquisition threshold, the IN SYNC LED should light, observe the error display in either of the bit error-rate modes or totalize, adjust the PHASE switch to minimize the error count.

If the receiver loses synchronization due to high error-rate at the data input, the SYNC LOST LED will be ON and the IN SYNC LED will be OFF, the only way to re-establish sync acquisition is to push the MANUAL SYNC button.

NOTE: This may happen when adjusting the PHASE switch during initial set-up of the system.

5.5.3.3 MANUAL REF DATA SELECT/EXT COMMAND

This mode functions similar to the MANUAL REF DATA SELECT/MANUAL SYNC mode except that the initiation of the sync acquisition function is done with an externally applied TTL pulse. Push the SELECT button until the MANUAL REF DATA SELECT and EXT COMMAND LEDs are lit. Check that the EXT COMMAND button is in the OUT (unlatched) position. Connect the external command signal source to the EXTERNAL COMMAND input, the signal is active LOW and synchronization is initiated on the LOW to HIGH transition (trailing edge) of this signal. This signal is TTL into the 1k-ohm input level, the minimum width is 50ns.

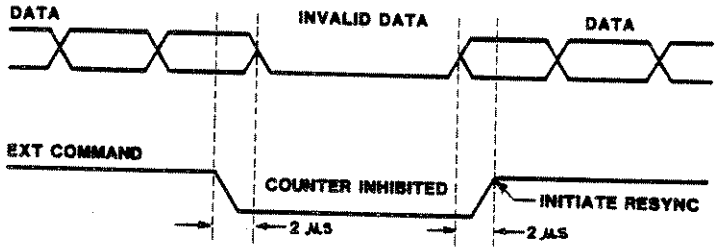
If receiver synchronization is lost then the EXT COMMAND pulse must be applied in order to re-establish the IN SYNC condition.

5.5.3.4 MANUAL REF DATA SELECT/BURST MODE

Push the select pushbutton until the MANUAL REF DATA SELECT/ EXT COMMAND LEDs light, then push the EXT COMMAND button so that it latches. Select the REF DATA PATTERN by pushing the MANUAL REF DATA SELECT pushbutton and observing the REF DATA LEDs in the upper left-hand corner of the front panel. In this mode, two operations take place, when the EXT COMMAND goes from its normal logic-1 value to logic-0, the MB-302 Error Counter is inhibited for the duration of the logic-0 level; when the EXT COMMAND makes a logic-0 to logic-1 transition, the synchronization process is initiated and resynchronization acquisition will occur.

This mode is used when the data are present in bursts or when continuous data have bursts of nonvalid data; in either case, error counting can be enabled only when the data are ready for measurement.

NOTE: The IN SYNC and SYNC LOST LEDs may be on simultaneously during a test in the BURST MODE because, even though the error counters are inhibited, the error threshold circuits are still active. The actual EXT COMMAND signal should have some guard band of approximately 2 micro-seconds on either side of the burst pulse to allow for loss of sync and reacquisition of sync before the counters are enabled.

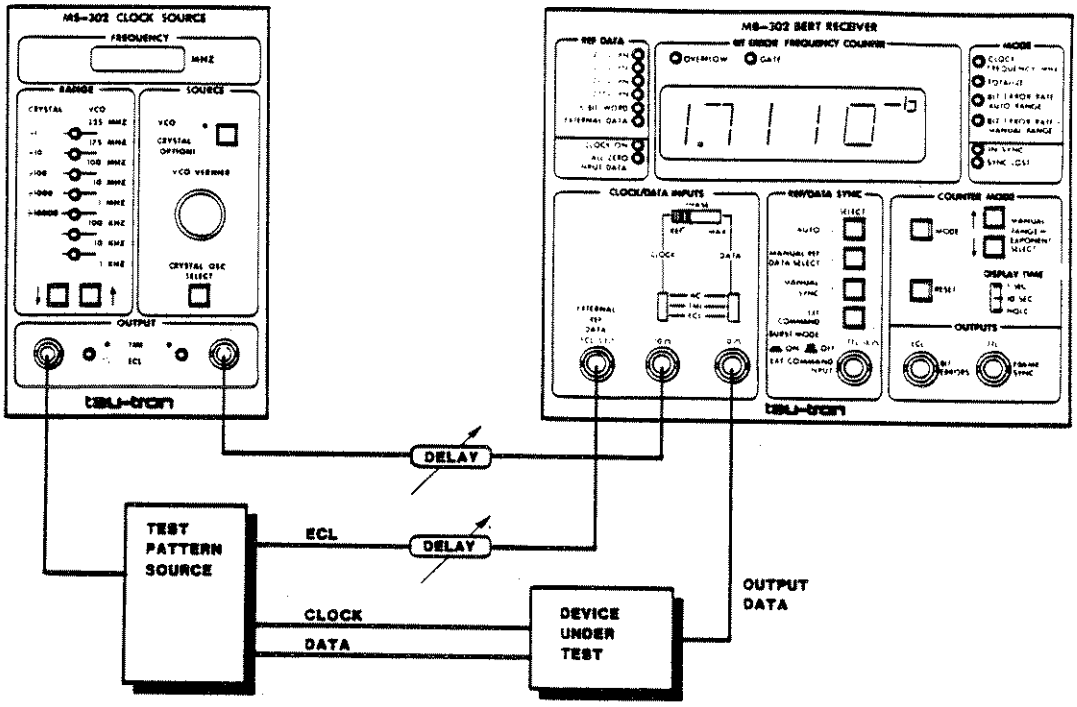


BURST MODE TIMING DIAGRAM

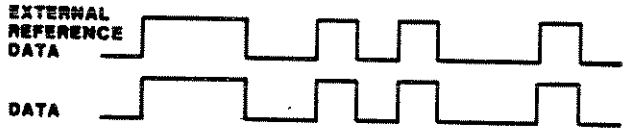
5.5.3.5 EXTERNAL REF DATA

In this mode, the MB-302 functions as a 2-channel comparator and any two identical data streams can be used as the input. Push the SELECT button until the MANUAL REF DATA SELECT LED is lit, then push the button again until EXTERNAL DATA is selected on the REF DATA indicators. Refer to page 5-12 for Test and Timing Diagrams.

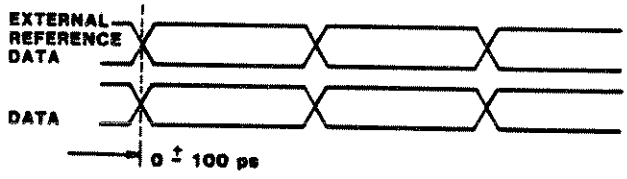
Connect the MB-302 EXTERNAL REF DATA input to an output of the test pattern source via a 50-ohm coaxial cable and a variable delay control. (Note that the MB-302 EXTERNAL REF DATA input must be ECL, the input termination is 50 ohms to -2 volts.)



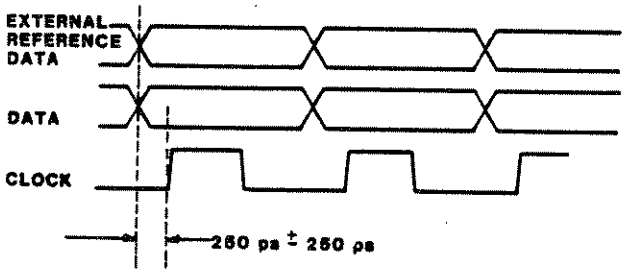
EXTERNAL REFERENCE DATA TEST DIAGRAM



BIT-BY-BIT ALIGNMENT



FINE TUNED DATA ALIGNMENT



DATA/CLOCK TIMING

EXTERNAL REFERENCE DATA TIMING DIAGRAMS

Connect the Device Under Test (DUT) output to the MB-302 DATA input. Make the appropriate input level selection. Set the MB-302 CLOCK/DATA PHASE control to the REF position.

Connect the MN-302 CLOCK input to the system clock output via a 50-ohm cable and a variable delay control.

Observe the EXTERNAL REF DATA input and the DATA input on a dual channel oscilloscope with matched delay inputs. Adjust the REF DATA variable delay control until it agrees with the DATA input bit-for-bit, then fine tune the delay control until the edges of the two data inputs are aligned to within ±100 pico-seconds.

Observe one of the DATA inputs and the CLOCK inputs, adjust the clock delay for the timing as shown in the diagram. Connect all inputs to the MB-302, fine tune the clock phase to minimize the error display. (ZERO errors if the set-up is using error-free data.)

Push the RESET pushbutton to initialize the counter and begin the test. The following characteristics of this mode should be noted:

1. There is no "synchronization/acquisition" function in the mode; hence, the IN SYNC/SYNC LOST LEDs have no meaning when determining the sync status.
2. The error counters function in all modes as before, the SYNC LOST LED may serve as a coarse indicator of burst error conditions, but as just mentioned, there is no "sync acquisition" function.
3. If large changes are made to the clock frequency, then all input timing must be rechecked.
4. The CLOCK/DATA PHASE control must NOT be moved from the REF postion.

5.5.4 COUNTER MODES

Four measurement modes are possible; all are selected by the MODE pushbutton in the COUNTER MODE section of the front panel.

CLOCK FREQUENCY — Push the MODE button until the CLOCK FREQUENCY LED lights. The display indicates the frequency in MHz, up to 6 digits plus overflow, with a 1kHz resolution. The GATE LED lights while the measurement is in progress.

TOTAL ERRORS — Push the MODE button until the TOTALIZE LED lights. The display indicates the number of total errors accumulated after the RESET button is pushed, up to 6 digits plus overflow. The GATE LED lights while the measurement is in progress. The measurement is stopped by pushing the RESET button.

ERROR RATE AUTO — Push the MODE button until the BIT ERROR RATE AUTO RANGE LED lights. In this mode, the range is selected automatically for 10^{-2} to 10^{-9}. The display indicates the error-rate, up to 3 digits plus overflow, with a 2-digit exponent. The GATE LED lights while the measurement is in progress.

ERROR RATE MANUAL — Push the MODE button until the BIT ERROR RATE MANUAL RANGE LED lights and the two MANUAL RANGE EXPONENT SELECT buttons light. Push the upper MANUAL RANGE EXPONENT SELECT button to increase the exponent as indicated on the display, or push the lower button to decrease it, until the desired range of from 10^{-2} to 10^{-9} is selected. The display indicates the error-rate, up to 3 digits plus overflow, with a 2-digit exponent. The GATE LED lights while the measurement is in progress.

NOTE: In the ERROR RATE modes (AUTO or MANUAL) the error-rate measurement is not valid until the END of the gate period, at this point the GATE LED goes out and the display is updated with the final count value.

5.5.5 DISPLAY TIME

Three different times are possible, all are selected by the DISPLAY TIME switch: 1 sec, 10 SEC or HOLD. With the 1 SEC or 10 SEC times, the display is held for the indicated time, then both the measurement and display are automatically reset to zero and a new measurement is initiated. With the HOLD time, the display is held until the RESET button is pushed at which time the display resets to zero and a new measurement is initiated.

NOTE: The BIT ERRORS output produces a pulse at an ECL level each time an error is detected during measurement, independent of the measurement mode selected. This output would be connected to an external counter so as to count total errors while the MB-302 is measuring the error-rate. As a result of this, a simultaneous indication of total errors and error-rate would be produced.

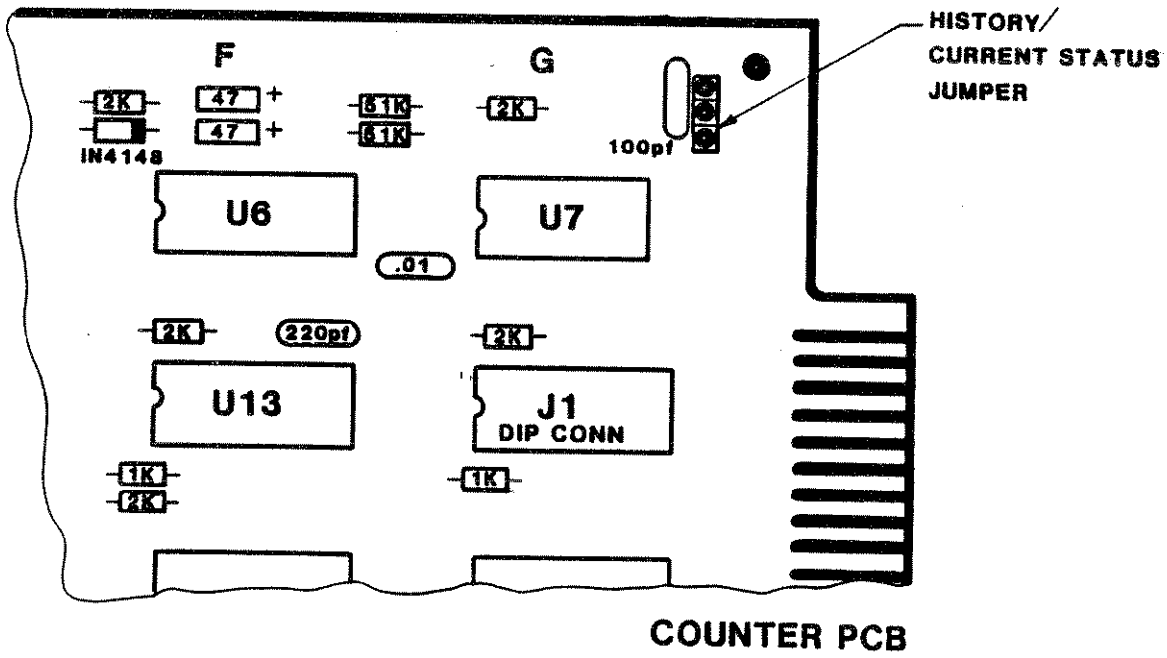
5.5.6. PRINTER INTERFACE

The MB-302 Printer Interface connector on the MF-5 Mainframe rear panel has all the available handshaking necessary to interface to any standard parallel BCD printer. Lines include 6 BCD digits plus decimal point, printer strobe, printer busy input, and status lines for time rate auto, time rate manual, frequency, totalize, in sync and lost sync.

NOTE: Ensure that the internal cable in the MF-5 Mainframe lines up correctly with the MB-302 Printer Interface connector.

5.5.6.1 CURRENT STATUS VS HISTORY STATUS

When in the current status mode and a BCD printer interface is installed in the system, the system will print twice for every over-threshold measurement or for every measurement the system takes. If this is undersirable, switch over from the current to the history mode by changing the jumper on the Counter PCB. This, as a result, lets the system update and print only once for every measurement.



5.6 THEORY OF OPERATION

The MB-302 receiver (refer to the system Block Diagram) performs bit-by-bit measurements between incoming data and its own locally generated reference generator. Bit errors exist when the incoming data and the reference generator do not agree on a bit-by-bit basis. The bit errors are then displayed in a variety of ways to the user; one is totalize where all errors from the start to the end of a test are accumulated, another is automatic time rate where the errors are displayed as a function of the total number of bits in the measurement internal. In this mode, the exponent is automatically selected as a function of the number of errors. The third way is manual bit error-rate where the gate time interval can be set manually with a front-panel pushbutton. An overflow LED signals when the measured errors exceed the range of the selected time interval or the six-digit totalize range.

The MB-302 contains a front-panel board which holds the high-speed input amplifiers, a Code Resync board where the reference pattern generator, frame sync circuits, and error detectors are located and a Counter board which contains all of the error counting logic and sync acquisition control functions. Standard units contain a BCD Interface board for the Printer Output. If GPIB option is installed, the BCD Interface is replaced by the GPIB Interface board.

5.6.1 FRONT-PANEL BOARD

The front-panel pc board contains the high-speed clock and data input amplifiers as well as the display and display control logic.

5.6.1.1 INPUT CLOCK AND DATA AMPLIFIERS

Identical wide-band, pulse amplifiers convert the three selectable input signals to ECL for use within the module. An internal threshold adjustment is factory-set for maximum sensitivity and frequency response. These amplifiers, designed by Tau-Tron, are plug-in hybrid micro-circuits and operate as extremely fast current-mode switches. Output rise and fall times are typically much less than one nano-second when driving 50-ohm terminated lines.

5.6.1.2 6-DIGIT DISPLAY

The 6-digit LED display is driven from a display controller/driver mounted on the front panel. The display controller multiplexes data from the counter board and, under control from an oscillator on the counter board, presents the information to the display in the form of a scan across the six LED digits. The scan rate is such

that the indicators appear to be on continuously, but are actually on only when selected by the controller.

5.6.1.3 STATUS, REF DATA, AND OTHER INDICATORS

These single LEDs are driven from logic circuits or discrete component drivers and are essentially DC levels which reflect the status of the indicated signal as opposed to the digit LEDs which are dynamically driven.

5.6.2 CODE RESYNC BOARD

This board contains all of the reference pattern generator circuits and high-speed comparators which determine the bit errors. The circuit elements are ECL devices either in dual inline or flat-pack packages.

5.6.2.1 CLOCK DISTRIBUTION

The full-rate clock, from the input amplifier, drives a divide-by-2 circuit and this half-rate clock becomes the primary clock signal for the Code ReSync Board. The only places where the full-rate clock is used are at the input data latch and the error sampler. All other code generator processing is done at half rate.

5.6.2.2 REFERENCE PATTERN GENERATOR

The pattern generator itself is a variable length linear feedback shift register with feedback taps chosen such that the output is a maximal-length pseudorandom sequence. The pattern generator runs at half the input clock rate, but two phases are developed as input to the error detector so as to match the two phases of input data from the input data demultiplexer. The length of the shift register can be either 7, 15, 20 or 23 stages.

5.6.2.3 INPUT DATA LATCH AND DEMULTIPLEXER

A high-speed data latch, clocked at the input clock rate, transfers the input data to the data demultiplexer. The variable delay, under control of the front-panel CLOCK/DATA PHASE switch, insures that the transitions of the data with respect to the rising edge of the clock do not violate the setup time of the data latch. The demultiplexer translates the input data from a single data stream at the input clock rate to a pair of identical data streams at half the clock rate. These data streams are displaced by a 1/2 frame ±1 bit with respect to each other. In addition, these data streams along with the reference generator signals with identical frame phase relationships become the inputs to the Error Detector.

5.6.2.4 ERROR DETECTOR

The error detector is a network consisting of a pair of Exclusive-OR gates; each gate has a reference data bit stream and a demultiplexed input data bit stream as an input. Hence, although the processing is done at one half of the input clock rate, the use of two comparators insures that every input data bit, on a bit-by-bit basis, is checked against the reference code. The error detector output is an NRZ pulse for each data bit in error.

5.6.2.5 ERROR SAMPLER

The error sampler combines the two half-rate NRZ error channels from the error detector into a single high-speed error signal. To do this, the full-rate system clock strobes the two error channels such that every error bit is present as a pulse at the output. This error signal drives a buffer gate to the front-panel ECL BIT ERROR output jack. It also is the input to the Error Threshold counter section.

5.6.2.6 FRAME SYNC COUNTER

In order to generate a sync pulse on a per frame basis, the Frame Sync Counter detects a unique bit pattern within the frame period of the selected code. This unique pattern is the maximum number of consecutive zeros which, in this type of pattern generator, is always one less than the number of stages in the shift registor. For instance, in the 2^7-1 code length, there are seven stages in the shift register; therefore, six consecutive zeros occur, but occur only once in the 127-bit frame length. The same analysis holds true for the remaining code lengths except that the number of bits per frame and; hence, the time between frames, is considerably longer.

5.6.2.7 ALL ZERO DETECT

The absence of data of the MB-302 DATA INPUT will cause the ALL ZERO INPUT DATA LED to light. This signal is derived by sampling both phases of the demultiplexed input data and the most significant bit of the Frame Sync Counter. Under normal conditions, there will always be activity on the input data line and; hence, the zero indicators will not light. If the data are removed, then no activity is present on the input line, the receiver loses synchronization and the zero indicator will be set by the first transition out of the Frame Sync Counter most significant bit.

NOTE: It must be remembered, when in the AUTO SYNC MODE, that the absence of data (logic-0 at the input) or a continuous logic-1 at the input can cause a

condition where the system appears to be in sync even though there are no data present. This is because, in the AUTO SYNC mode, the static levels of logic-1 or 0 are interpreted as a 16-bit fixed word and; hence, represent a valid data pattern even though the original pattern may have been one of the pseudorandom codes.

5.6.2.8 HIGH-SPEED ERROR COUNTER

The first stage of error counting, which corresponds to the least significant digit on the error display, is done on the code ReSync Board. The input to this first counting stage can be as high as 325Mb/s; hence, in order to localize the high-speed signals, a bi-quinary divider is used to count the first digit in both the bit error-rate and totalize count modes. The first stage of error counting for the threshold circuits is also done on this board, sharing logic circuits with the totalize counting circuits. Two error count signals are sent to the Counter Board from the Code Resync Board, one is the E/4 signal to the threshold logic and the other is the least significant digit (BCD) for the display. In addition, a CLOCK/20 is also generated on the ReSync Board for use on the Counter Board.

5.6.3 COUNTER BOARD

The Counter Board accepts the error signals and prescaled clock signals from the ReSync Board and generates all of the error display information for the front panel. In addition, the digital error threshold circuits are located on this board; these circuits determine whether the amount of bit measured errors with respect to the number of bits sampled exceeds a pre-defined ratio.

5.6.3.1 ERROR THRESHOLD

The error threshold logic has two thresholds for operation, a low threshold which is active when the receiver is trying to establish code synchronization (search) and a high threshold which allows the receiver to maintain code synchronization in high error-rate situations (hold). The thresholds are as follows:

MODE	SEARCH (LOW) THRESHOLD	HOLD-IN (HIGH) THRESHOLD
P/N SEQUENCE	64 errors/800 bits	3200 errors/10,000 bits
FIXED WORD	32 errors/1600 bits	1600 errors/10,000 bits

The thresholds are determined by fixed dividers on the system clock which provide the block of bits over which the error measurement must be made, the high-speed

dividers on the ReSync board provide the error information to the low-speed counters on the Counter Board. The block of bits determines an error threshold frame which resets the error accumulators at the end of the block time. If the accumulator is filled before the end of the frame, then an over-threshold condition exists and other circuit and system functions are initiated.

5.6.3.2 TIME BASE CONTROL AND COUNTER

The Time Base Counter is an 8-decade counter driven by a pre-scaled clock pulse from the Code ReSync board. The counting window or time base is selected by the Time Base Control which enables the proper decade. This decade is represented by the exponent on the front-panel display and may be selected manually or automatically. The range of the exponent is from 10^{-2} to 10^{-9} which selects decade divider ranges from 10^{-4} to 10^{-11}.

5.6.3.3 ERROR COUNTER

The actual error counter is a six-decade BCD counter; the least significant digit is located on the ReSync board and is a high-speed bi-quinary circuit, this output drives the remaining 5 decades on the counter board which are low-speed (TTL) BCD dividers. The counter outputs drive data selectors which control the multiplexing of the counter onto the scanned front-panel display.

5.6.3.4 DISPLAY TIME

The front-panel DISPLAY TIME switch controls the time constant of a TTL one-shot multivibrator. This circuit controls the rate at which the display holds its information for observation by the user. The display time generator also provides reset and preset signals to the error counters, time base counters and error latch circuits; these signals occur at the end of the display time.

5.6.4 THE SYNCHRONIZATION PROCESS

The synchronization of incoming data with the internal reference data is accomplished using a "feed-forward" technique. Assuming that the receiver is not synchronized with the incoming data, an output from the error threshold detector will cause the incoming data stream to be loaded into the internal reference code generator shift register. At the end of 800 bits, the feed-forward signal is removed and the reference generator begins to shift on its own, advancing to the next state of the code. The input data should also be advancing to the same state and; hence, the errors should be zero. The error detector compares the two data streams, one from the reference

generator and one from the device under test. If the errors are less than 64 over the next 800 bits, then the input data are assumed to be correct and the error threshold converts to the high threshold value where errors less than 3200 in 10,000 bits are required to maintain synchronization. This basic procedure is used in all sync modes and pattern selections.

5.6.4.1 AUTO SYNC MODE

In this mode, the search for the proper internal reference code is done automatically. Assuming initially that the receiver is not synchronized, the basic feed-forward procedure is initiated. If, at the end of an 800-bit sample, the error threshold is exceeded, then the procedure is re-initiated. If, after the second attempt, the error threshold is still too high, the reference code selector is automatically advanced to the next pattern and the synchronization procedure starts again. This will continue until all of the pattern lengths have been examined at least twice. This can be observed on the front panel, the REF DATA indicators will be flashing as they are selected.

5.6.4.2 MANUAL SYNC MODES

All of these modes require that the internal reference code be selected manually with the front-panel controls. The other common feature of the manual modes is that some external signal must generate the feed-forward or re-synchronization signal. In the MANUAL mode, it is the front-panel pushbutton and, in the EXTERNAL modes, it is from some other electrical signal. If synchronization is acquired and then lost, the external re-sync signal must be applied in order to start the synchronization process again.

5.6.5 THE COUNTING PROCESS

The counter section provides three methods of counting bit errors, two of them are bit error-rate modes and the third is a totalize mode. In addition to counting errors, the counter functions as a frequency meter and displays the input clock frequency on the front-panel display.

5.6.5.1 BIT ERROR RATE AUTO

In this mode, the exponent of the bit error-rate is automatically set as a function of the measured errors. The exponent always starts at 10^{-2} and increments to the next

lowest error-rate -- 10^{-3}, 10^{-4} etc. Each selection of an exponent enables an increased counting window in the error counter because the exponent is a direct function of the number of bits or clock periods over which the measurement is being taken. The exponent will continue to increment until a minimum of 200 errors are counted in a particular range. Once at least 200 errors are counted, the measurement will continue until the end of the counting window; at that time the exponent will be incremented to the next value and the display will be updated with the present value held in the error-counter buffer. The counters get reset and the count cycle re-starts at 10^{-2}, incrementing at the end of each exponent time-out until at least 200 errors are detected. If no errors are detected, the counter will reach 10^{-9} and remain there.

5.6.5.2 BIT ERROR RATE MANUAL

In this mode, the counting window is set via the front-panel EXPONENT SELECT push-buttons. The count window is fixed and errors are constantly measured over the same time base. If the errors exceed the time base, then an overflow condition exists, and the OVERFLOW LED will be lit. The overflow condition can be avoided by setting the exponent to some higher error-rate value.

NOTE: The GATE LED is illuminated during the time that the counter gate is open. The displayed value is valid only at the END of the count cycle when the GATE LED goes out and the counter is updated with the final value.

5.6.5.3 TOTALIZE

The totalize mode functions by opening the count gate at the start of a measurement (such as after a reset) and will not close the gate until the RESET button is pushed or the mode is switched. In this mode, errors accumulate indefinitely or until the measurement is deemed to be complete. If the six-digit counter overflows, the OVER-FLOW LED remains on while the overflow condition exists.

5.6.5.4 FREQUENCY

In the Frequency mode, the input clock frequency will be displayed on the front panel. The units displayed are Megahertz but the six-digit display has resolution down to 1 kilohertz. A 1MHz crystal time base divided down to 10^{-5} provides the basic count-ing window for this measurement. The 10 millisecond squarewave enables the input clock to be divided and entered into the display buffer. At the end of this time, the value is latched and presented to the display.

5.6.6 BCD INTERFACE

The BCD Interface is a synchronous demultiplexer with six output latch sets, one for each of the five data digits and one for the exponent digit. When the MB-302 gate signal goes low, indicating end of measurement, the BCD Interface starts looking for the first data byte address, 0. The interface then latches the data byte into the corresponding output data latch. When address 6 is detected, all data have been loaded and are ready for the printer where a print strobe is generated. When the printer responds with a $\overline{\text{BUSY}}$ signal, the BCD Interface holds the output data stable and does not accept any more data from the MB-302 until the printer $\overline{\text{BUSY}}$ line goes high, initializing the interface for the next block of data.

5.6.7 MODULE POWER SUPPLIES

The unregulated mainframe voltages of ±34 and ±17 are the inputs to voltage regulators located on the rear and side of the module. The +34V and -34V drive the +15V and -15V regulators with loads of much less than 1A. The +17V is regulated to +8V which provides power to the micro-circuit amplifiers and is also the input to a +5V regulator located on the clock source board. This voltage is used for TTL logic circuit power. The -17V is regulated to -5.2V high current supply using a combination of a three-terminal regulator and boost transistor. This voltage is also used to drive a pc board mounted -2V regulator which supplies the termination voltage for the high-speed ECL circuits.

5.7 GPIB OPTION

GENERAL

All front-panel controls, except CLOCK/DATA INPUTS PHASE and MANUAL SYNC switches, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An associated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired. This option replaces the standard printer output.

MESSAGE Format

The message consists of five digits (in ASCII code) followed by a terminator.

Ident	CNTR Mode	SYNC Mode	REF DATA	BER EXP	Termi-nator

Ident

Digit	Meaning
3	MB-302

CNTR Mode

Digit	Meaning
0	Bit error rate-Manual range
1	Bit error rate-Auto range
2	TOTALIZE
3	Clock frequency

SYNC Mode

Digit	Meaning	
0	Auto synchronization	
1	Manual synchronization	Burst
2	EXT COMMAND sync	mode
3	EXT REF DATA	enabled
4	Auto synchronization	
5	Manual synchronization	Burst
6	EXT COMMAND sync	mode
7	EXT REF DATA	disabled

Internal REF DATA

Digit	Meaning
0	2^7-1 pseudorandom pattern
1	2^{15}-1 pseudorandom pattern
2	2^{20}-1 pseudorandom pattern
3	2^{23}-1 pseudorandom pattern

Digit	Meaning
4	Any 16-bit pattern
5	Illegal
6	Illegal
7	Illegal

BER Exponent Terminator

Any number in ASCII code between 2 and 9 inclusive. Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

Measurement Output

Place the MF-5 in TALK mode following GPIB protocol. The MF-5 will now send measurement and status data back to the GPIB controller when available. No prior module ID setup is necessary since the MF-5 interface will support only one GPIB talker module. Whenever a measurement is available, the MB-302 will load the measurement value and status bits into the MF-5 GPIB interface. If addressed to talk, the MF-5 GPIB interface will immediately send an 11-character (ASCII code) message containing a space between the status digit and measurement (including overflow) digits, followed by the terminators CR and LF.

STATUS DIGIT	SPACE	OVER-FLOW DIGIT	MSD	2nd	3rd	4th	5th	LSD	CR	LF

Definition of the digits are as follows:

STATUS DIGIT:

ASCII DIGIT	SYNC LOST	IN SYNC
0	FALSE	FALSE
1	FALSE	TRUE
2	TRUE	FALSE
3	TRUE	TRUE
+	FREQUENCY MEASUREMENT	
OTHER VALUES	ILLEGAL	

OVERFLOW DIGIT:

+	OVERFLOW TRUE
SPACE	OVERFLOW FALSE

MSD THRU LSD:

Decimal numbers, period, or minus sign

MEASUREMENT	FORMAT (MSD FIRST)
BIT ERROR RATE	A . BC - D
TOTALIZE	A B C D E F
FREQUENCY	A B C D E F (in kHz)

Measurements become available at the end of the measurement gating period. This happens automatically in all counter modes except TOTALIZE. For a TOTALIZE measurement, the gating period is infinite; thus, the MB-302 will not automatically generate a measurement output. The controller can request the current total error measurement by issuing a group execute trigger (GET) while the MF-5 is addressed to LISTEN. A service request will be generated if enabled.

Service Request Serial Poll

When the MB-302 has a measurement available, and the MF-5 is not addressed to talk, a service request (SRQ) will be generated if the SRQ INHIBIT switch on the rear panel of the MF-5 has not been set. This alerts the controller that a device on the bus needs service. The normal controller response would be a serial poll to determine which device needs service. When serial polled, the MF-5 will respond with 41 (hexadecimal) to indicate that it needs service. If the MF-5 does not need service it responds with 00 (hexadecimal).

When power is first turned on, the SRQ interrupt will normally be present if enabled at the rear of the MF-5 Mainframe. In the bit error-rate or frequency mode, this is caused by the termination of the first measurement. In the totalized mode the interface card and the MF-5 will load the data present at its input into its buffer. When power is turned on, either the mainframe rear-panel RESET button should be pushed, or an IEEE-488 IFC should be issued. SRQ may be cleared by issuing an IFC in bit error-rate or frequency modes. Of course, SRQ will be set again when the next measurement is completed. In the totalized mode the only way to clear the SRQ interrupt line is to address the MF-5 as a talker and turn off the ATN signal. No actual data transfer need take place, unless desired.

DISPLAY TIME Control

The DISPLAY TIME control, along with the other slide switches on the front panel of the MB-302, is not under remote/local control. All slide switches are always under local control. Care should be taken to see that the DISPLAY TIME control is set to either 1 second or 10 seconds when the MB-302 is under GPIB control. If the DISPLAY TIME control is set to hold, the MB-302 will not make continuous outputs to the GPIB controller. Measurements will stop after 1 measurement is taken, unless the GPIB controller issues a DCL or SDC bus command to initiate another measurement.

Manual Synchronization

When the GPIB controller places the MB-302 into the manual synchronization mode, it cannot initiate a manual synchronization attempt. This can only be done by pushing the front-panel MANUAL SYNC pushbutton, which is always active: independent of the remote/local mode.

Burst Mode

In local operation, the burst mode is indicated by the position of the external command pushbutton. Under GPIB control, the controller can place the MB-302 into either the burst or the non-burst mode. However, there is no way to indicate which mode has been selected on the front-panel of the MB-302 since the physical position of the external command pushbutton does not reflect the GPIB setting.

Manual Bit Error Rate

When the manual range-bit error-rate is selected by the GPIB controller, it can also select the exponent. The exponent will always be found by an automatic incrementation of the current exponent until it equals the exponent selected. The front-panel "up" exponent pushbutton is also disabled, but would interfere with the exponent selection if held. Therefore, when under GPIB control, do not push the front-panel "down" exponent select pushbutton.

Automatic Synchronization

When under local control, automatic synchronization also means automatic pattern selection. When under GPIB control, automatic synchronization does not mean automatic pattern selection. Pattern auto/synchronization selection under GPIB control is auto/synchronization only, not auto/pattern selection.

Changing Measurement Modes

When changing modes to make a new measurement, a sync or overflow error will occur. This is due to the previous measurement data being held in the output latch of the interface card.

Reset

It is recommended practice to reset (DCL, SDC) the MB-302 immediately after changing the COUNTER MODE or any control function to insure a valid measurement. If a reset is not issued, additional measurements of the previous counter mode will have to be accepted before measurements of the new counter mode are available. After a reset, a valid new measurement will be immediately available, except for the earlier software versions as described below.

GPIB Interface Card prior to serial number 8301001.

A measurement is almost always held in the software buffer, even after the hardware buffer (earlier version), has been cleared (per above). Consequently, in order to clear the buffer, an additional measurement of the previous mode must be accepted after the COUNTER MODE has been changed on the MB-302. This is especially true when changing from the FREQUENCY MODE to another mode; i.e., it becomes necessary to accept an additional frequency measurement whenever a FREQUENCY MODE change is made.

In the TOTALIZED MODE, however, a measurement will not usually be waiting in the software buffer unless commanded by a GET command, and not serviced. That is, measurement entry into the software buffer is to be under user control via the GET command. Therefore, it is up to the user to determine from his controller software, whether or not he has serviced the last commanded totalize transfer before changing to the COUNTER MODE. If he has, there will not be any totalize measurement in the buffer after the COUNTER MODE has been changed.

Similarly, when changing from either of the bit error rate modes to another mode, the occurrence of a measurement left in the software buffer will, as a rule, depend on the bit error rate range in manual, and on the actual bit error rate of the system in automatic.

Naturally, transfers to the software buffer will occur every time a valid bit error rate measurement is made. For example, in the manual bit error rate mode, these transfers will occur at the end of the measurment window as commanded by the user after setting the bit error rate exponent. In the automatic bit error rate mode, the end of the measurement window will depend on the actual error rate in the system under test. Therefore, it is not always possible to predict whether or not a bit error rate measurement will be left in the software buffer after the COUNTER MODE has been changed.

5.8 SERVICE

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

5.8.1 ROUTINE SERVICE

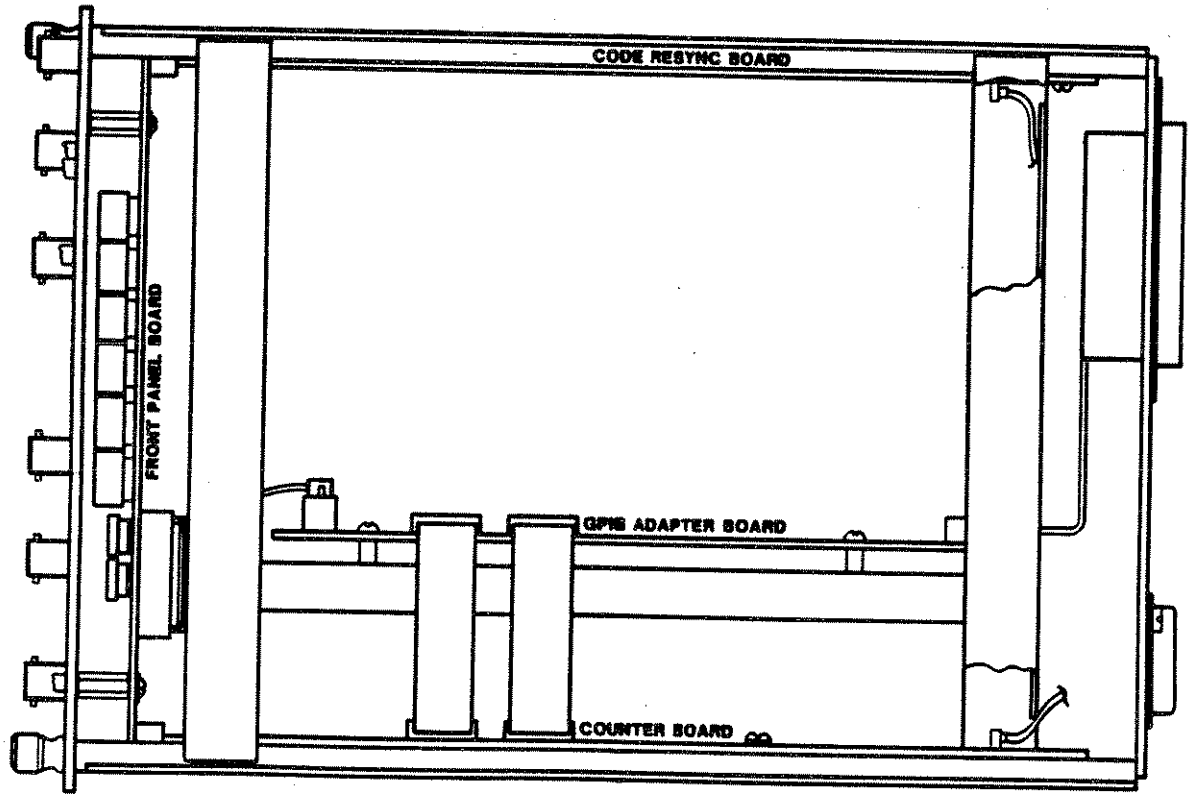
Routine service includes the performance of checks and service procedures which prevent or minimize the downtime of the unit. The checks and service are simplified, and may be limited to visual inspection for defective components, loose hardware and/or accumulation of dust within the unit at critical areas.

NOTE: It is recommended that periodic cleaning (approximately once every three months) of the interior and exterior of the unit be done with a vacuum cleaner.

Refer to Section 5.3, INSTALLATION, for module removal.

Board Seating

Ensure that all printed cicuit boards are securely seated in their connectors as shown in the illustration below.



MB-302

5.8.2 REPAIR RETURNS

For mechanical damage or electrical malfunctions, refer to Page ii, REPAIR RETURNS.

5.8.3 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617) 256-9013. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

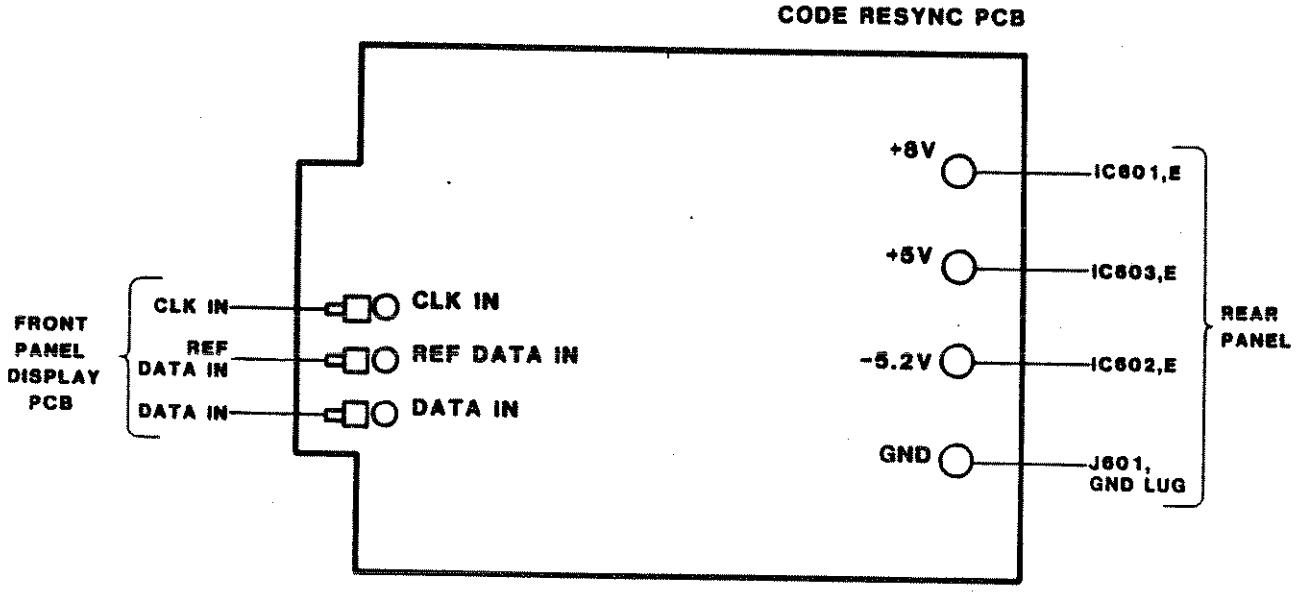
5.8.4 TROUBLE ANALYSIS

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

DC Voltages

WARNING: While measuring the -5.2V DC power supply, ensure that utmost care is taken. A power supply could be either severely damaged or completely destroyed if it is accidentally shorted to ground.

Verify that the DC votages are correct by measuring them on the Code Resync circuit board. Refer to the illustration below for the proper measurement points.



If the correct voltages are not indicated, consult the factory.

Calibration

Routine calibration is not normally required except in the following situations:

a. Failed component or circuit. Consult factory for further details.

b. Harsh environment; typical environment is:

Temperature	32 to 95°F (0 to 35°C)
Humidity	0 to 95% RH max at 20°C, non-condensing.

Any calibrations or technical adjustments other than the situations mentioned above should not be made during the Warranty period unless otherwise authorized. Consult factory for further details. (Refer to sections 5.2 and 5.5, SPECIFICATIONS and OPERATION, respectively, for proper switch, control, level and LED indicator settings.)

7. PARTS

7.1 REPLACEABLE PARTS

This section contains a listing of all electronic components and mechanical parts subject to normal wearout or failure. In the index shown below, table 7-1 is described. The table references the replaceable parts according to Tau-Tron Part no., description and quantity required.

Table	Description	Page
7-1	MB-302 BERT Receiver	7-3

TABLE 7-1

MB-302

BERT Receiver

MB302 BERT RECEIVER

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHC MET NO.4-40X5/16	8.000
8000-0071	SCREW PNHC MET NC.5-40X1/4	8.000
8000-0072	SCREW PNHC MET NO.5-40X3/8	8.000
8000-0614	SCREW FLTHD MET NO.4-40X5/16	12.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	8.000
8000-1203	LOCKWASHER NO.5 INT TOOTH	8.000
8000-9020	MODULE THUMBSCREW B-63013	2.000
9303-0004	PIN RECEPTACLE SNAP-ON	8.000
9303-0092A	HEX NUT FOR 9303-0092	6.000
9515-4424	MB302 FRONT PANEL ASSY	1.000
9525-4424	MB302 REAR PANEL ASSY	1.000
9545-4362	MB302 COUNTER PCB ASSY	1.000
9545-4364	MB302 CODE RESYNC PCB ASSY	1.000
9545-4431	MB302 BCD INTERFACE PCB ASSY	1.000
9555-4439	CABLE ASSY FLAT 16 POS	2.000
9705-4410	MODULE SIDE COVER	2.000
9705-4433	PCB HOLDER BRACKET	4.000
9705-4434	PC CARD HOLDER BRACKET	2.000
9705-4528	BERTS 325 MODULE RAILS	1.000

ME302 FRONT PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
9545-4359	ME302 F/P DISPLAY ED ASSY	1.000
9555-4559	CABLE ASSY COAXIAL	3.000
9705-4420	ME302 FRONT PANEL FINISHED	1.000
9725-4417	ME302 DISPLAY WINDOW	1.000
9735-6414	SPACER MET HEX 0.531 LG	4.000

ME302 REAR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-1300	RES COMP 3 OHM 5P 1/4W	1.000
0022-2120	RES COMP 12 OHM 5P 1/4W	1.000
0022-3150	RES COMP 150 OHM 5P 1/4W	1.000
0022-3300	RES COMP 300 OHM 5P 1/4W	2.000
1014-4610	CAP CER 0.1 MFD 20P 200V	2.000
1024-5110	CAP ELEC 1 MFD 35WVDC	3.000
1024-5147	CAP ELEC 4.7 MFD 20P 35WVDC	1.000
1024-5210	CAP ELEC 10 MFD 35WVDC	2.000
2101-4001	DIODE RECTIFIER 1N4001	2.000
3180-3055	TRNSTR NPN POWER 2N3055	1.000
4200-340K5	IC LINEAR REGULATOR LM340K5	2.000
4201-320K5	IC LINEAR REGULATOR LM320K5	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	2.000
8000-0047	SCREW PNHD MET NO.4-40X1/2	10.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	8.000
8000-1002	NUT HEX MET NO.4-40	12.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	5.000
8000-1302	FLAT WASHER MET NO.4	4.000
8000-1506	LUG SOLDER ANGLE NO.4	7.000
8000-6000	BUSHING INSULATING TO-3	8.000
8000-6001	WASHER INSULATING TO-3	4.000
8000-6002	SOCKET TO-3 MOUNTING	4.000
9300-0103	CONN PLUG PANEL MNT 24 POS	1.000
9555-4440	CABLE ASSY FLAT 50 POS	1.000
9705-4426	ME302 REAR PANEL MACHINED	1.000

ME302 F/P DISPLAY BD ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-1560	RES COMP 5.6 OHM 5P 1/8W	2.000
0012-2330	RES COMP 33 OHM 5P 1/8W	6.000
0012-2470	RES COMP 47 OHM 5P 1/8W	2.000
0012-2510	RES COMP 51 OHM 5P 1/8W	2.000
0012-3120	RES COMP 120 OHM 5P 1/8W	7.000
0012-3160	RES COMP 160 OHM 5P 1/8W	1.000
0012-3220	RES COMP 220 OHM 5P 1/8W	12.000
0012-3270	RES COMP 270 OHM 5P 1/8W	3.000
0012-3390	RES COMP 390 OHM 5P 1/8W	2.000
0012-3470	RES COMP 470 OHM 5P 1/8W	5.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	4.000
0012-4470	RES COMP 4.7 KOHM 5P 1/8W	2.000
0012-4510	RES COMP 5.1 KOHM 5P 1/8W	1.000
0012-6200	RES COMP 200 KOHM 5P 1/8W	1.000
0022-2510	RES COMP 51 OHM 5P 1/4W	6.000
0022-3750	RES COMP 750 OHM 5P 1/4W	2.000
0333-2100	RES VAR 10 OHM 10P 1/2W	2.000
0333-3500J	RES VAR 500 OHM 10P 1/2W	2.000
0333-4100T	RES VAR 1 KOHM 10P 1/2W	2.000
1013-8510	CAP CER .01 MFD 20P 200V	7.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	17.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	4.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	4.000
1084-4710	CAP CHIP .01 MFD 50WVDC	4.000
2112-4148	DIODE GEN PURPOSE IN4148	2.000
2274-5274	DIODE LED GREEN MV5274C	2.000
2274-5374	DIODE LED YELLOW MV5374C	9.000
2274-5774	DIODE LED RED MV5774C	5.000
3224-4401	TRNSTR NPN AMPLIFIER 2N4401	6.000
3224-4403	TRNSTR NPN AMPLIFIER 2N4403	2.000
4012-4490	IC CMOS MC14490BCP PLSTC	1.000
4012-4520	IC CMOS MC14520BCP PLSTC	1.000
4012-74C912	IC CMOS MM74C912	1.000
4012-74LS08	IC TTL SN74LS08N PLSTC	2.000
4012-74S139	IC TTL SN74S139N PLSTC	2.000
4012-7408	IC TTL SN7408N PLSTC	1.000
4513-0308	IC DISPLAY TIL308	1.000
4513-7653	IC DISPLAY HP 5082-7653	6.000
4513-7736	IC DISPLAY HP 5082-7736	1.000
8000-2403	SPACER INSL CLRNC 4 X 7/16	16.000
9201-0003	SWITCH SLIDE DP4T SS24	1.000
9201-0007	SWITCH SLIDE DPDT MSSA2350	3.000
9205-0011	SWITCH PB MAINTAINED LTD YEL	1.000
9205-0012	SWITCH PB MOMENTARY LTD YEL	7.000
9300-0030	SOCKET IC 16 PIN LOW PROFILE	1.000
9300-0048	SOCKET IC 14 PIN LOW PROFILE	7.000
9303-0081	CONN EDGE DUAL 22 POS PC MNT	1.000
9303-0082	CONN EDGE DUAL 35 POS PC MNT	1.000

M8302 F/P DISPLAY BD ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9303-0092	BNC RECEPTACLE PCB MNT	6.000
9306-0004	SOCKET PIN LOW PROFILE	24.000
9306-0034	CONN PCB HDR MALE STRT 20 PCS	1.000
9306-0035	CONN SOCKET FEMALE 20 POS	1.000
9565-9083	MASSOM MCKT ASSY	2.000
96ART-54358	M8302 FRONT PANEL DISPLAY PCB	1.000
96SCH-54357	M8302 FRONT PANEL DISPLAY	1.000
9605-4358	M8302 FRONT PANEL DISPLAY PCB	1.000

MB302 CCUNTER PCB ASSY

CCMPONENT ITEM NO.	DESCRIPTICN	QLANTITY PER
0012-3180	RES CCMP 180 OHM 5P 1/8W	2.0CC
0012-3390	RES CCMP 390 OHM 5P 1/8W	2.0CC
0012-4100	RES CCMP 1 KOHM 5P 1/8W	10.0CC
0012-4200	RES CCMP 2 KOHM 5P 1/8W	16.0CC
0012-4470	RES CCMP 4.7 KOHM 5P 1/8W	1.0CC
0012-4510	RES CCMP 5.1 KOHM 5P 1/8W	1.0CC
0012-5100	RES CCMP 10 KOHM 5P 1/8W	1.0CC
0012-5510	RES CCMP 51 KOHM 5P 1/8W	1.0CC
1013-8310	CAP CER 100 PF 20P 200V	2.0CC
1013-8322	CAP CER 220 PF 20P 200V	1.0CC
1013-8347	CAP CER 470 PF 20P 200V	1.0CC
1013-8510	CAP CER .01 MFD 20P 200V	30.0CC
1064-0847	CAP MIN-TANT 47 MFD 6WVCC	2.0CC
1064-1233	CAP MIN-TANT 33 MFD 10WVCC	2.0CC
2112-4148	DICDE GEN PURPOSE IN4148	3.0CC
4012-4072	IC CMOS MC14072BCP PLSTC	1.0CC
4012-74LS00	IC TTL SN74LS00N PLSTC	2.0CC
4012-74LS04	IC TTL SN74LS04N PLSTC	2.0CC
4012-74LS08	IC TTL SN74LS08N PLSTC	5.0CC
4012-74LS123	IC TTL SN74LS123N PLSTC	1.0CC
4012-74LS138	IC TTL SN74LS138N PLSTC	1.0CC
4012-74LS151	IC TTL SN74LS151N PLSTC	1.0CC
4012-74LS157	IC TTL SN74LS157N PLSTC	3.0CC
4012-74LS161	IC TTL SN74LS161N PLSTC	2.0CC
4012-74LS192	IC TTL SN74LS192N PLSTC	1.0CC
4012-74LS257	IC TTL SN74LS257N PLSTC	6.0CC
4012-74LS32	IC TTL SN74LS32N PLSTC	3.0CC
4012-74LS490	IC TTL SN74LS490N PLSTC	9.0CC
4012-74LS74	IC TTL SN74LS74N PLSTC	5.0CC
4012-74276	IC TTL SN74276N PLSTC	2.0CC
4012-74390	IC TTL SN74390N PLSTC	1.0CC
4160-0555	IC LINEAR NE555N	1.0CC
9080-1001	OSC 1 MHZ 14 PIN DIP	1.000
9300-0048	SCCKET IC 14 PIN LOW PRCFILE	1.0CC
9303-0003	CCNN POST MALE	2.000
9306-0012	CCNN PCB HCR 16 PIN 0.062 PCB	2.0CC
9314-0011	STIK POST C.10 CTRS	6.0CC
9314-0012	JUMPER FOR STIK PCST C.10 CTRS	2.000
96ART-54361	MB302 CCUNTER PCB	1.0CC
96SCH-54360	MB302 CCUNTER	1.0CC
9605-4361	MB302 CCUNTER PCB	1.0CC

MB302 CODE RESYNC PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-2510	RES COMP 51 OHM 5P 1/8W	11.000
0012-2750	RES COMP 75 OHM 5P 1/8W	3.000
0012-3100	RES COMP 100 OHM 5P 1/8W	74.000
0012-3470	RES COMP 470 OHM 5P 1/8W	14.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	11.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	1.000
0022-2750	RES COMP 75 OHM 5P 1/4W	1.000
0022-3120	RES COMP 120 OHM 5P 1/4W	1.000
0333-4100T	RES VAR 1 KOHM 10P 1/2W	2.000
0822-3100	RES SIP 8PIN 100 OHM 2P 0.3W	8.000
0822-3470	RES SIP 8PIN 470 OHM 2P 0.3W	2.000
1013-8510	CAP CER .01 MFD 20P 200V	67.000
1014-8410	CAP CER 1000 PF 20P 200V	3.000
1024-5110	CAP ELEC 1 MFD 35WVDC	2.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	6.000
1064-3747	CAP MIN-TANT 4.7 MFD 20WVDC	1.000
1084-4710	CAP CHIP .01 MFD 50WVDC	8.000
2112-4148	DIODE GEN PURPOSE IN4148	1.000
4012-10H116	IC ECL MC10H116P PLSTC DIP	1.000
4012-10016	IC ECL F10016DC CER	1.000
4012-10102	IC ECL MC10102P PLSTC	4.000
4012-10105	IC ECL MC10105P PLSTC	1.000
4012-10124	IC ECL MC10124P PLSTC	3.000
4012-10125	IC ECL MC10125P PLSTC	3.000
4012-10131	IC ECL MC10131P PLSTC	1.000
4012-10141	IC ECL MC10141P PLSTC	5.000
4012-10178	IC ECL MC10178P PLSTC	1.000
4012-10198	IC ECL MC10198P PLSTC	1.000
4012-10211	IC ECL MC10211P PLSTC	2.000
4012-10212	IC ECL MC10212P PLSTC	1.000
4012-10231	IC ECL MC10231P PLSTC	6.000
4012-11C70	IC ECL F11C70DC CER	1.000
4012-1662L	IC ECL MC1662L CER	4.000
4012-1672L	IC ECL MC1672L CER	1.000
4012-1678L	IC ECL MC1678L CER	2.000
4012-1688F	IC ECL MC1688F CER	4.000
4012-1692L	IC ECL MC1692L CER	1.000
4055-0102	IC ECL F100102FC	1.000
4055-0131	IC ECL F100131FC	1.000
4201-337T	IC LINEAR REGULATOR LM337T	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	1.000
8000-1002	NUT HEX MET NO.4-40	1.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	1.000
9100-0116	HEAT SINK FOR TAB MNT TRNSTR	1.000
9301-0060A	CONN COAXIAL PCB MNT	3.000
9303-0003	CONN POST MALE	4.000
96ART-54365	MB302 CODE RESYNC PCB	1.000
96SCH-54364	MB302 CODE RESYNC	1.000
9605-4365	MB302 CODE RESYNC PCB	1.000

MB302 BCD INTERFACE PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-3100	RES COMP 100 OHM 5P 1/4W	1.000
0022-3180	RES COMP 180 OHM 5P 1/4W	4.000
0022-3390	RES COMP 390 OHM 5P 1/4W	4.000
0022-4200	RES COMP 2 KOHM 5P 1/4W	13.000
0022-5100	RES COMP 10 KOHM 5P 1/4W	3.000
0333-61008	RES VAR 100 KOHM 10P 1.25W	2.000
1013-8233	CAP CER 33 PF 20P 200V	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	6.000
1014-8410E	CAP CER 1000 PF 20P 100V 0.1SP	1.000
1064-1233	CAP MIN-TANT 33 MFD 10WVCC	1.000
1064-3747	CAP MIN-TANT 4.7 MFD 20WVCC	2.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS02	IC TTL SN74LS02N PLSTC	3.000
4012-74LS04	IC TTL SN74LS04N PLSTC	2.000
4012-74LS11	IC TTL SN74LS11N PLSTC	1.000
4012-74LS123	IC TTL SN74LS123N PLSTC	2.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	3.000
4012-74LS175	IC TTL SN74LS175N PLSTC	6.000
4012-74LS74	IC TTL SN74LS74N PLSTC	1.000
4012-74LS76A	IC TTL SN74LS76AN PLSTC	1.000
4012-7407	IC TTL SN7407N PLSTC	1.000
9303-0003	CONN POST MALE	2.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	2.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
96ART-54430	MB302 BCD INTERFACE PCB	1.000
96SCH-54429	MB302 BCD INTERFACE	1.000
9605-4430	MB302 BCD INTERFACE PCB	1.000

MB302 GPIB OPTION KIT

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9545-4543	MB302 GPIB ADAPTER PCB ASSY	1.000
9555-4552	CABLE ASSY FLAT 20 PCS	1.000

ME302 GPIE ADAPTER PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-3100	RES CCMP 100 CHM 5P 1/8W	1.000
0012-3180	RES CCMP 180 CHM 5P 1/8W	4.000
0012-3390	RES CCMP 390 OHM 5P 1/8W	4.000
0012-4300	RES CCMP 3 KOHM 5P 1/8W	25.000
0012-4510	RES CCMP 5.1 KOHM 5P 1/8W	2.000
1013-8315	CAP CER 150 PF 10P 200V	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	19.000
1014-8210	CAP CER 10 PF 20P 200V	1.000
1014-8410	CAP CER 1000 PF 20P 200V	1.000
1064-1233	CAP MIN-TANT 33 MFD 10WVCC	1.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS02	IC TTL SN74LS02N PLSTC	1.000
4012-74LS04	IC TTL SN74LS04N PLSTC	2.000
4012-74LS11	IC TTL SN74LS11N PLSTC	1.000
4012-74LS123	IC TTL SN74LS123N PLSTC	1.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	7.000
4012-74LS174	IC TTL SN74LS174N PLSTC	2.000
4012-74LS175	IC TTL SN74LS175N PLSTC	7.000
4012-74LS74	IC TTL SN74LS74N PLSTC	1.000
4012-74LS76A	IC TTL SN74LS76AN PLSTC	1.000
4012-7407	IC TTL SN7407N PLSTC	1.000
4012-7485	IC TTL SN7485N PLSTC	2.000
9303-0003	CONN POST MALE	2.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCE	2.000
9306-0039	CONN PCE HDR MALE 50 POS	1.000
9306-0044	CONN PCB HDR MALE RTAGL 20 POS	1.000
9314-0011	STIK POST 0.10 CTRS	3.000
9314-0012	JUMPER FOR STIK POST 0.10 CTRS	3.000
96ART-54482	GPIB ADAPTER PCE	1.000
96SCH-54481	GPIB ADAPTER	1.000
9605-4482	GPIB ADAPTER PCB	1.000

8. DIAGRAMS

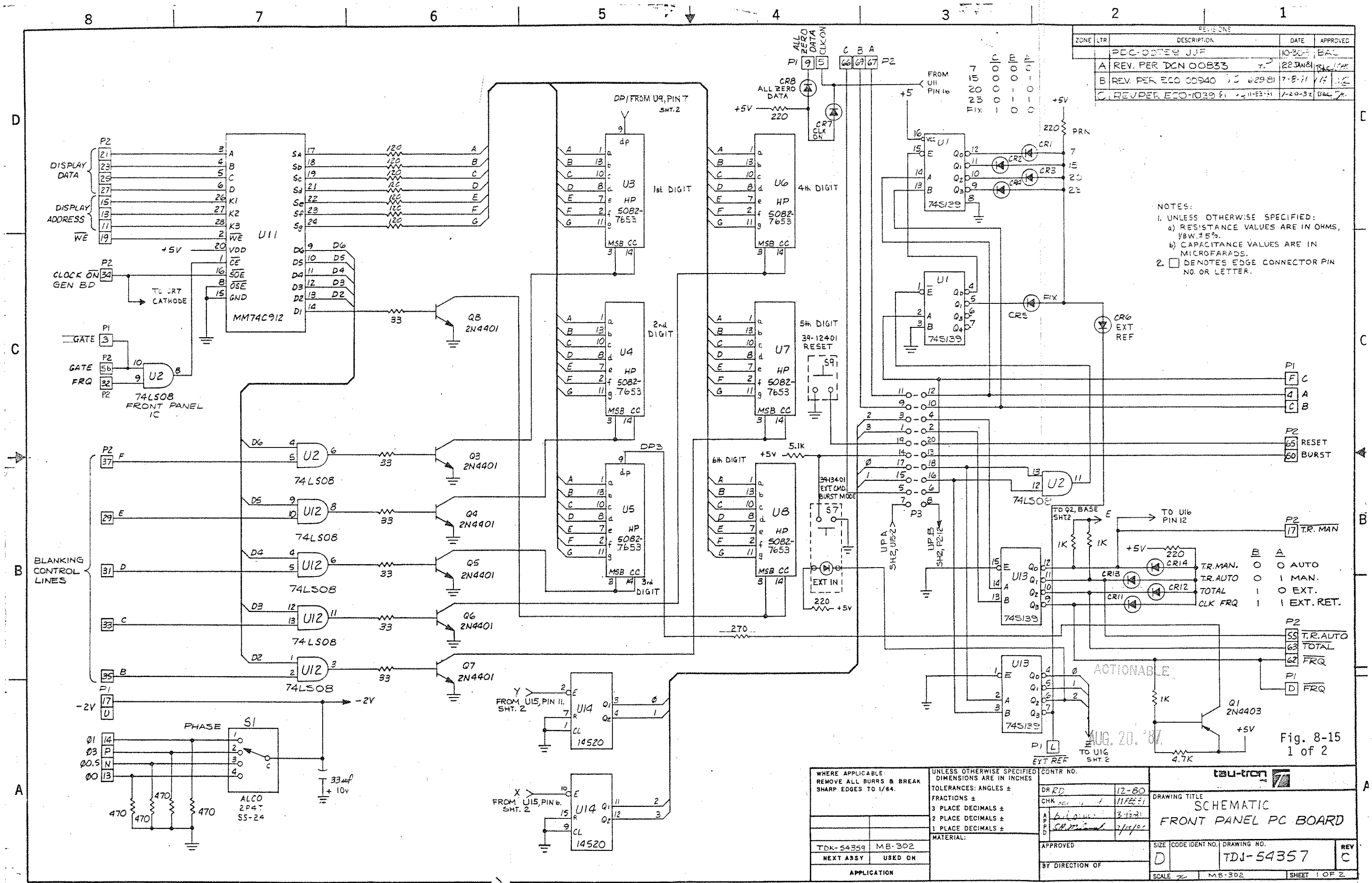
8.1 GENERAL

This section contains Block and Schematic diagrams for the MB-302 module. Figures are given in the table below.

TABLE 8-1

DIAGRAMS

Figure	Description
8-14	MB-302 Block Diagram
8-15	MB-302 Front-Panel Schematic
8-16	MB-302 Code ReSync Schematic
8-17	MB-302 BCD Interface Schematic
8-18	MB-302 Counter Board Schematic
8-19	MB-302 Power Supply Schematic
8-20	MB-302 GPIB Adapter Schematic



REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
PDC-00769 JJF | 10-30-79 | BAC
A | REV. PER DCN 00833 | 22 JAN 81
B | REV. PER ECO 00940 | 6-29-81 | 7-8-81
C | REV PER ECO-1039 | 11-23-81 | 1-20-82
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%.
b) CAPACITANCE VALUES ARE IN MICROFARADS.
2. ☐ DENOTES EDGE CONNECTOR PIN NO. OR LETTER.
DISPLAY DATA
DISPLAY ADDRESS
CLOCK ON GEN BD
TO CRT CATHODE
GATE
FRQ
74LS08 FRONT PANEL IC
BLANKING CONTROL LINES
PHASE
ALCO 2P4T SS-24
33uf + 10v
DP1 FROM U9, PIN 7 SHT. 2
1st DIGIT
2nd DIGIT
3rd DIGIT
4th DIGIT
5th DIGIT
6th DIGIT
39-12401 RESET
39-13401 EXT CMD BURST MODE
EXT IN
ALL ZERO DATA
CLK ON
FROM U11 PIN 16
PRN
FIX
CR6 EXT REF
RESET
BURST
T.R. MAN
T.R. AUTO
TOTAL
FRQ
TO U16 PIN 12
TO Q2, BASE SHT. 2
TO U16 SHT. 2
EXT REF
T.R. MAN. 0 0 AUTO
T.R. AUTO 0 1 MAN.
TOTAL 1 0 EXT.
CLK FRQ 1 1 EXT. RET.
ACTIONABLE
AUG. 20. '87
WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:
TDK-54359 | MB-302
NEXT ASSY | USED ON
APPLICATION
CONTR NO.
DR RD 12-80
CHK 11 FEB 81
APPROVED
BY DIRECTION OF
tau-tron
DRAWING TITLE
SCHEMATIC
FRONT PANEL PC BOARD
SIZE D
CODE IDENT NO.
DRAWING NO. TDJ-54357
REV C
SCALE
MB-302
SHEET 1 OF 2

Fig. 8-15
1 of 2

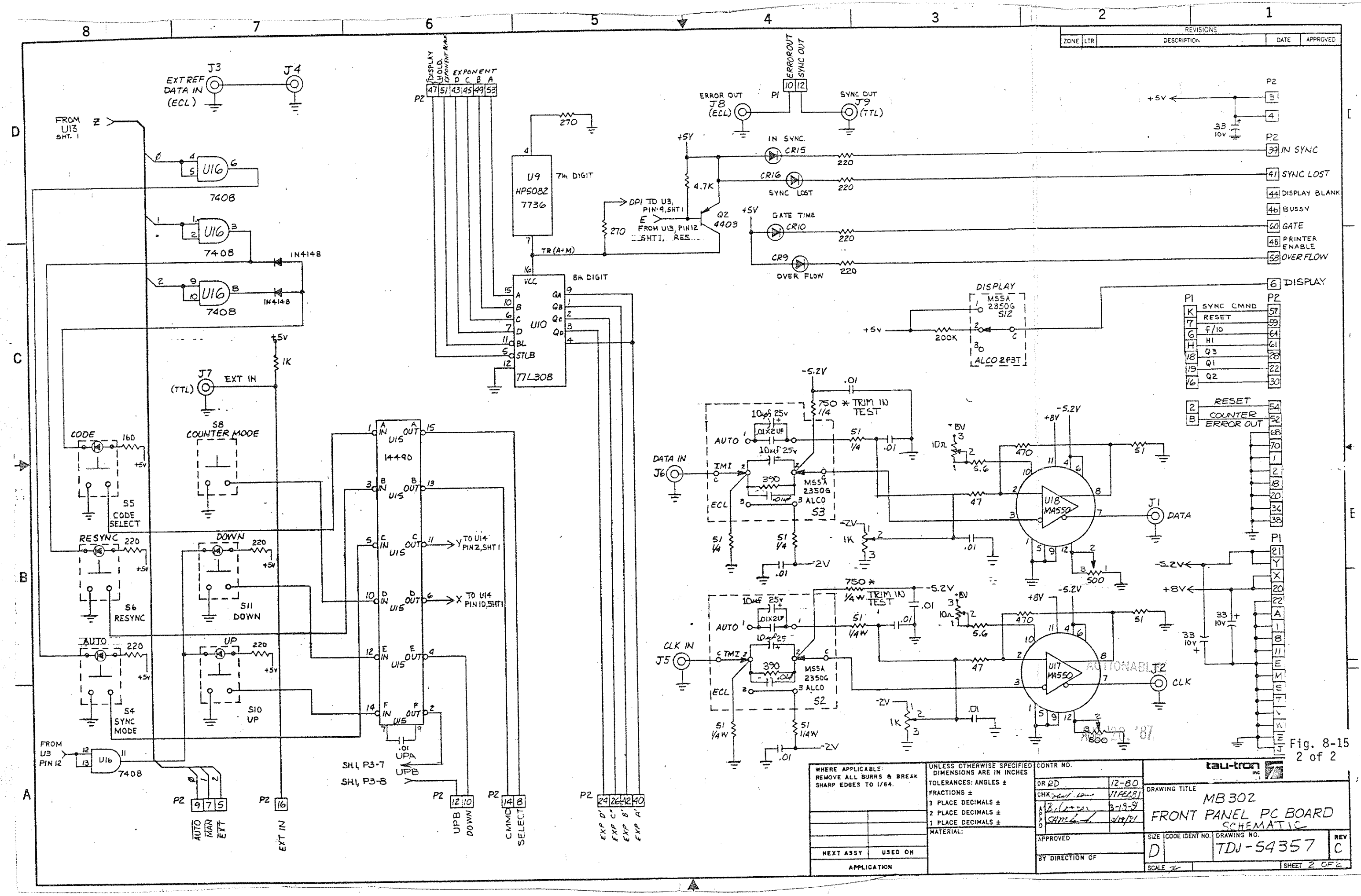


Fig. 8-15
2 of 2

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

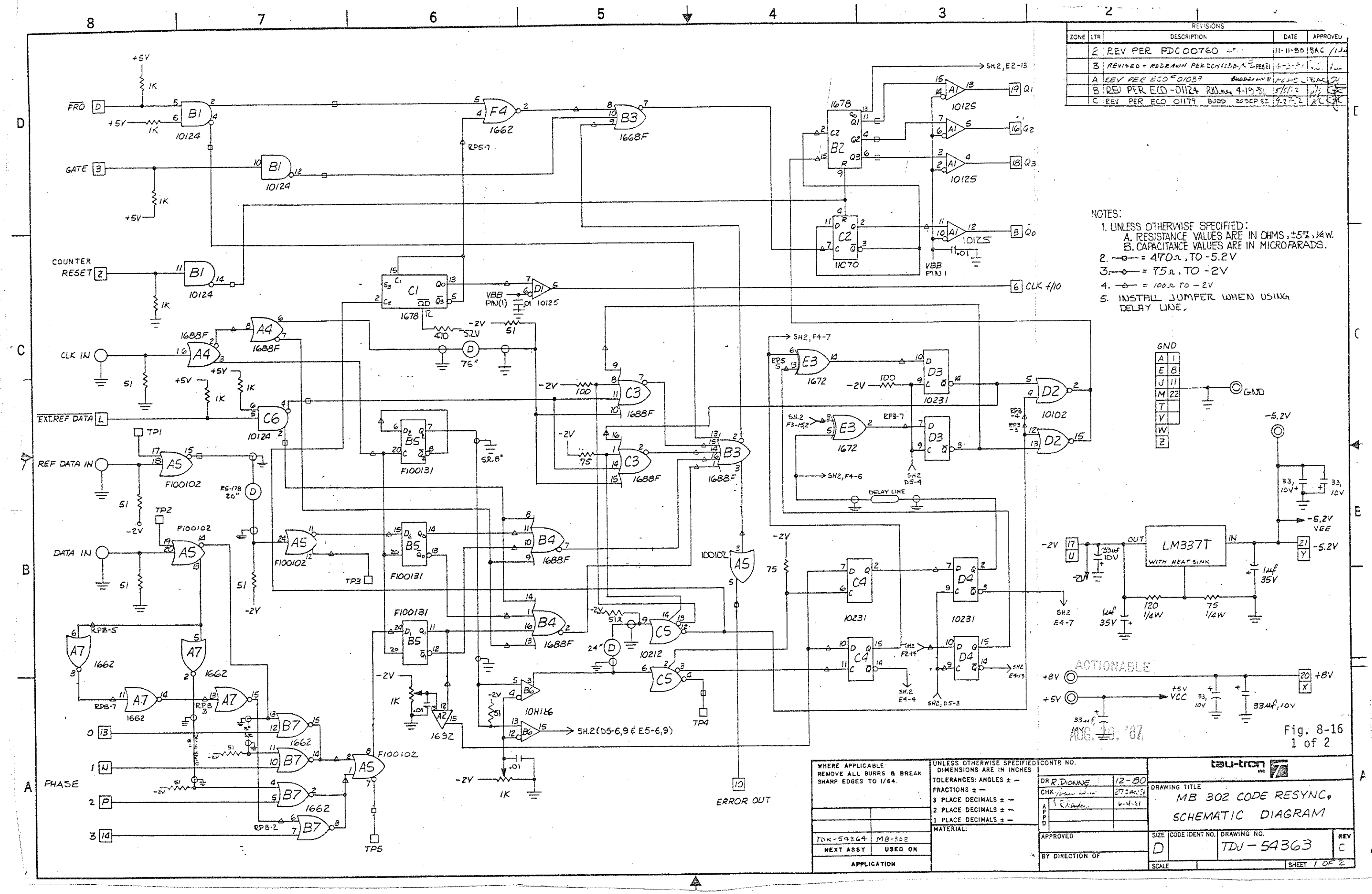
NEXT ASSY | USED ON
APPLICATION

CONTR NO.
DR RD 12-80
CHK 11 FEB 81
APPD 3-19-81
APPROVED
BY DIRECTION OF

tau-tron inc

DRAWING TITLE
MB 302
FRONT PANEL PC BOARD
SCHEMATIC

SIZE D | CODE IDENT NO. | DRAWING NO. TDJ-54357 | REV C
SCALE | SHEET 2 OF 2



REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
2 | REV PER PDC00760 | 11-11-80 | BAC
3 | REVISED + REDRAWN PER DCN 02310 | 6-3-81
A | REV PER ECO #01037 | BUDD 20 JAN 81
B | REV PER ECO-01124 | 4-19-82
C | REV PER ECO 01179 | BUDD 20 SEP 82
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W.
B. CAPACITANCE VALUES ARE IN MICROFARADS.
2. = 470Ω, TO -5.2V
3. = 75Ω, TO -2V
4. = 100Ω TO -2V
5. INSTALL JUMPER WHEN USING DELAY LINE.
FRQ
GATE
COUNTER RESET
CLK IN
EXT.REF DATA
REF DATA IN
DATA IN
PHASE
ERROR OUT
CLK f/10
GND
LM337T
WITH HEAT SINK
DELAY LINE
SH.2(D5-6,9 & E5-6,9)
ACTIONABLE
AUG. 19, '87
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± —
2 PLACE DECIMALS ± —
1 PLACE DECIMALS ± —
MATERIAL:
TDK-54364 | MB-302
NEXT ASSY | USED ON
APPLICATION
CONTR NO.
DR R. DIONNE 12-80
CHK 27 JAN 81
APPD 6-4-81
APPROVED
BY DIRECTION OF
tau-tron inc
DRAWING TITLE
MB 302 CODE RESYNC, SCHEMATIC DIAGRAM
SIZE D
CODE IDENT NO.
DRAWING NO. TDJ-54363
REV C
SCALE
SHEET 1 OF 2

Fig. 8-16
1 of 2

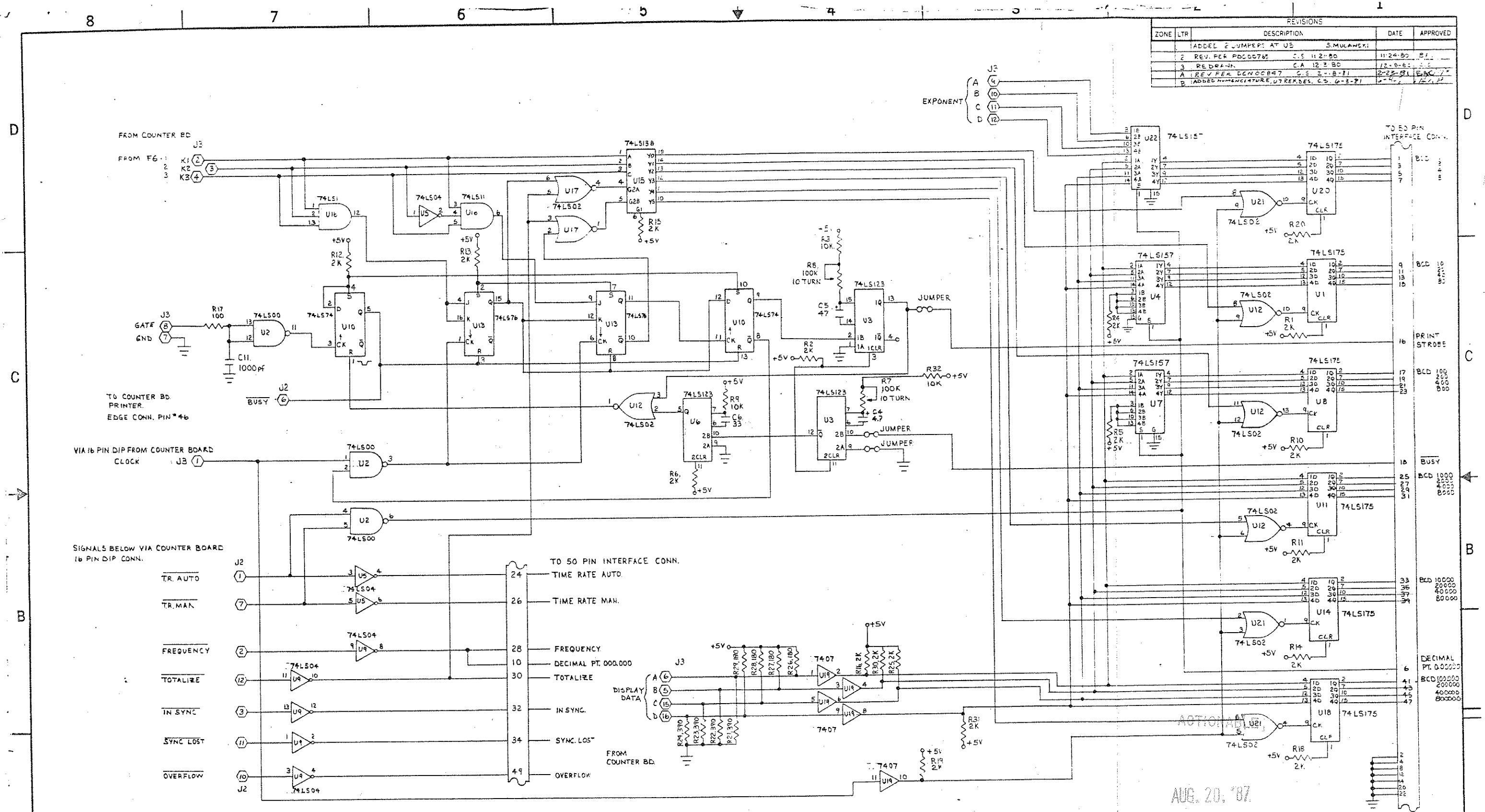
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SH. 1		

CODE SELECT
A 4
B C
C F
1000 PF
1K
+5V
SH1 (B2-13)
SYNC ERROR COUNTER RESET 7
RESYNC COMMAND IN K
R65 470
IN4148
-2V
51
SH1 B6-15
G3-4
F2-4
F3-9
F5-9
G5-4
G4-4
SHT1 D3-9
SHT1 D4-9
F6-4
RG178 10"
-5.2V
10K
4.7
.01
RP1-4
VBB PIN1
CLK ON 5
HIGH H
"77" RG-178
E5-3
E5-2
E5-12
E5-13
E5-4
SH1 E3-3
SH1 D4-3
SH1 C4-14
SH1 B4-14
SH1 E3-5
SH1 E3-6
S-1 D4-10
SEE NOTE 5
100
-2V
RESISTOR PACK LOCATION F-3/4
TP
ALL ZERO DATA
SYNC OUT
VBB PIN(1)
RP4-5
RP4-7
RP4-2
RP4-3
RP3-6
RP3-5
RP6-6
RP6-7
RP5-3
RP5-2
RP5-6
RP5-4
RP7-6
RP7-5
RP7-7
RP7-3
RP7-4
RP2-5
RP2-7
RP2-4
RP2-6
RP2-3
RP1-2
RP1-6
RP1-8
RP1-11
ER1-3
ES-14
DS-13
10124
10102
10231
10105
10125
10131
10141
10211
10198
10178
1662
1672
F1016
G3
G4
G5
G6
F2
F4
F5
F6
F7
G7
E1
E2
E3
E4
E5
E6
E7
C6
C7
D2
D5
D6
D7
F1
F3
DI
1K
10" 51 .01

AUG. 20. '87

Fig. 8-16
2 of 2

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.	tau-tron inc
TDK-54364 / MB302 NEXT ASSY / USED ON		DR R. DIONNE 12-80 CHK [illegible] 27 JAN 3 APPD	DRAWING TITLE: MB 302 CODE RESYNC. SCHEMATIC DIAGRAM
APPLICATION		APPROVED BY DIRECTION OF	SIZE D · CODE IDENT NO. · DRAWING NO. TDU-54363 · REV C SCALE — · MB-302 · SHEET 2 OF 2



LAST REF. DES. USED	UNUSED
U22	
R32	
C11	
J3	J1

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE VALUES ARE IN OHMS 1/4 W, ± 5%.
   b) CAPACITANCE VALUES ARE IN MICROFARADS.
2. 74LS76 DOES NOT USE STANDARD VOLTAGE PIN OUT.
3. ◯ DENOTES 16 PIN CONNECTOR.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
		ADDED 2 JUMPERS AT U3 S. MULAWSKI		
	2	REV. PER PDC00765 C.S. 11-21-80	11-24-80	
	3	REDRAWN C.A. 12-3-80	12-8-80	
	A	REV PER DCN00847 C.S. 2-18-81	2-23-81	
	B	ADDED NOMENCLATURE, U7 REF. DES. C.S. 6-3-81		

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

NEXT ASSY	USED ON
TDK-54431	MB-302

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

CONTR NO.
DR C. ATHERTON 12-3-80
CHK 12-9-80
APPD
APPROVED
BY DIRECTION OF

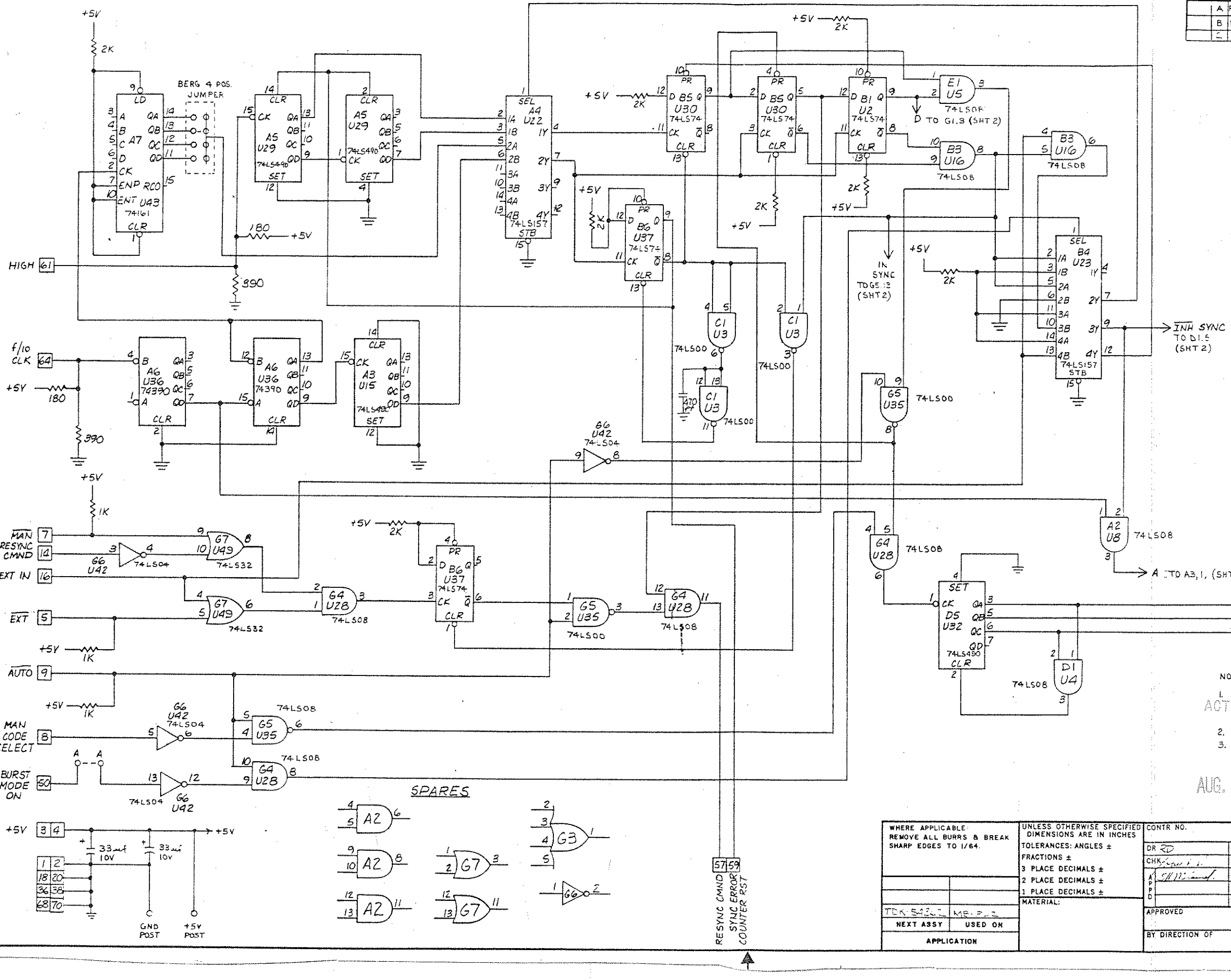
tau-tron inc

DRAWING TITLE
BCD INTERFACE SCHEMATIC
Fig. 8-17
1 of 1

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		TDJ-54429	E

SCALE MB-302 SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER DRAWING RELEASE (ECO D0284-0)		
	B	REV PER ECO D0284-0	6/23/81	
	C	REV PER ECO D0332 C.Nunes 12/23/81	12 DEC 81	



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE VALUES ARE IN OHMS, 1/8W, ± 5 %.
   b) CAPACITANCE VALUES ARE IN MICROFARDS.
2. ⬡ DENOTES J2,J3 CONNECTORS.
3. ☐ DENOTES EDGE CONNECTOR.

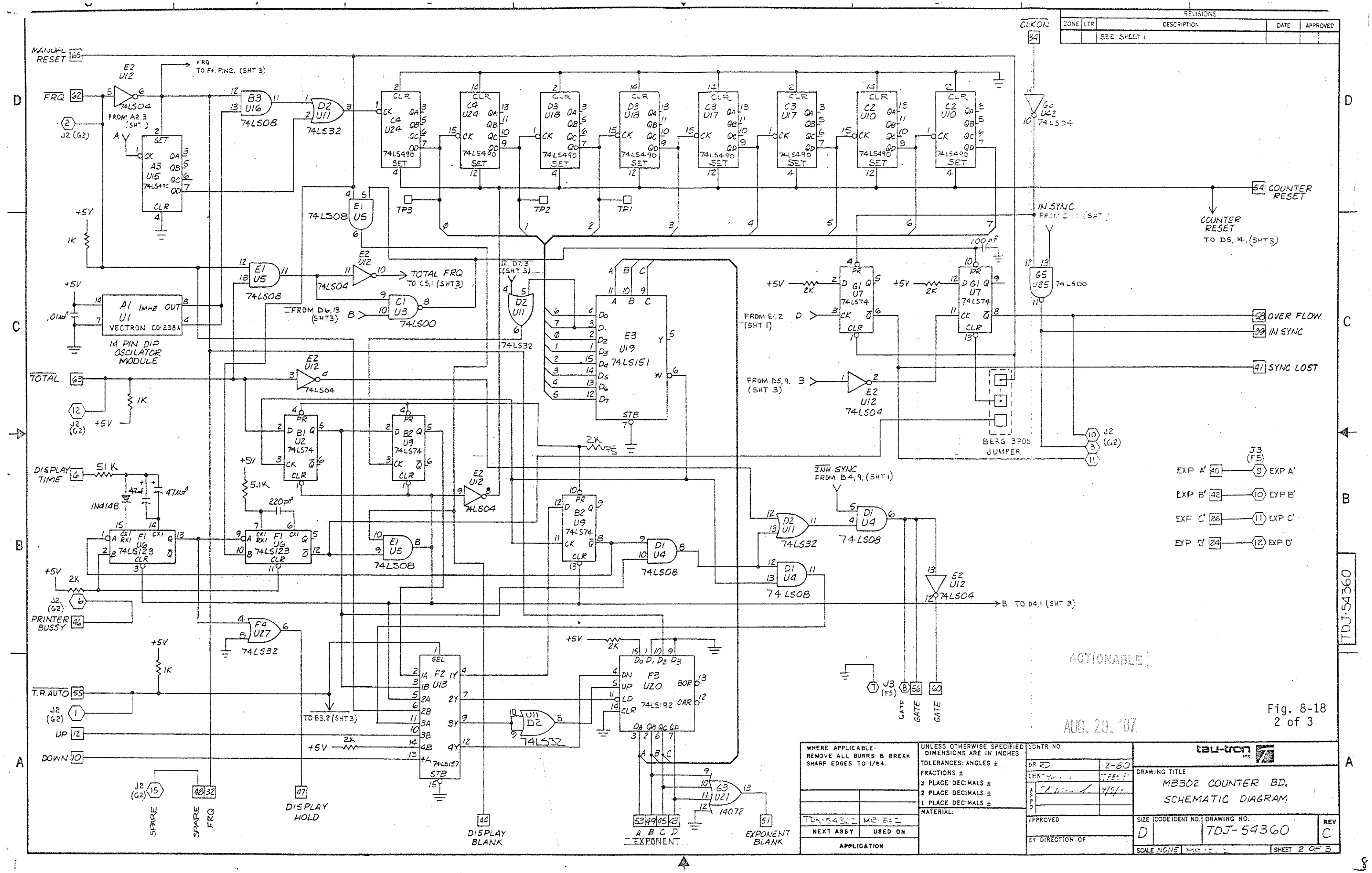
ACTIVE RESISTANCE

AUG. 20, '87

Fig. 8-18
1 of 3

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.	tau-tron inc
TDK 54360 / MB-P-3		DR RD 12-80	DRAWING TITLE MB302 COUNTER BD, SCHEMATIC DIAGRAM
NEXT ASSY / USED ON		CHK 11 FEB 81	
APPLICATION		APPD 4/5/81	
		APPROVED	SIZE D / CODE IDENT NO. / DRAWING NO. TDJ-54360 / REV C
		BY DIRECTION OF	SCALE — / SHEET 1 OF 3

TDJ-54360



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
SEE SHEET 1
MANUAL RESET
FRQ
TOTAL
DISPLAY TIME
PRINTER BUSSY
T.R. AUTO
UP
DOWN
SPARE
SPARE FRQ
DISPLAY HOLD
DISPLAY BLANK
EXPONENT
EXPONENT BLANK
14 PIN DIP OSCILATOR MODULE
VECTRON CO-238A
TOTAL FRQ TO C5,1 (SHT3)
FROM D6,13 (SHT3)
FROM E1,2 (SHT 1)
FROM D5,9 (SHT 3)
IN SYNC
COUNTER RESET
COUNTER RESET TO D5,14 (SHT3)
OVER FLOW
IN SYNC
SYNC LOST
BERG 3POS JUMPER
INH SYNC FROM B4,9 (SHT 1)
B TO D4,1 (SHT 3)
TO B3,2 (SHT 3)
EXP A'
EXP B'
EXP C'
EXP D'
GATE
ACTIONABLE
AUG. 20. '87
TDJ-54360
WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:
NEXT ASSY
USED ON
APPLICATION
CONTR NO.
DR RD 2-80
APPROVED
BY DIRECTION OF
tau-tron inc
DRAWING TITLE
MB302 COUNTER BD. SCHEMATIC DIAGRAM
SIZE D
CODE IDENT NO.
DRAWING NO. TDJ-54360
REV C
SCALE NONE
SHEET 2 OF 3

Fig. 8-18
2 of 3

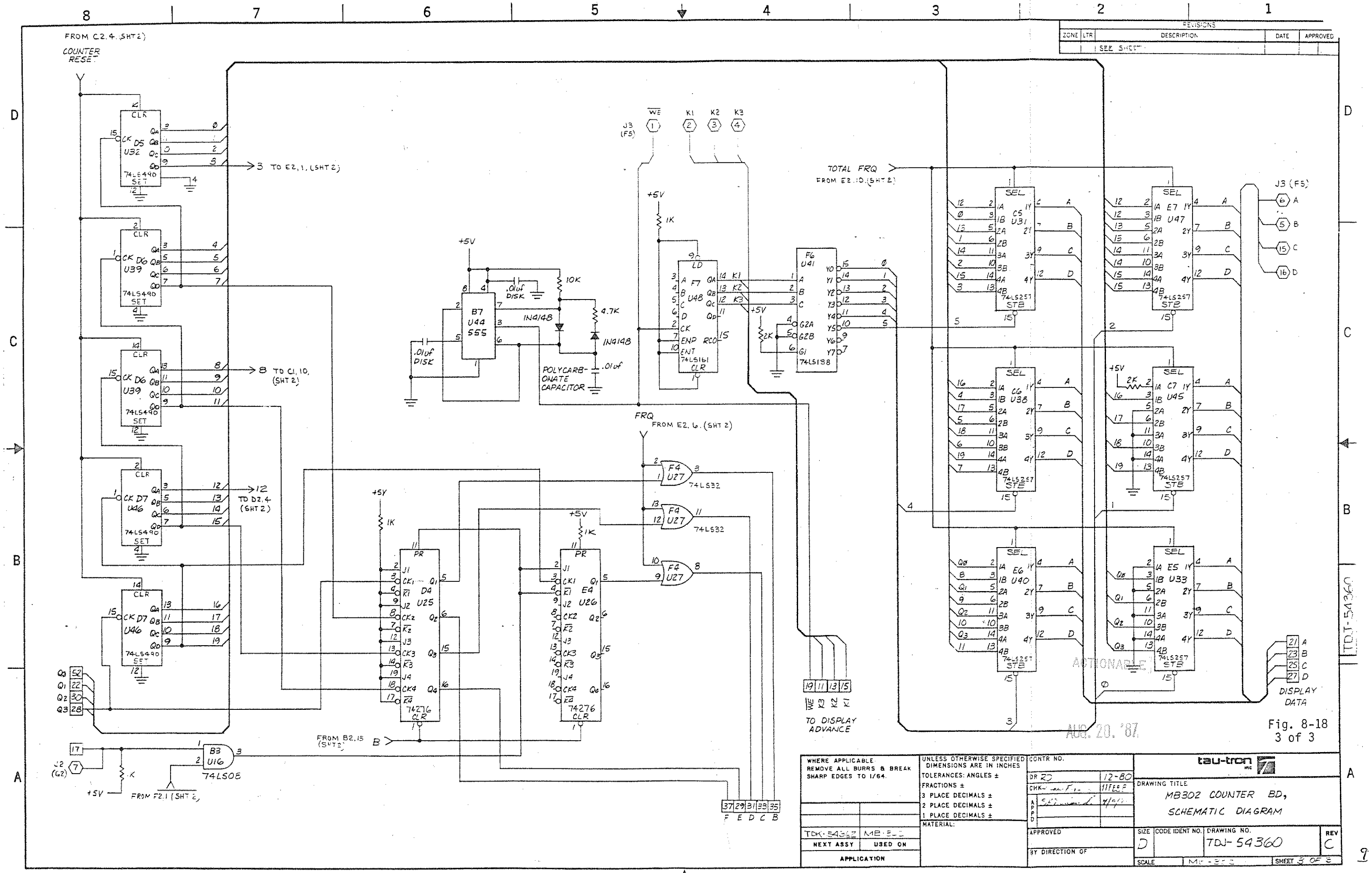


Fig. 8-18
3 of 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET		

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

NEXT ASSY	USED ON
TDK-54362	MB-302

APPLICATION

CONTR NO.
DR RD 12-80
CHK
APPD
APPROVED
BY DIRECTION OF

tau-tron inc

DRAWING TITLE
MB302 COUNTER BD, SCHEMATIC DIAGRAM

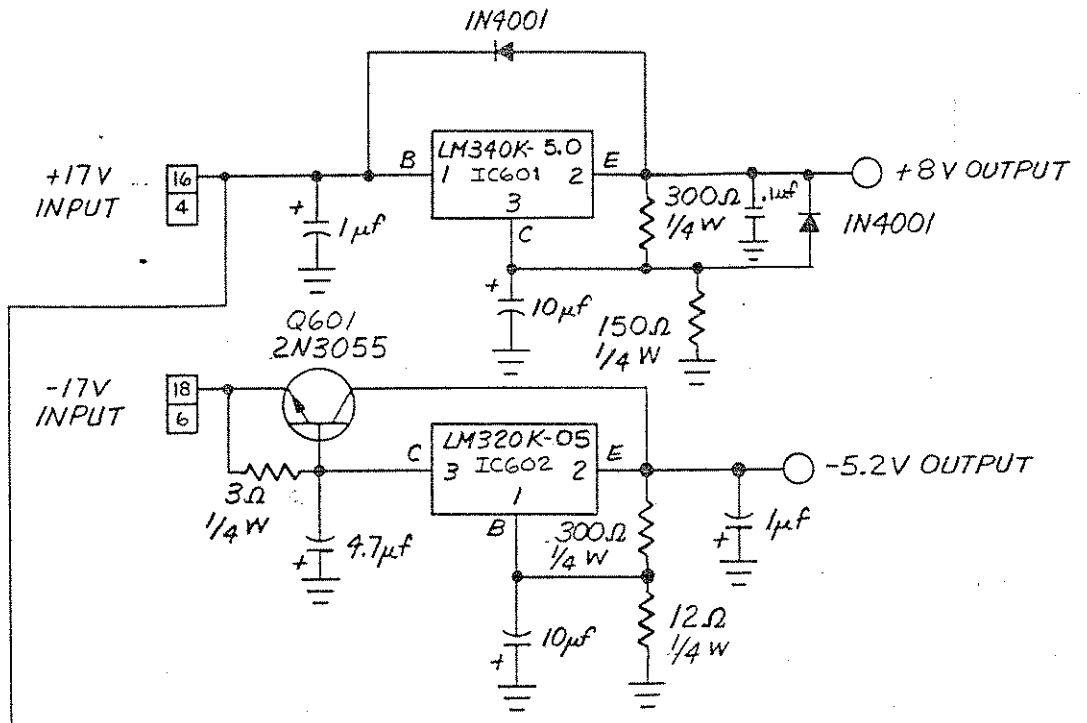
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		TDJ-54360	C

SCALE MB-302 SHEET 3 OF 3

TDJ-54360

9

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	DELETE +5 BOOST TRANSISTOR KRW		
	2	REV PER PDC 00785 CA.	11-13-80	BAC



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
   B. CAPACITANCE VALUES ARE IN MICROFARADS.
2. □ INDICATES 24 PIN POWER CONNECTOR

ACTIONABLE

TEK-54424	MB-302
NEXT ASSY	USED ON
APPLICATION	

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± —
2 PLACE DECIMALS ± —
1 PLACE DECIMALS ± —
MATERIAL:

CONTR NO.
DR JRW 5 Jun 80
CHK MJC 18 June 80
APPD
APPROVED
BY DIRECTION OF

tau-tron inc.

DRAWING TITLE
MB-302 POWER SUPPLY
SCHEMATIC +8V, +5V, -5V BOOST

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C		TCJ-54421	2

SCALE NONE | TM1 SERIES | SHEET 1 OF 1

Fig. 8-19
1 of 1

A	REV PER ECO# 00993 JRP 17 JUN 81	6-18-81	RJL DAT
B	REV PER ECO#01077 RN 2-23-82	3-4-82	RJL DAT
C	REDRAWN BMB. 5-12-82	5-12-82	RJL

CNTR A J2-3
CNTR B J2-1
SYNC A J2-17
SYNC B J2-15
BURST J2-14
SEQ A J2-11
SEQ B J2-9
SEQ C J2-5
UP EXP J2-7
RESET J2-19
CH5 CH6 CH9 CH10 CH11 CH13
CH14 CH15 CH17 CH18 CH19 CH20
CLR REM
DATA1 CH1 CH2 CH3
CLEAR ← U14-10 SHT-2
EXP DATA A, J5-9
EXP DATA B, J5-10
EXP DATA C, J5-11
EXP DATA D, J5-12
EXP 1 (U9-3)
EXP 2 (U9-6)
EXP 4 (U9-10)
EXP 8 (U9-12)

74LS157 U16
74LS157 U17
74LS157 U28
74LS174 U18
74LS174 U19
74LS04 U23
74LS00 U15
7485 U7
7485 U26
74LS123 U31
R38 3K
R32 3K
R33 3K
R3 3K
R7 3K
R12 3K
R14 3K
R15 3K
R16 3K
C4 10PF
R2 5.1K
C3 150PF
R1 5.1K
C2 33μF
.01μF C6-C21

→ J2-4 CNTR A
→ J2-2 CNTR B
→ J2-18 SYNC A
→ J2-16 SYNC B
→ J2-13 BURST
→ J2-12 SEQ A
→ J2-10 SEQ B
→ J2-6 SEQ C
→ J2-8 UP EXP
→ J2-20 RESET

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A) RESISTANCE VALUES ARE IN OHMS' 1/8W ±5%.
B) CAPACITANCE VALUES ARE IN MICROFARADS

AUG. 20, '82

Fig. 8-20
1 of 2

REFERENCE DESIGNATIONS			
LAST USED		UNUSED	
C24		R13	
R47			
U32			

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

D-54543 | MB-302
NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

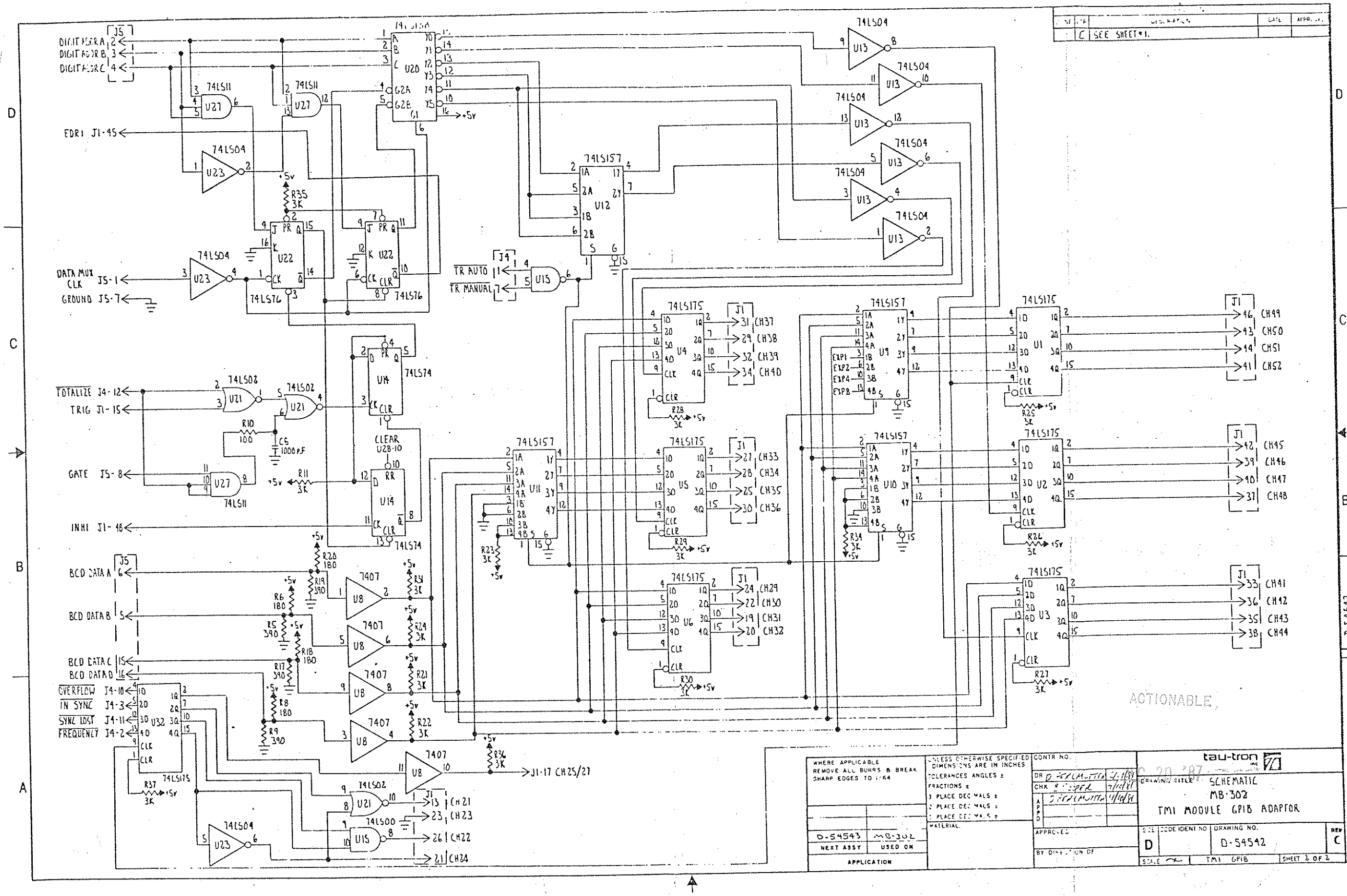
CONTR NO
ORIG. PERLMUTTER 2/19/81
CHK J. COOPER 4/10/81
APPD D. PERLMUTTER 11-4-81
APPROVED
BY DIRECTION OF

tau-tron

DRAWING TITLE SCHEMATIC
MB-302
TMI MODULE GPIB ADAPTOR

SIZE D | CODE IDENT NO | DRAWING NO D-54542 | REV C
SCALE 1 | TMI GPIB | SHEET 1 OF 1

D-54542



DIGIT ADDR A
DIGIT ADDR B
DIGIT ADDR C
EDR1 J1-45
DATA MUX CLK J5-1
GROUND J5-7
TOTALIZE J4-12
TRIG J1-15
GATE J5-8
INHI J1-48
BCD DATA A
BCD DATA B
BCD DATA C
BCD DATA D
OVERFLOW J4-10
IN SYNC J4-3
SYNC LOST J4-11
FREQUENCY J4-2
TR AUTO
TR MANUAL
CLEAR U28-10
J1-17 CH25/27
ACTIONABLE
SEE SHEET #1.
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL
D-54543
MB-302
NEXT ASSY
USED ON
APPLICATION
CONTR NO.
APPROVED
BY DIRECTION OF
tau-tron
DRAWING TITLE
SCHEMATIC
MB-302
TMI MODULE GPIB ADAPTOR
SIZE D
CODE IDENT NO
DRAWING NO. D-54542
REV C
SCALE
TMI GPIB
SHEET 2 OF 2

Fig. 8-20
2 of 2