INSTRUCTION MANUAL

MODEL 22
11 MHz STABILIZED SWEEP GENERATOR

WAVETEK®

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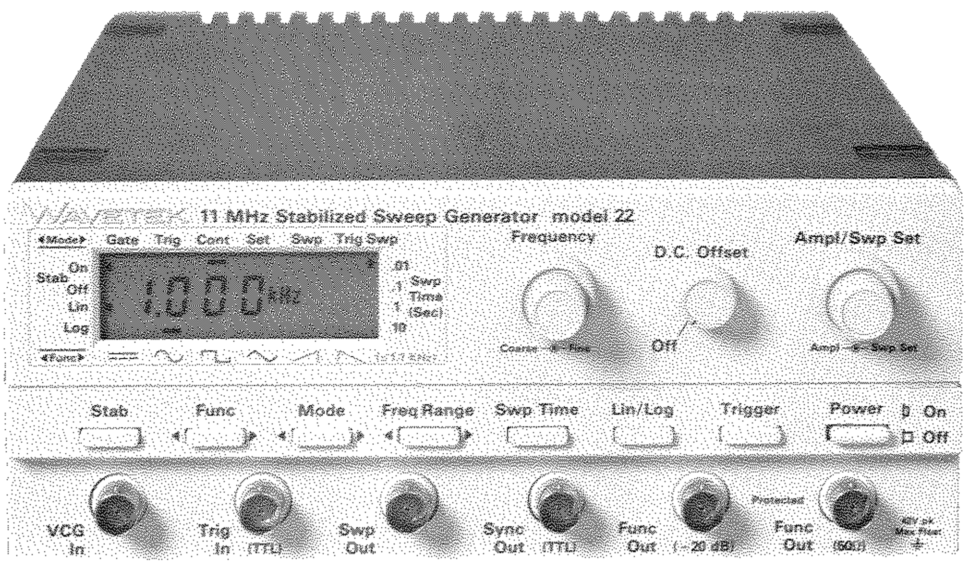
WARRANTY

Wavetek warrants that all products of its own manufacture conform to Wavetek specifications and are free from defects in material and workmanship when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek hereunder shall expire one (1) year after delivery and is limited to repairing, or at its option, replacing without charge, any such product which in Wavetek's sole opinion proves to be defective within the scope of this Warranty. In the event Wavetek is not able to repair or replace defective products or components within a reasonable time after receipt thereof, Buyer shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the warranty period and the affected product returned to Wavetek's factory or to an authorized service center within thirty (30) days after discovery of such defect or nonconformity. Shipment shall not be made without prior authorization by Wavetek.

This is Wavetek's sole warranty with respect to the products delivered hereunder. No statement, representation, agreement or understanding, oral or written, made by an agent, distributor, representative or employee of Wavetek, which is not contained in this warranty, will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Wavetek makes no other warranty of any kind whatsoever, expressed or implied, and all implied warranties of merchantability and fitness for a particular use which exceed the aforestated obligation are hereby disclaimed by Wavetek and excluded from this agreement. Under no circumstances shall Wavetek be liable to Buyer, in contract or in tort, for any special, indirect, incidental or consequential damages, expenses, losses or delays however caused.**



Model 22. 11 MHz Stabilized Function and Sweep Generator

SECTION 1
GENERAL DESCRIPTI

1.1 MODEL 22

Model 22 is a closed-loop, frequency stabilized, sweep/function generator. Both short term and long term frequency accuracy is 0.09% over its 100 μHz to 11 MHz frequency span.

Modes are continuous, triggered, gated, sweep set, continuous sweep and triggered sweep. Output levels are to 20V peak-to-peak (10 Vp-p into 50Ω).

Waveforms are sine, triangle, square, ramp up, ramp down, and dc. Above 1.1 kHz waveforms are analog generated; below, waveforms are digitally synthesized.

An LCD display shows frequency (3½ digits plus unit of measure) and annunciators that indicate selected operating modes, etc. The waveform output circuit is protected from accidental application of high voltage to the BNC connector.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

A bidirectional pushbutton switch selects sine (∿), triangle (∿), square (⊓) and dc (⎓), and for frequencies on or below the 1.100 kHz range, ramp up (⟋) and ramp down (⟍).

Operational Modes

Continuous: Generator runs continuously at selected frequency. Continuous frequency and sweep start frequency set with Frequency Course and Fine controls.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one complete waveform cycle at selected frequency.

Gated: As triggered mode, except output continues for duration of gate signal. Last waveform started is completed.

Set: Generator runs continuously at sweep stop frequency set by Sweep Set control. Sweep stop frequency is displayed.

Sweep: Generator frequency is swept from the start frequency limit set by the Frequency control to the stop frequency limit set by the Sweep Set control in a (tinuously occurring sweep. Sweep Time and linea logarithmic sweep are selectable.

Triggered Sweep: Generator is quiescent until trigge by a low to high external signal at Trig In BNC or manu by Trigger button. After a trigger, generator is gate for the duration of a single sweep at selected sweep t and start and stop frequencies. If external trigger si has returned to the low state (or manual Trigger is rel ed) before the end of the sweep time, generator retu to the quiescent state until the next trigger input. If ger is high at the end of the sweep (or manual Trig is held) the generator returns to the start frequency runs continuously until the next trigger input.

Frequency Range

100 μHz to 11 MHz in 9 overlapping decade ran Range switching with bidirectional switch with freque digits, decimal and units displayed on LCD display. E decade range capable of 1100:1 frequency change trolled by the Frequency Course and Fine control

Function Output

Waveform amplitude variable over a 20 dB range u 20 Vp-p (10 Vp-p into 50Ω) at Function Out. Wavef also present at Function Out (-20 dB) with a fixed 2 attenuation relative to the Function Out for a full 4 of amplitude range. Peak output current is 100 mA r imum at Function Out. Source impedance of both puts is 50Ω.

DC Offset and DC Output

Waveform offset and dc output variable with DC O control with off position for calibrated zero offset. F tion Out is ± 10V maximum (± 5V into 50Ω) as offs Vdc output. Signal peak plus offset limited to ± 10V (into 50Ω). DC offset plus waveform attenuated pro tionately at Function Out (-20 dB).

Sync Output

TTL pulse (50% duty cycle) at generator frequency drive 10 LS TTL loads.

VCG — Voltage Controlled Generator

Up to 1100:1 frequency change with external 0 to ± 5V signal applied to VCG IN connector. Upper and lower frequencies limited to maximum and minimum of selected range. Input impedance is 5kΩ and maximum slew rate is 0.1V/μs. VCG IN is disconnected when the Stabilizer is enabled.

Trigger and Gate

External TTL compatible signal at Trig In BNC triggers or gates generator output when generator is in trigger, gate or triggered sweep mode. Generator triggers on positive edge of input or gates on for duration of high level input. External signal pulse width is 50 ns minimum with a maximum repetition rate of 5 MHz.

Stabilizer

When selected, the generator frequency is stabilized at the displayed frequency to a crystal-controlled reference.

When the stabilizer is on, long term frequency stability is corrected to the displayed frequency over the entire operating temperature range of 0 to +50°C. The stabilizer is automatically turned off when the mode is taken out of continuous or when Log frequency is enabled.

Display

1100 count LCD frequency display with frequency ranging units (mHz, Hz, kHz, and MHz) and a floating decimal point. Annunciators indicate selection of waveform, stabilizer status, generator mode, sweep time and linear or logarithmic sweep.

Sweep Generator

Sweep Mode: Linear or logarithmic, up to 3 decades.

Sweep Time: Selectable (in seconds) .01, .1, 1 and 10.

Sweep Output: Output voltage at sweep out connector proportional to the sum of Frequency control, internal sweep voltage and external VCG In voltage. Scale factor is 0 to +5V (open circuit) linear voltage change from bottom to top frequency of a range. Source impedance is 600Ω for driving horizontal axis of oscilloscope or recording equipment.

Sweep Width: Up to 1100:1 linear or logarithmic.

1.2.2 Frequency Precision

Frequency Display Accuracy

±1 count of 1100 counts, which is 0.09% of range. Stabilizer maintains same reading indefinitely.

Time Symmetry

Square waveform variation from 1100 to 100 counts on display less than:

±0.1% to 1.100 kHz (across bottom five specified ranges),
±1% to 110.0 kHz,
±5% to 11.00 MHz.

1.2.3 Amplitude Precision

Sine Variation with Frequency

Less than:
±0.2 dB on all ranges up through the 110.0 kHz range,
±1.5 dB to 11.00 MHz.
Referenced to 1 kHz.

1.2.4 Waveform Characteristics

Sine Distortion

<0.5% THD up through the 11.00 kHz range.
<1.0% THD on 110.0 kHz range.

All harmonics 40 dB below fundamental on 1.100 MHz range, and 28 dB below fundamental on 11.00 MHz range.

Square Wave

Rise/Fall Time: <22 ns

Total Aberrations: Each peak <5% of p-p amplitude.

Triangle Linearity

>99% to 110.0 kHz.

1.2.5 General

Output Protection

Function outputs are protected against a short circuit to any voltage between ±10V dc and also have internal fused protection (both output and common conductors) against accidental application of up to 250 Vac or 350V dc.

Stability

Amplitude, Frequency (Non-Stabilized) and DC Offset:

After 30 minute warm-up:
±0.10% of range for 10 minutes,
±0.50% of range for 24 hours.

Frequency (Stabilized): ±0.10% of range for ⩾10 minutes, 0 to 50°C.

5 cm

5 VA.

Environmental

Temperature Range: 25°C ± 10°C for spec operation, operates 0°C to 50°C, −20°C to +75°C for storage.

Warm-up Time: 20 minutes for specified operation.

Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.

Relative Humidity: 95% at 25°C and at sea level (noncondensing).

Dimensions
21.1 cm (8.3 in.) wide, 8.6 cm (3.4 in.) high, 30.
(12 in.) deep.

Weight
3.4 kg (7 1/2 lb) net, 4.5 kg (10 lb) shipping.

Power
90 to 128, 180 to 256V, 48 to 66 Hz, less than 3

NOTE

All specifications apply for display between 1100 and 100 frequency counts; amplitude at 10 Vp-p into 50Ω.

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage. If damage is discovered, file a claim with the carrier who transported the instrument. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

> To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

> To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 3/8 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit.

2.2.2 Verifying the Line Voltage

CAUTION

> All calibration pots are located inside the bottom cover on the circuit board. Be careful not to bump any pots, as this may require a recalibration of the instrument. Moving R103, located near the front panel, can keep the generator from operating; if adjustment is needed, refer to table 5-1 steps 1 through 10.

To verify the line voltage (or change the fuse) operator must first remove the top and bottom co Remove the top and bottom using the following step figure 2-1.

1. Remove two (2) screws holding top and bc covers to rear panel.
2. Slide both covers (together as a unit) to the rea remove from the chassis assembly.

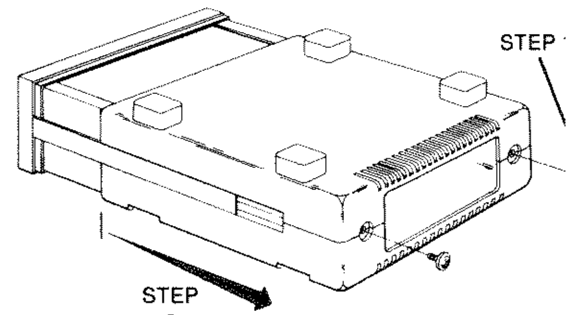


Figure 2-1. Top and Bottom Cover Remov

After the covers have been removed, the line voltag be checked by viewing the voltage label through t spection hole as shown in figure 2-2.

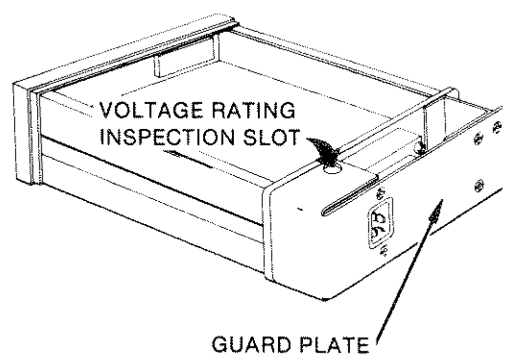


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct, perform the following steps and refer to figure 2-3 for steps 1 and 2, and figure 2-4 for steps 3 thru 5 to change the line voltage and fuse.

1. Remove the five screws attaching the guard plate.
2. Hold the ac power receptacle assembly against the rear panel while removing the guard plate.

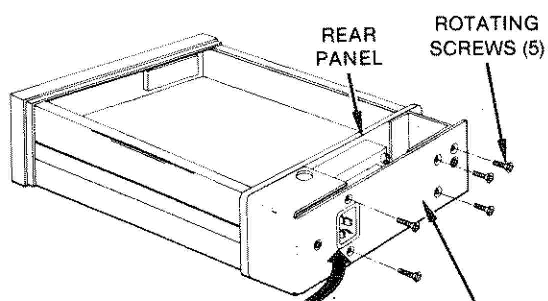


Figure 2-3. Guard Plate Removal

3. Hold the ac power receptacle firmly against the rear panel and remove the voltage selector connector from the ac primary board. Rotate the connector until the correct voltage selector indicator is on top.

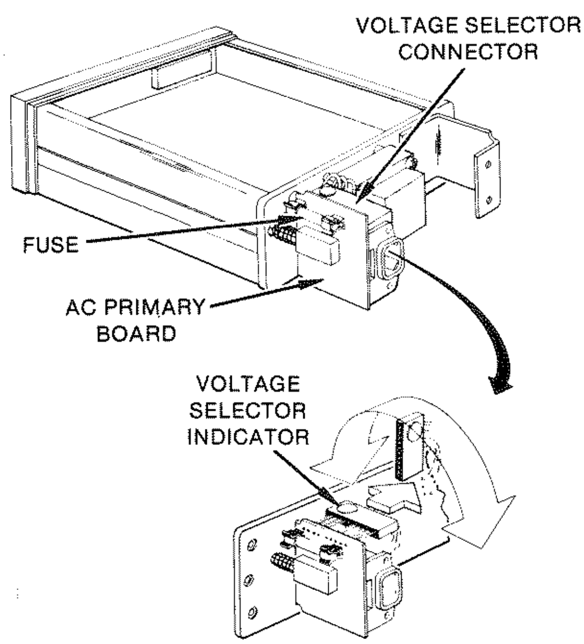


Figure 2-4. Fuse and Voltage Selection

4. Reinstall the voltage selector connector.
5. Remove the fuse and install new fuse as called out in table 2-1.

Table 2-1. Voltage/Fuse Selection

Connector Position	Voltage Range	Fuse
115V	90 to 128 Vac	3/8 amp
220V	180 to 256 Vac	3/16 amp

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the guard plate is attached to the unit.

2.2.4 Reassembly

Refer to figure 2-5 for steps 1 thru 5 and figure 2-6 for steps 6 thru 8.

1. Ensure the power rod goes through the slot in the front panel and the ac primary board seats into the slot in the rear panel.
2. Align the guard plate to the ac power receptacle and check the routing of all wires to prevent pinching wires between the transformer and guard plate.
3. Verify that the power rod extends through the front panel slot, the circuit board seats correctly in the rear panel slot.
4. Verify the guard plate, ac power receptacle and rear panel standoffs are properly aligned and then secure with two screws.
5. Fasten the guard plate to the unit with the three remaining screws.

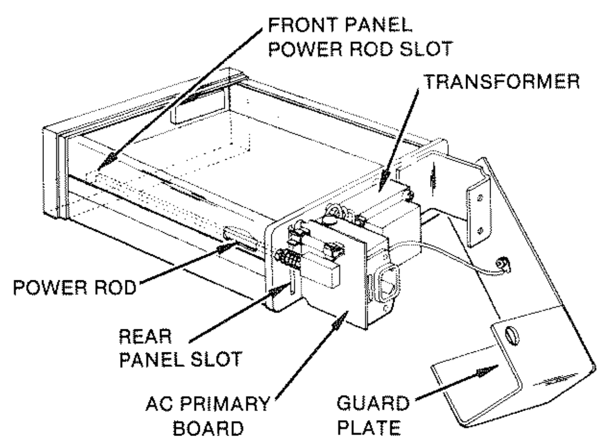


Figure 2-5. Rear Chassis Assembly

CAUTION

When sliding on the bottom cover, avoid pinching any coaxial cables located near the front panel.

6. Turn the instrument upside down, position the bottom cover over the guard shield, and then slide the bottom cover forward approximately two inches while engaging the top cover and slides (see figure 2-6, detail A and detail B). Don't slide the cover on yet.
7. Turn the instrument right side up. Install the top cover using the same procedure as in step 6. Don't slide the cover on yet.
8. Align the rear of both the top and bottom cover with each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly toge and slide the chassis assembly into the matec and bottom covers.
9. Secure covers to unit using two screws as sh in figure 2-1.

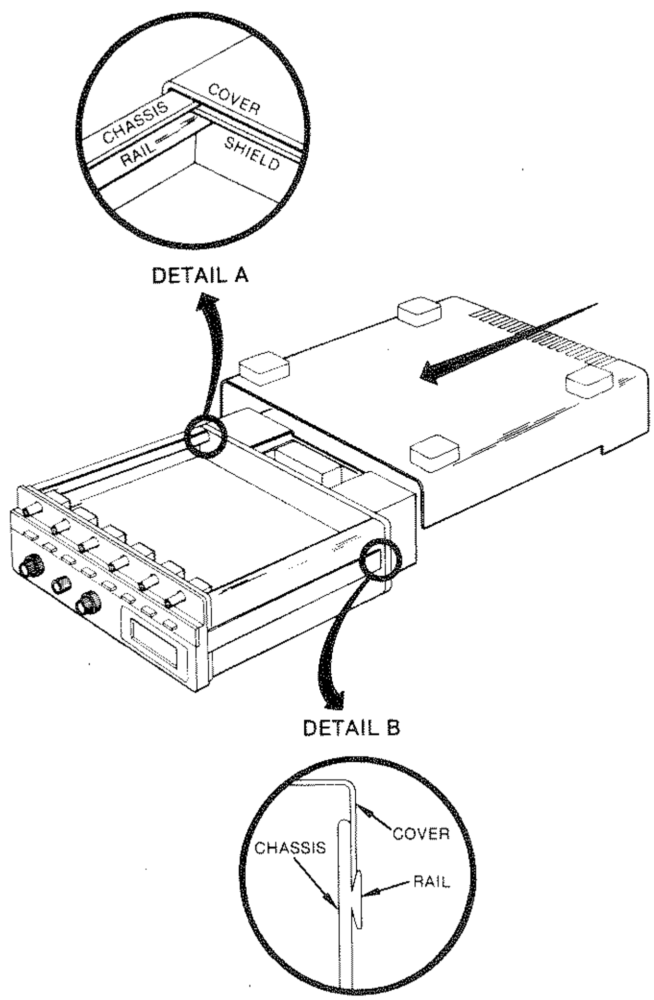


Figure 2-6. Top and Bottom Cover Installation

2.2.5 Signal Connections

Use RG58U 50Ω or equivalent 50Ω coaxial ca equipped with BNC connectors to distribute signa

NOTE

Signal ground may be floated up to ±42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.3 INITIAL CHECKOUT PROCEDURE

The initial checkout procedure in table 2-2 allows operator to learn the basic operation and capabiliti the Model 22 in an easy and orderly fashion. In addi it can be used as a receiving inspection or post-re checkout. While this procedure verifies functional op tion of this instrument, it does not verify the calibra **The frequencies shown are typical values and sh only be used as a guide.** Required tools and test e ment are listed below.

Instrument	Comments
Oscilloscope	Dual channel, 100 MHz bandwidth
Voltage Source	+5Vdc
50Ω Feedthrough	0.5% accuracy, 2W
External Generator	200 Hz to 1.1 MHz TTL output
BNC Tee	1 male, 2 female connec
BNC Coax Cable	RG58U, 3 ft. length (3 ea

2.3.1 Using the Procedure

The checkout procedure (table 2-2) can be used se different ways. It can be started at step 1 and foll straight through to the final step. Or, it can be en at the highlighted steps, which start specific grou checks. If the table is being followed in sequence the previous step, perform the instructions as wr But if starting at a highlighted step, the Model 22 first be reset to the power on settings (see belov do this, turn the Power Off, then On.

Power-On status:

Frequency Range: 0.001 to 1.100 kHz
Mode: Continuous
Function: Sine
Lin/Log: Lin
Sweep Time: 0.01s.
Stabilizer: Off

2.3.2 Front Panel Switches

The Func, Mode, and Freq Range switches are bidirectional. To use these switches, the operator must press the left or right side of the switch's front surface, as indicated by the arrows on the panel. Pressing the center of any bidirectional switch does not ensure correct operation. All other switches can be pressed anywhere.

When a switch is pressed, either the frequency or an annunciator on the display will change, as shown in table 2-2.

Table 2-2. Initial Checkout Procedure

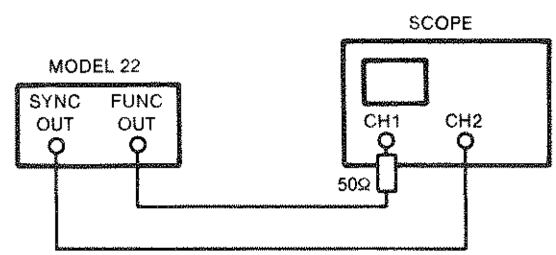
NOTE

1. *Before beginning this procedure, review paragraph 2.3.*
2. *Frequencies shown are typical and should only be used as a guide.*
3. *If starting at a highlighted step, first press Power Off, then On.*

Initial Settings

Control	Setting
Frequency	
Coarse	cw
Fine	cw
D.C. Offset	Off
Amplitude	cw
Swp Set	cw

Test Setup 1



Scope	Setting
Time base	0.2 ms/div
CH1 Vert	2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

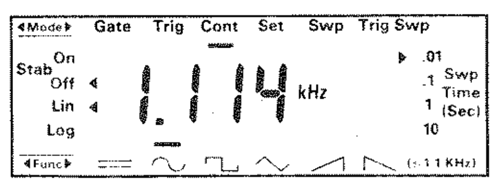
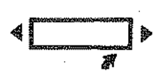
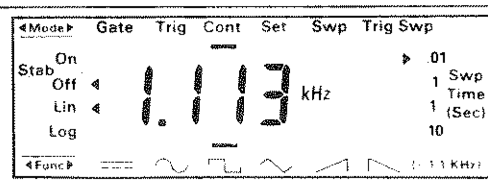
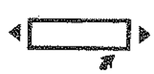
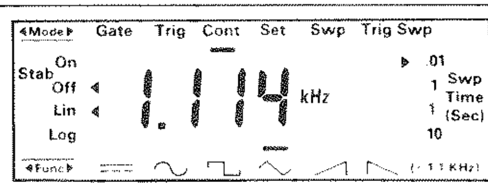
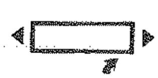
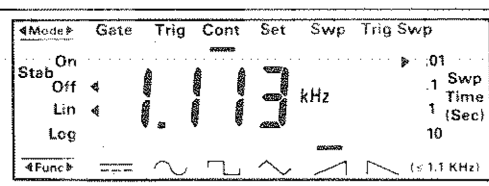
Step	Control	Operation	Display	Observation/Comments
Function Check				
1	Set to Initial Settings Power On			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
2(a)	Func	 Press Once		10Vp-p square wave.
2(b)		 Press Once		10Vp-p triangle.
2(c)		 Press Once		10Vp-p ramp up.

Table 2-2. Initial Checkout Procedure (Continued)

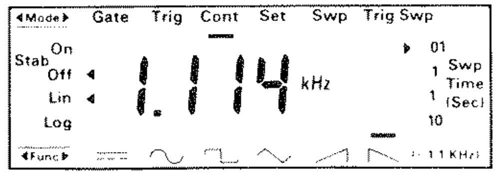
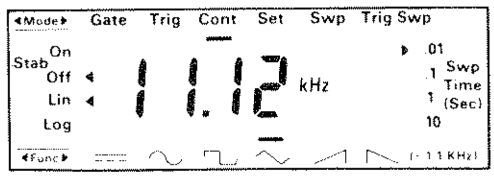
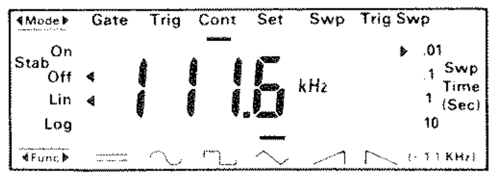
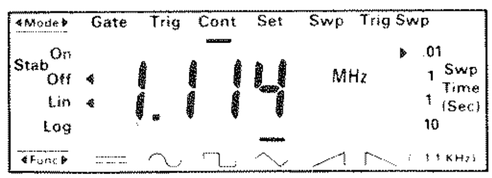
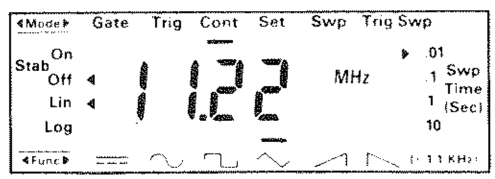
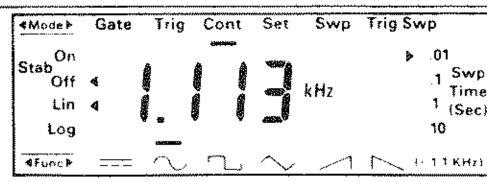
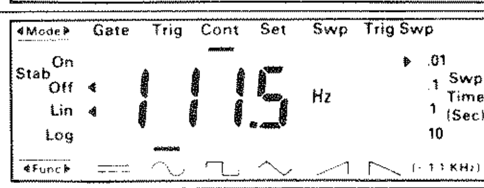
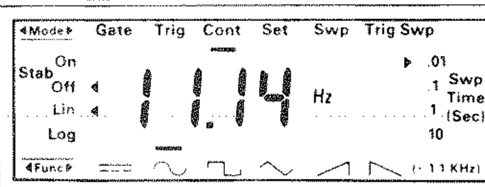
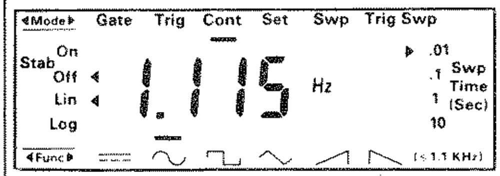
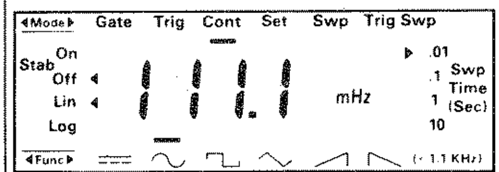
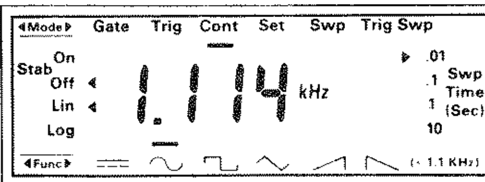
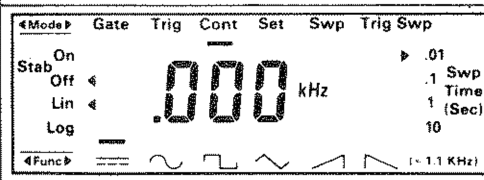
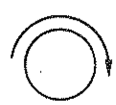
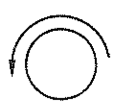
Step	Control	Operation	Display	Observation/Comme
2(d)	Func	Press Once		10Vp-p ramp down
Frequency Range Check (11k to 11 MHz)				
3(a)	Freq Range	Press Once		11 kHz, 10Vp-p trian Ramp defaults to triangle above the 1.1 kHz range.
3(b)		Press Once		110 kHz
3(c)		Press Once		1.1 MHz
3(d)		Press Once		11 MHz
Frequency Range Check (110 Hz to 110 mHz)				
4	Set to Initial Setting			Connect as shown i test setup 1. 1.1 kHz, 10Vp-p sin wave.
	Power	Press to Off then to On.		
5(a)	Freq Range	Press Once		110 Hz
5(b)		Press Once		11 Hz

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
5(c)	Freq Range	Press Once		1.1 Hz
5(d)		Press Once		110 mHz

DC Offset Check

Step	Control	Operation	Display	Observation/Comments
6	Set to Initial Setting			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off then to On.		
7	Func	Press Once		0 Vdc
8(a)	D.C. Offset	 Full cw		Greater than +5 Vdc
8(b)		 Full ccw, but not off		Greater than −5 Vdc
8(c)		 Off		0 Vdc

Coarse and Fine Frequency Check

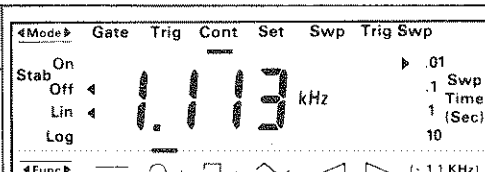
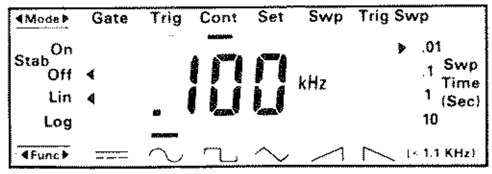
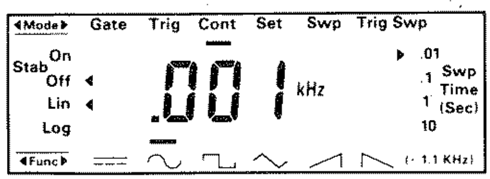
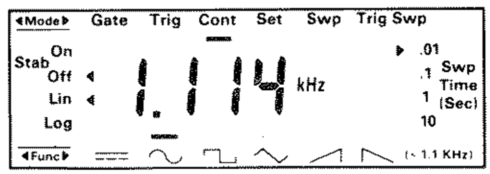
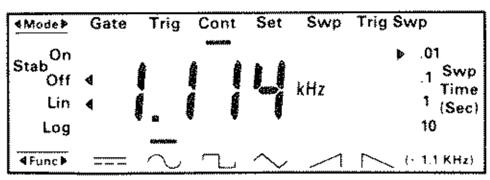
Step	Control	Operation	Display	Observation/Comments
9	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Func	Press Once		

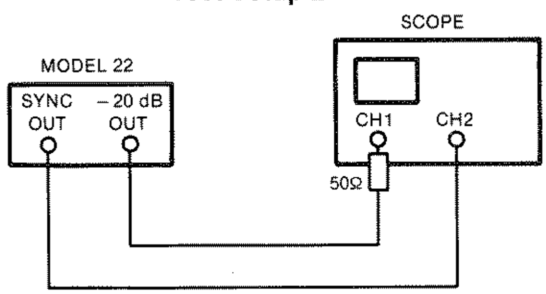
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comme
10	Frequency Coarse	 Full ccw		Approximately 11:1 fr quency change. Verif all display segements function.
11	Frequency Fine	 Full ccw		Approximately 100:1 frequency change.
12	Frequency Coarse and	 Both full cw		Total frequency char of 1100:1.

Amplitude Check

Step	Control	Operation	Display	Observation/Comme
13 (a)	Set to Initial Setting			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave; output level decreases to 1 Vp-p control is rotated.
	Amplitude	 Full ccw		

Test Setup 2

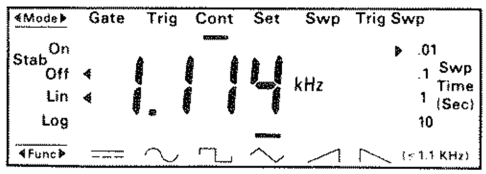
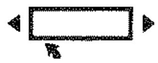
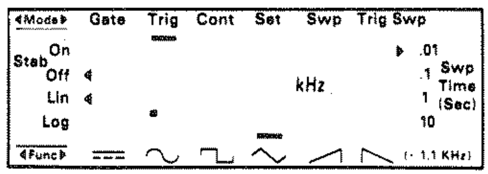


Step	Control	Operation	Display	Observation/Comme
13(b)		 Rotate cw		Connect as shown ir test setup 2. Output increases from 0.1 t 1 Vp-p.

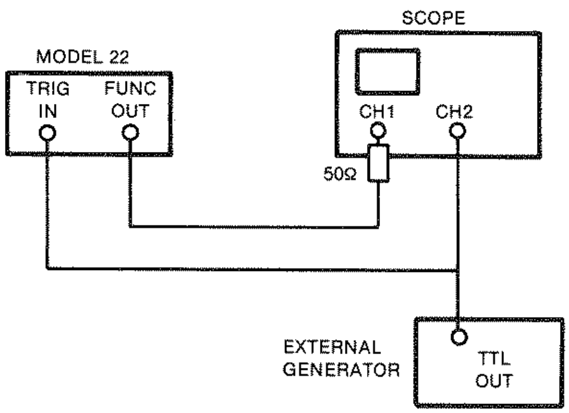
Sync Out Check

Step	Control	Operation	Display	Observation/Comme
14				Display CH2; 1.1 kH TTL square wave.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
Trigger and Gated Check				
15	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p triangle.
	Func	 Press Twice		
16(a)	Mode	 Press Once		Approximately 0 Vdc level.

Test Setup 3



Scope	Settings
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH2
Display	CH1 and CH2

External Generator Setting
200 Hz TTL

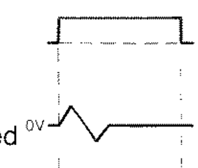
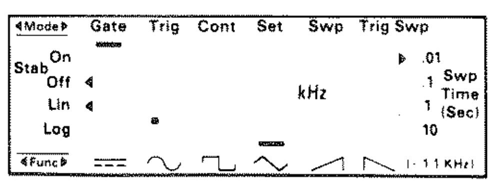
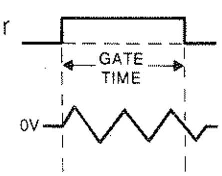
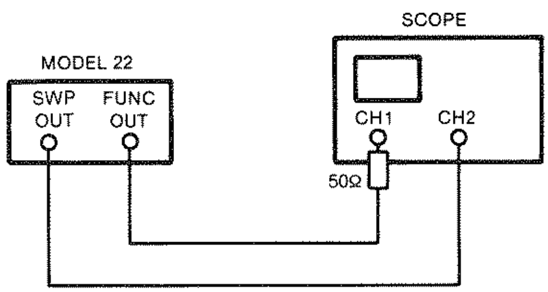
Step	Control	Operation	Display	Observation/Comments
16(b)		Connect as shown in test setup 3		CH2: Trigger Input CH1: Triggered Triangle 
16(c)		 Press Once		CH1: Trigger Input CH2: Gated Triangle 
16(d)	Trig In	Disconnect External Generator		Display CH1. 0 Vdc.

Table 2-2. **Initial Checkout Procedure (Continued)**

Step	Control	Operation	Display	Observation/Comme
Manual Trigger Check				
17	Trigger	 Press and Hold		Continuous triangle while trigger button i pressed.

Sweep Check

Test Setup 4



Scope	Settings
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH1
Display	CH1 and CH2

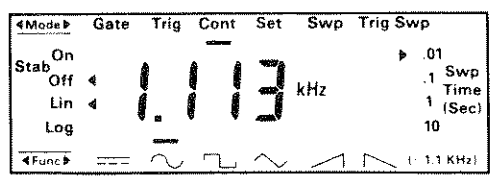
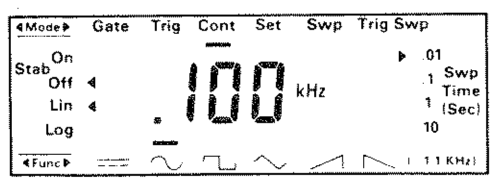
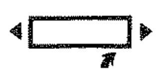
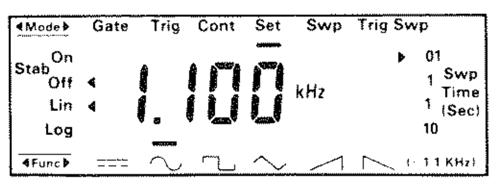
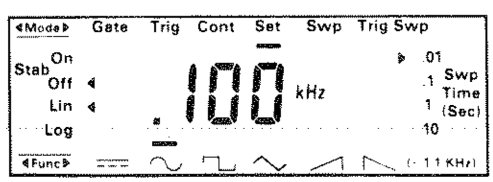
Step	Control	Operation	Display	Observation/Comme
18	Set to Initial Settings			Connect as shown test setup 4 CH1: 1.1 kHz 10 V sine wave. CH2: +5 Vdc level.
	Power	Press to Off then to On		
19	Frequency Coarse	 Full ccw		CH1: 100 Hz sine w CH2: Voltage level decreases.
20	Mode	 Press Once		CH1: 1.1 kHz sine wave. CH2: +5 Vdc level.
21(a)	Swp Set	 Full ccw		CH1: 100 Hz sine w CH2: Voltage level decreases.

Table 2-2. Initial Checkout Procedure (Continued)

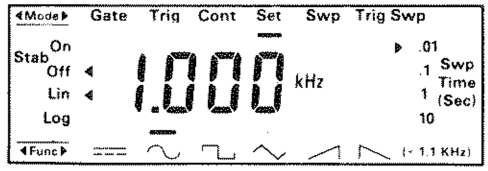
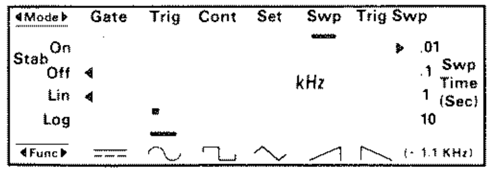
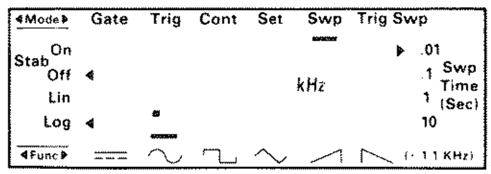
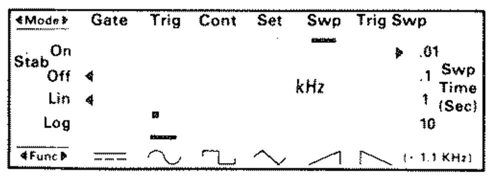
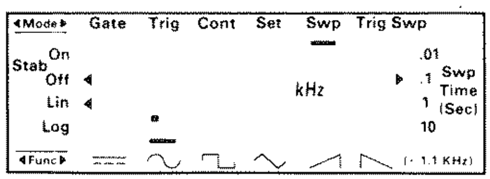
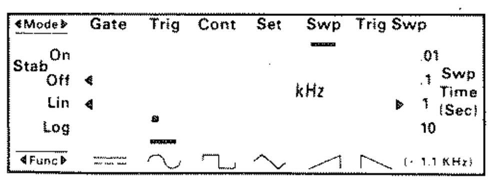
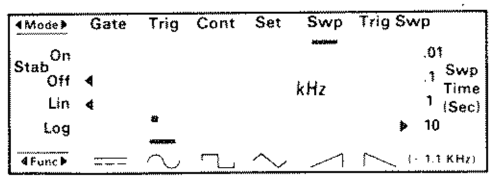
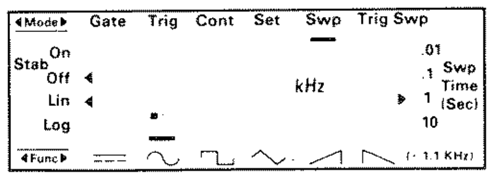
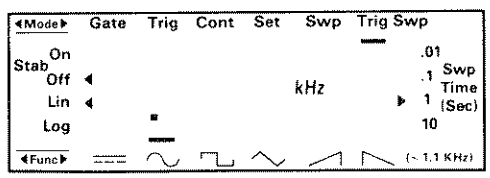
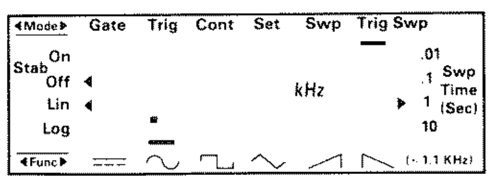
Step	Control	Operation	Display	Observation/Comments
21(b)	Swp Set	See comments		Display: Set to 1.00 kHz. CH1: 1.00 kHz sine wave. CH2: Voltage level decreases.
22	Mode	Press Once		Trigger scope on falling edge of sweep range (CH2). CH1: Linear sine wave sweep from 100 Hz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).
23(a)	Lin/Log	Press Once		Logarithmic sine wave sweep from 100 Hz to 1.00 kHz.
23(b)		Press Once		Linear sine wave sweep from 100 Hz to 1.00 kHz.
24(a)	Swp Time	Press Once		Scope: Trigger sweep to normal; time base to 10 ms/div. CH1: Linear sine wave sweep from 100 kHz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).
24(b)		Press Once		Scope: Time base to 0.1 s/div. CH1: Linear sine wave sweep from 100 Hz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comm
24(c)		Press Once		Scope: Time base t 1 ms/div. CH1: Linear sine wa sweep from 100 Hz 1.00 kHz. CH2: Slow rising ra
24(d)		Press three times		Scope: Time base t 1s/div. Sweep time annuni- cator steps to 0.01 0.1 s to 1 s each tir the switch is presse
25	Mode	Press Once		CH1: 0 Vdc level.
26(a)	Trigger	Press and release		CH1: Triggered sine wave sweep from 100 Hz to 1.00 kHz 1s and return to qu cent 0V level.
26(b)		Press and Hold		Triggered sine wav sweep from 100 Hz 1.00 kHz in 1s and returns to 100 Hz.

Stabilizer Check

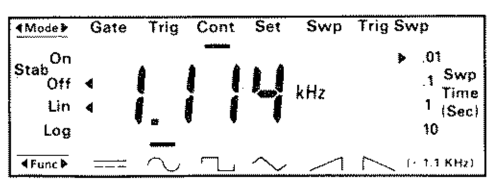
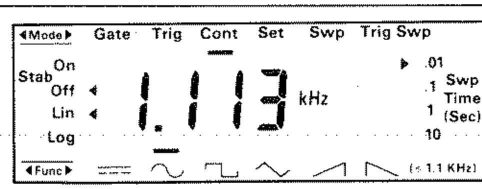
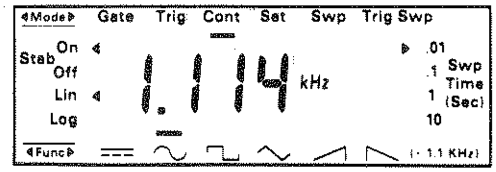
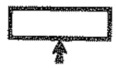
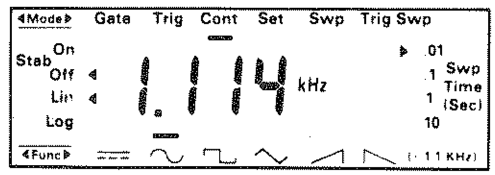
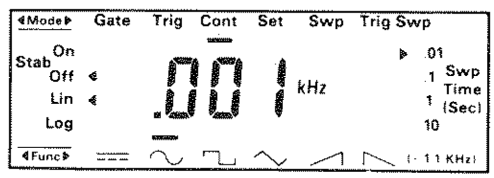
Step	Control	Operation	Display	Observation/Comm
27	Set to Initial settings			Connect generator shown in test setup 1.1 kHz 10 Vp-p sir wave.
	Power	Press to Off then to On		
28	Frequency Fine	See Comments		Rotate knob until th least significant dig fluctuates between digits.

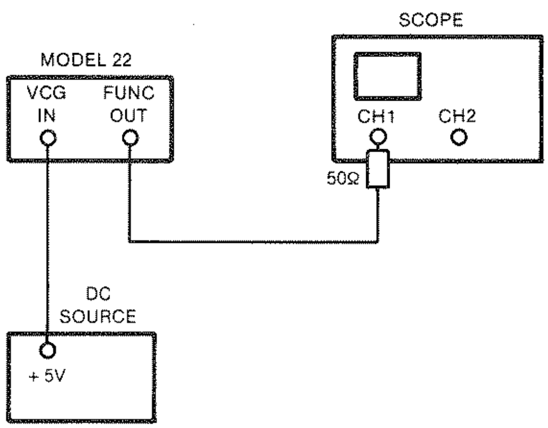
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
29	Stab	 Press Once		The least significant digit remains stabilized.

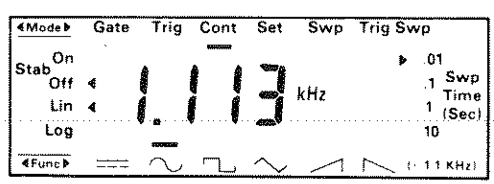
VCG Check

Step	Control	Operation	Display	Observation/Comments
30	Set to Initial Settings Stab	 Press Once		1.1 kHz 10 Vp-p sine wave.
31	Frequency Coarse and Fine	 Both full ccw		Low frequency sine wave.

Test Setup 5



Scope	Settings
Time base	0.2 ms/div
CH1 Vert	2 V/div
Display	CH1

Step	Control	Operation	Display	Observation/Comments
32	VCG In	+5 Vdc		Connect as shown in test setup 5. 1.1 kHz 10 Vp-p sine wave.

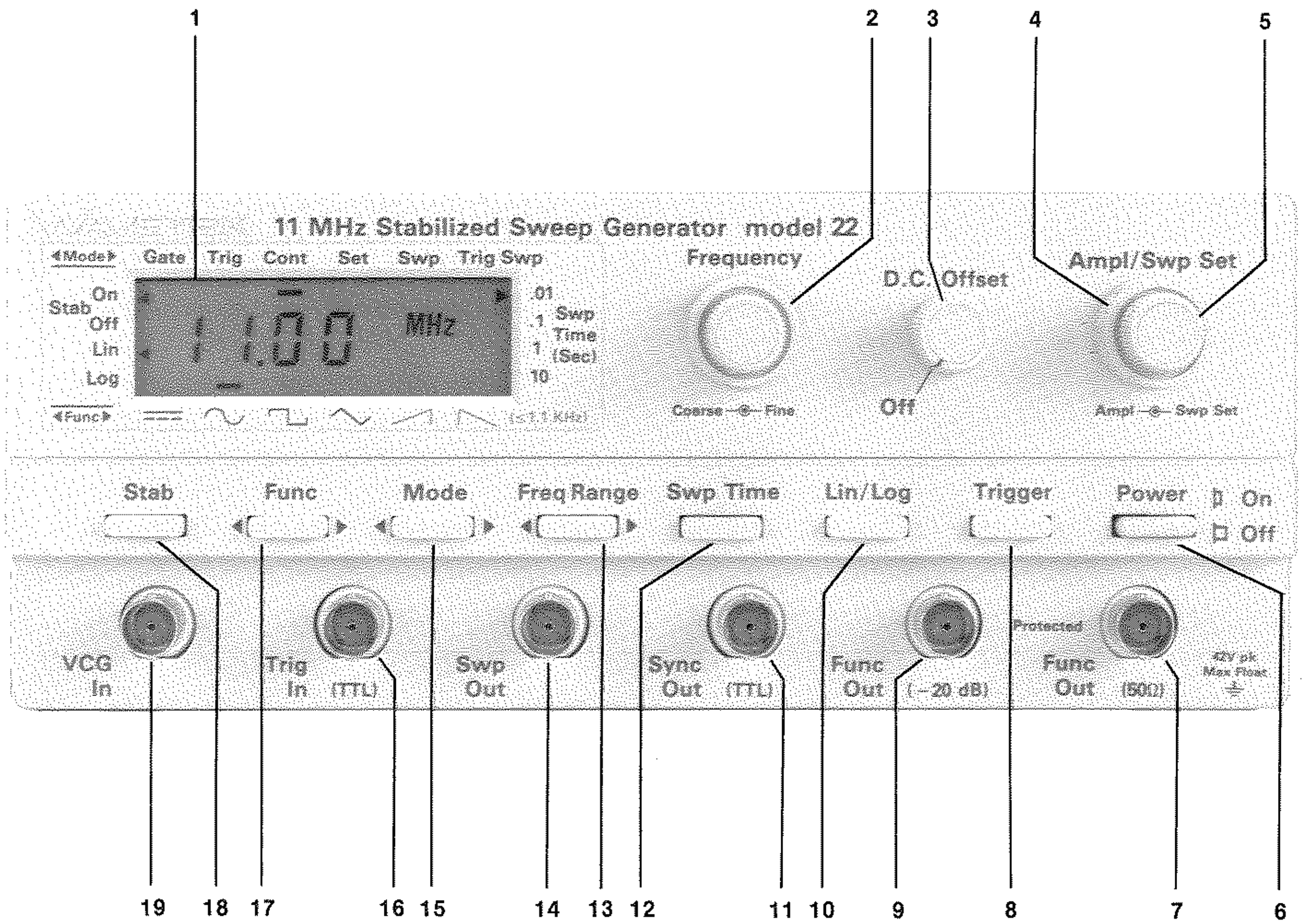


Figure 3-1. Controls and Connectors

3.1 INTRODUCTION

This section describes the operation of the Model 22. The first part describes the controls and connectors of the instrument. The following part illustrates several applications which use the various functions and modes of this instrument.

3.2 CONTROLS AND CONNECTORS

Figure 3-1 shows the front panel controls and connectors that are keyed to the following paragraphs.

1 **Display** A 3½ digit (1100 count) LCD frequency display which incorporates annunciators that indicate Mode, Function (waveform), stabilizer on/off, lin/log sweep, and sweep time.

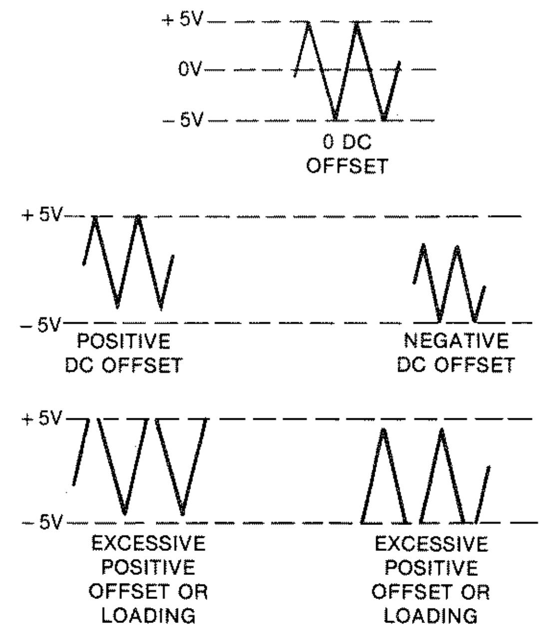
2 **Frequency Controls** The coarse frequency control, the outer knob of the concentric pair, allows coarse frequency adjustment (approximately 1000 counts) within the selected frequency range.

The fine frequency control, the inner knob of the concentric pair, allows fine frequency adjustment (approximately 100 counts) within the selected frequency range.

For linear mode, these controls vary the frequency linearly over the frequency range. For logarithmic mode, these controls vary the frequency logarithmically over the frequency range. Together the fine and coarse controls cover a 1100:1 frequency span within a selected range.

3 **D.C. Offset Control** The DC offset knob controls the dc voltage and offset of waveforms. A clockwise rotation vertically offsets the waveform up from the normal position (figure 3-2). A counterclockwise rotation vertically offsets the waveform down from the normal position (figure 3-2). A full counterclockwise rotation to Off ensures zero offset.

4 **Amplitude Control** The amplitude knob, the outer knob of the concentric pair, controls waveform amplitudes. Rotate the control full clockwise for maximum amplitude (see table 3-1). A counterclockwise rotation decreases the amplitude by 20 dB.



Function Out (50Ω) terminated with 50Ω

Figure 3-2. DC Offset Control

Table 3-1. Maximum Voltage

Function	Open Circuit	50Ω Terminat
	20 Vp-p	10 Vp-
DC	±10V	±5V

5 **Sweep Set Control** The Swp Set control, the knob of the concentric pair, sets the stop freq in the sweep modes (see figure 3-3).

6 **Power Switch** The power switch turns the in ment On or Off. At power-up the instru initializes in the following conditions:

Stab: Off
Func: Sine
Mode: Cont
Freq Range: 0.001 to 1.100 kHz
Lin/Log: Lin
Swp Time: 0.01s

7 **Function Output Connector** This BNC connector is the main output for the selected function. The Amplitude knob **4** controls the amplitude from 1 to 10 Vp-p into a 50Ω load (20 Vp-p into open circuit). Source impedance is 50Ω.

8 **Trigger Switch** In triggered mode, the trigger button, when pressed, manually initiates a single cycle of the selected waveform. In the gated mode, it gates the output until the button is released; the last gated cycle will always be completed. The quiescent output depends on the waveform selection and dc offset (see figure 3-4). In triggered sweep mode, the trigger button, when pressed, initiates a triggered sweep (refer to Triggered Sweep Mode).

9 **Function Output (−20dB)** This BNC connector is the same as the Func Out **7** except the output is 1/10th (−20 dB) of the amplitude, 0.1 to 1Vp-p. Both the waveform and offset are attenuated at Func Out (−20 dB). Source impedance is 50Ω.

10 **Lin/Log Switch** When pressed, the Lin/Log switch selects either linear or logarithmic mode for up to 1100:1 linear or logarithmic frequency range. An annunciator arrow on the display indicates the status.

11 **Sync Output** This output is a TTL square wave at the frequency of the generator. This output can be used as a synchronizing reference for the Function Outputs **7** and **9**. Phase of the waveforms relative to the sync output is shown in figure 3-4.

12 **Sweep Time Switch** The Sweep time button, when pushed, steps through the sweep time (.01, .1, 1, and 10 seconds). Sweep time is indicated by an annunciator arrow on the display. Frequency of the internal sweep ramp, the sweep rate, is governed by the Sweep time switch **12** (see figure 3-3).

13 **Frequency Range Switch** Frequency Range switch, when pushed on the left or right, steps through the nine frequency ranges, a shown below.

Specified Range	**Lowest Obtainable Frequency**
11.00 to 1.00 MHz	0.01 MHz
1.100 to 0.100 MHz	0.001 MHz
110.0 to 10.0 kHz	0.1 kHz
11.00 to 1.00 kHz	0.01 kHz
1.100 to 0.100 kHz	0.001 kHz
110.0 to 10.0 Hz	0.1 Hz
11.00 to 1.00 Hz	0.01 Hz
1.100 to 0.100 Hz	0.001 Hz
110.0 to 10.00 mHz	0.1 mHz

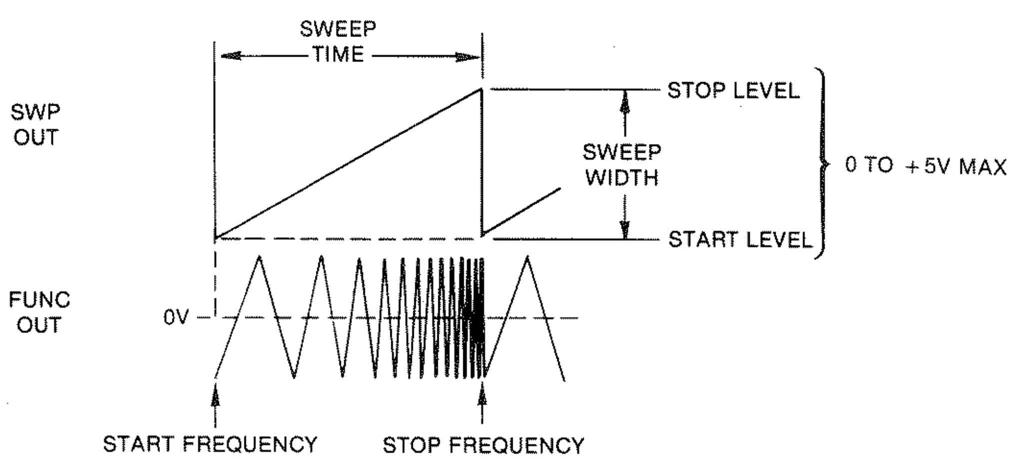


Figure 3-3. Sweep Time and Width

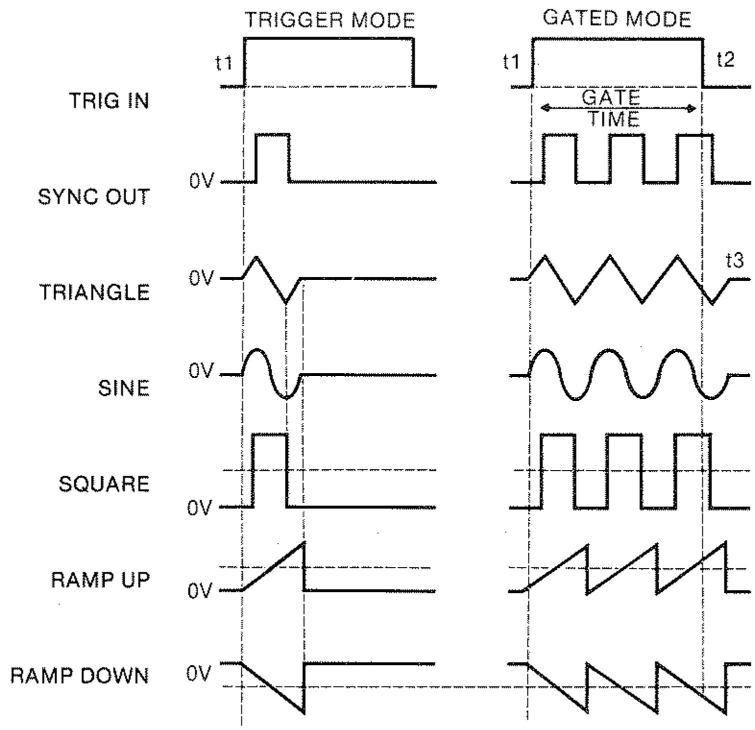


Figure 3-4. Waveform Phase Relationships

the LCD display **1**. Each range has an 1100:1 breadth. Power-up range is 0.100 to 1.100 kHz.

14 Sweep Out Connector The Swp Out BNC provides a linear ramp at the frequency selected by the Swp Time **12** switch. The ramp will be linear in both linear and logarithmic modes. The output voltage is proportional to the linear output frequency which is a summation of Frequency knobs **2** position, internal sweep voltage and external voltage at VCG In **18** connector. Output source impedance is 600Ω.

15 Mode Switch The Mode switch, when pushed on the left or right, steps through the six operating modes of the instrument.

Continuous (CONT) Generator runs continuously at the selected frequency. This is also the sweep start frequency.

Triggered (TRIG) Generator is quiescent (quiescent level depends on waveform and offset selected, figure 3-4) until triggered, at which time on plete cycle of waveform is generated.

Gated (GATE) As for triggered except the wa is continuous for the duration of the gate When the signal stops, the last waveform started is completed.

Sweep Set (SET) The generator runs contin at the sweep stop frequency set by Swp Set The sweep stop frequency is displayed.

Continuous Sweep (SWP) The generator fre sweeps from the start frequency limit, set frequency knobs **2**, to the stop limit, set by t set **5** knob.

Triggered Sweep (TRG SWP) The gener quiescent until triggered by a low to high e signal at Trig In or by the Trigger buttor receiving this trigger, the generator makes a sweep at the selected sweep time start ar frequencies. If the trigger signal is low at t of a sweep, the generator returns to the qui state. If the trigger is high at the end of a sweep, the generator returns to the start frequency and runs continuously until the next trigger pulse.

For proper operation, repetition rate of the trigger pulse should not exceed twice the sweep time.

An annunciator on the display indicates the selected mode.

16 Trigger In Connector The Trig In connector accepts a positive-going TTL level input (t_1) to trigger and gate the generator, as shown in figure 3-4. A negative-going edge (t_2) ends the gated operation. When triggered, the generator produces one complete cycle for each trigger input. When gated, the generator produces continuous cycles until the gate signal (t_2) is removed; the last cycle started is always completed (t_3).

17 Function Switch The Func switch, when pushed on the left or right, steps through the six function of the Model 22: sine ∿, triangle ∿, square ⊓⊔, ramp up ⟋, ramp down ⟍, and dc. An annunciator on the LCD display **1** indicates the selected function. Ramps are only available at frequencies at or below the 1.100 kHz range.

18 VCG In Connector This connector accepts 0 to ± 5V ac or dc input signals, which, when summed with a level proportional to the frequency knobs setting, controls the output frequency within the selected range. Positive input levels increase the frequency, while negative inputs decrease the frequency. Frequency excursions of 1100:1 are possible by placing the Frequency knobs **2** to full clockwise (0 to − 5V) or counterclockwise (0 to + 5V). Input impedance is 5kΩ. VCG slew rate is 0.1V/μs. If frequency stabilization is selected, the VCG In connector is internally disconnected.

19 Stabilizer Switch The Stab button references the generator to an internal standard which maintains the frequency within ± 1 (least significant) digit. An annunciator on the LCD display **1** indicates the status of the stabilizer. The stabilizer works only in the continuous mode and with an internal reference.

3.3 OPERATION

Perform the initial checkout procedure in Section 2 for a feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.2. Bold numbers are keyed to figure 3-1. Outputs are shown in figure 3-4.

3.3.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, figure 3-5 shows proper termination of the Func Out (50Ω) connector. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

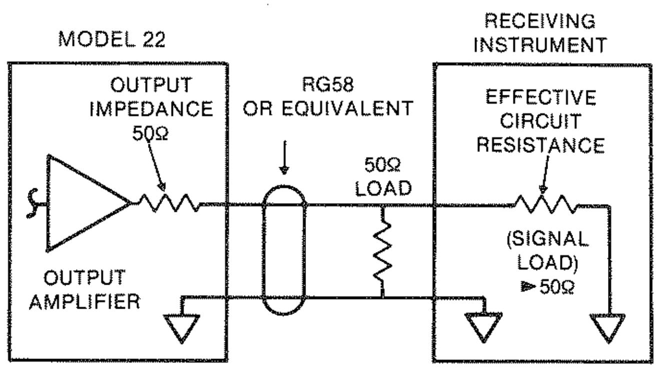


Figure 3-5. Signal Termination

The input and output impedances of the generator connectors are:

Connectors	Impedance
Func Out (50Ω) **7**	50Ω
Func Out (− 20 dB) **9**	50Ω
Sync Out **11**	TTL
Swp Out **14**	600Ω
Trig In **16**	TTL
VCG In **18**	5kΩ

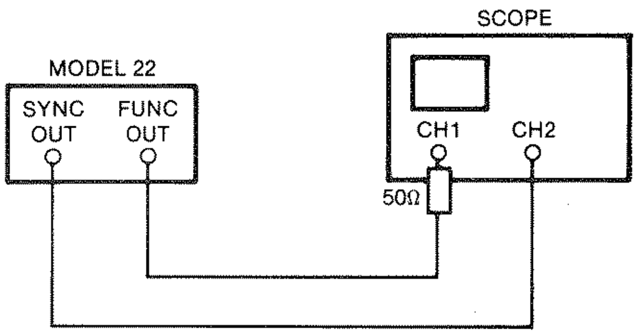
3.3.2 Continuous Operation

The basic generator supplies a continuous function (waveform) at a fixed frequency set by the operator.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **15**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).

Control	Setting
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate continuous operation connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	Scope Settings
Power: On	Time base: 0.2 ms/div.
Amplitude: cw	CH1 Vert: 2V/div
D.C. Offset: Off	CH2 Vert: 2V/div.
Frequency knobs: cw	Trigger: CH2.
	Display: CH1.

Observation: The scope displays a 1.1 kHz 10 Vp-p sine wave.

3.3.3 Voltage Controlled Generator (VCG) Operation

VCG is an external electronic means of controlling the frequency of the generator by using signal levels of up to 5V peak. This allows the generator to be swept (up or down in frequency) or frequency modulated.

Control	Setting
Freq Range **13**	Set to the desired frequency range. Frequency can only be changed within a range.
Frequency Coarse and Fine **2**	For positive dc inputs at VCG In, set the Frequency knobs to the lower frequency limit. For negative dc inputs at the VCG In, set the Frequency knobs to the higher frequency lim For modulation with ac input at VCG In, set Frequency knobs at desired center freque
VCG In **18**	As required.
Mode **15**	Select continuous.
D.C. Offset **3**	Set as desired. Limit set to prevent clipp (see figure 3-3).
Amplitude **4**	Set to desired out level at Func Out (50Ω Func Out (−20 dB).
Func **17**	Set to desired functi
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit ur test (refer to paragr 3.3.1).
Lin/Log **10**	Select desired mode

NOTE

Excessive VCG input voltage may cause nonlinear operation when the generator attempts to exceed the range limits.

The generator can be swept up to 1100:1 with a 5V ir signal to the VCG In connector. With the frequency to 1100, excursions between −5 and 0V at VCG In vide a 1100:1 decreasing frequency. With the freque set to 0001, excursions between 0V and +5V at the V In provide a 1100:1 increase frequency within the quency range.

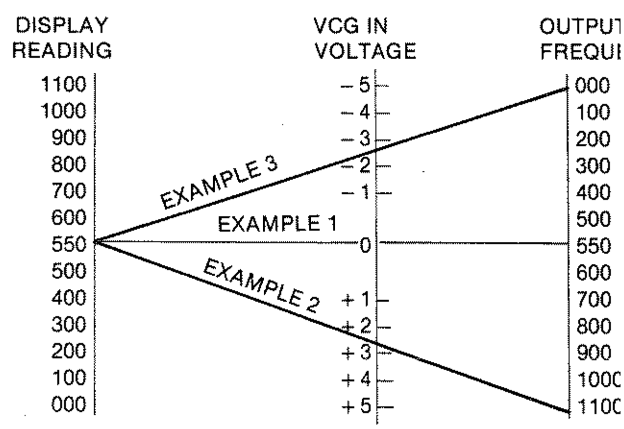
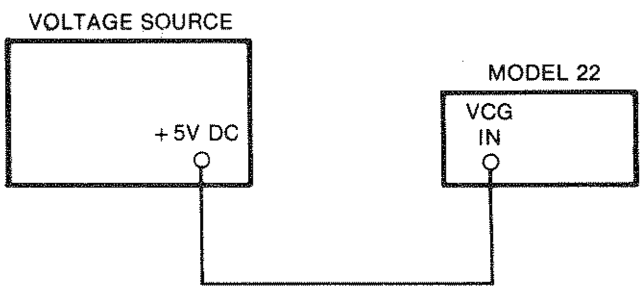


Figure 3-6. VCG Nomograph

The VCG nomograph, figure 3-6, gives examples of how an input voltage affects the output frequency (LIN). Example 1 shows that with 0V VCG input, the Frequency knobs determine the output frequency. Example 2 shows that a positive VCG input increased the output voltage. Example 3 shows that a negative VCG input decreases the output frequency. In the nomograph decimal points are not shown. The output frequency must be multiplied by the range. For example, in example number 2 if the frequency range is set to the .001 to 1.100 kHz range, the display will read .550 kHz and when the VCG voltage is applied the display will read 1.1 kHz.

To demonstrate VCG operation, connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	Voltage Source Settings
Power: On	Output level: +5Vdc.
Frequency knobs: ccw	

Observation: The display reads approximately 1.1 kHz.

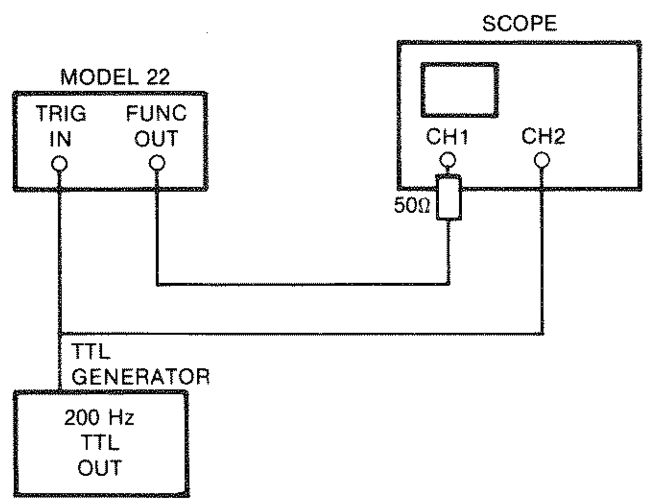
3.3.4 Triggered Operation

A triggered generator produces a single waveform each time a trigger signal is received. The Model 22 can be triggered by manual control or with a TTL signal.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Mode **15**	Select Trigger.
Trig In **16**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Trigger **8**	Press to trigger.

The triggered waveform starts from a quiescent point i.e., sine and triangle (0Vdc), square and ramp up (lower level), ramp down (upper level). All waveforms may be d.c offset). The Model 22 triggers on the rising (_/‾) edge of the trigger signal.

To demonstrate trigger operation, connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	CH2 Vert: 2V/div.	
D.C. Offset: Off	Trigger: CH2	
Mode: Trigger	Display: CH1 and 2.	

Observation : Scope Channel 1 displays a single 1.1 kHz, 10Vp-p sine wave coincident with the rising edge of the trigger input signal (CH2).

3.3.5 Gated Operation

A gated generator produces a continuous output waveform for the duration of the trigger signal. The Model

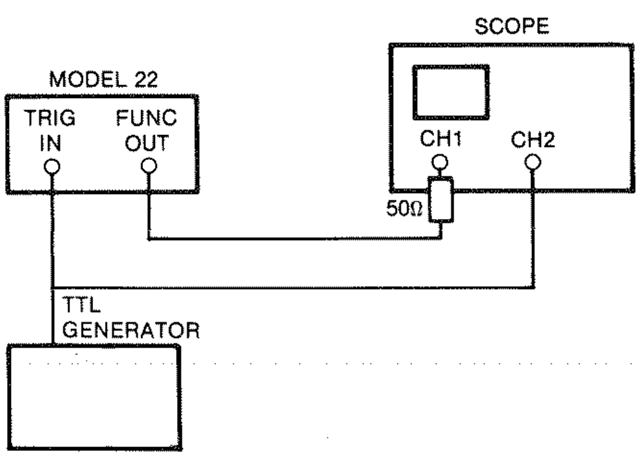
22 can be gated by manual control (Trig Switch) or with an external TTL signal (Trig In).

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **16**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Mode **15**	Select Gate.
Trigger **8**	Press in to start gate; release to stop gate.

The gated waveform starts from a quiescent point i.e., sine and triangle (0Vdc), square and ramp up (lower level), ramp down (upper level). All waveforms may be dc offset.

The instrument gates from the rising edge (_/‾) to the falling edge (‾_) of the Trig In signal. The last cycle started will be completed.

To demonstrate gate operation, connect the instrument as shown below, then set the controls as listed below.



Model 22 Settings	Scope Settings	T… Gene…
Power: On	Time base: 1ms/div.	Frequ… 200 H…
Amplitude: cw	CH1 Vert: 2V/div.	Outpu…
D.C. Offset: Off	CH2 Vert: 2V/div.	Level:
Frequency knobs: cw	Trigger: CH2.	
Mode: Gate	Display: CH1 and 2	

Observation: Scope CH1 displays gated sine waves ing at the rising edge of the trigger input (CH2) and e after the falling edge of the trigger input.

3.3.6 Stabilizer Operation

The stabilizer, when turned on, locks the freque the display frequency reading. Stabilizer circuit tains the generator frequency at this setting stabilizer works on all frequency ranges. Thus, tl quency range can be changed without unlockii stabilizer.

Control	Setting
Freq Range **13**	Set to the desire quency range.
Frequency Coarse and Fine **2**	Set to the desire quency within a ra
Mode **15**	Select continuous
D.C. Offset **3**	Set as desired. Lir set to prevent cl (see figure 3-2).
Amplitude **4**	Set to desired c level at Func Out (5 Func Out (−20 dl
Func **17**	Set to desired fun
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit test (refer to para 3.3.1).
Stab **19**	Select On.

3.3.7 Sweep

The Model 22 uses an internal generator to line logarithmically change the output frequency. Tl can be continuously swept or triggered swept.

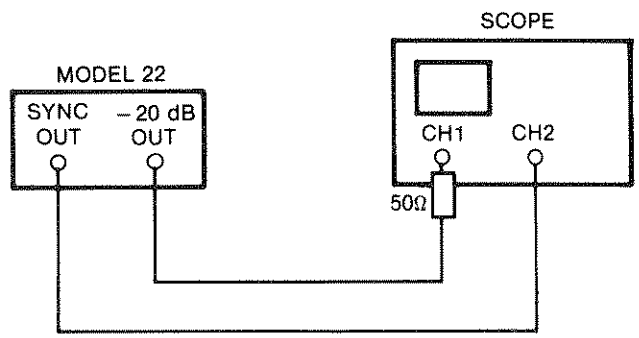
3.3.7.1 Continuous Sweep

For continuous sweep, the generator sweeps fr start frequency to the stop frequency in a contin occurring sweep.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Mode **15**	Select continuous to set the start frequency, Set to set the stop frequency, and, finally, Sweep for continuous sweep.
Frequency Coarse and Fine **2**	These controls set the desired start frequency within a range. In the Continuous mode, the display **1** shows the start frequency.
Swp Set **5**	This control sets the desired stop frequency within a range. In the Set mode, the display **1** shows the stop frequency.
Lin/Log **10**	Select either linear or logarithmic sweep.
Swp Time **12**	Select one of the four sweep times. Sweep rate should be << generator waveform frequency.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.

Model 22 Settings	Scope Settings
Power: On	
Mode: Continuous Frequency knobs: Set to 0.001 kHz	Time base: 1ms/div. CH1 Vert: 2V/div.
Mode: Set Frequency knobs: Set to 1.100 kHz	CH2 Vert: 2V/div.
Mode: Swp	Trigger: CH2 (– slope) Trigger Mode: Norm Display: CH1 and CH2
Amplitude: cw D.C. Offset: Off Lin/Log: Lin Func: sine wave	



Observation: The Model 22 continuously sweeps from approximately 1 Hz to 1.100 kHz at a 0.01 second rate.

3.3.7.2 Triggered Sweep

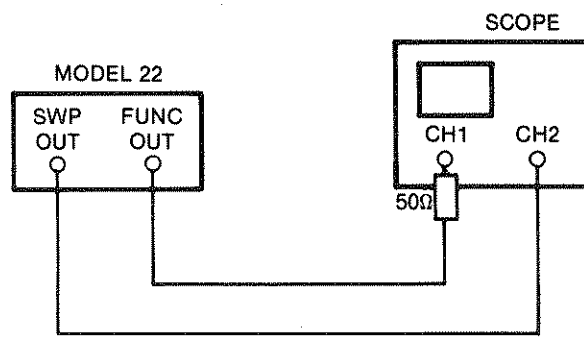
For triggered sweep, the generator sweeps from the start frequency to the stop frequency upon receipt of a trigger. The trigger can be handled in two differenct ways. First, if the trigger input returns low before the output reaches the stop frequency, the output returns to a quiescent level (same as in triggered mode). If the trigger input remains high after the output reaches the stop frequency, the output returns to the start frequency.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range. In the Continuous mode, the display **1** shows the start frequency.
Swp Set **5**	This control sets the desired stop frequency within a range. In the Set mode, the display **1** shows the stop frequency.
Lin/Log **10**	Select either linear or logarithmic sweep.
Swp Time **12**	Select one of the four sweep times.

D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Mode **15**	Select Continuous to set the start frequency, Set to set the stop frequency, and Trigger Sweep for that mode.
Trigger **8**	Press for manual trigger.
Trig In **16**	For external trigger, connect to TTL signal source.
Func **16**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate triggered sweep operation, connect the instruments as shown below, then set the controls.

Model 22 Settings	**Scope Settings**
Power: On	
Mode: Continuous	Time base: 10ms/div.
Frequency knobs: Set to 0.001 kHz	CH1 Vert: 2V/div.
Mode: Set	CH2 Vert: 2V/div.
Swp Set: Set to 1.100 kHz	
Mode: Trigger Sweep	Trigger: CH2
	Trigger Mode: Au
Swp Time: 1 Sec	
Amplitude: cw	Display: CH1 and
D.C. Offset: Off	
Lin/Log: Log	
Func: sine wave	
Trigger: Press once and immediately release it.	



Observation: The output is at a quiescent state un manual trigger is pressed. At this time the output sw from approximately 1 Hz to 1.1 kHz in 1 secon returns to the quiescent state.

Trigger: Press and hold until completion of swee

Observation: The output is at a quiescent state un manual trigger is pressed. At this time the output sw from approximately 1 Hz to 1.1 kHz in 1 secon returns to 1 Hz.

4.1 INTRODUCTION

The Model 22, an 11 MHz stabilized sweep function generator, operates as an analog waveform generator at frequencies above 1.100 kHz and a digital waveform synthesizer at frequencies below 1.100 kHz. The frequency, regardless of range, can be stabilized to the display frequency. In addition, all frequency ranges may be logarithmically or linearly swept.

As shown in figure 4-1, the function generator loop, controlled by Frequency Coarse and Fine verniers, VCG In, Trig In and the stabilizer (ASWP), is the heart of the generator. On the top four frequency ranges (11.00 kHz, 110.0 kHz, 1.100 MHz, and 11.00 MHz), the fur generator loop produces triangle and square wave are routed directly to the function selector located output block; a sine converter, also in the output l modifies the triangle into a sine wave. The waveforr thesizer, which is clocked by the function generatc via the stabilizer (MFSQ), produces all the wave on the five lower frequency ranges (110.0 1.100 Hz, 11.00 Hz, 110.0 Hz, and 1.100 kHz). Th thesizer output, like on the top four frequency ra is routed through the function selector to the outpu all ranges, the output block selects and controls th put signal at the Func Out (50Ω), Func Out(– 20dE

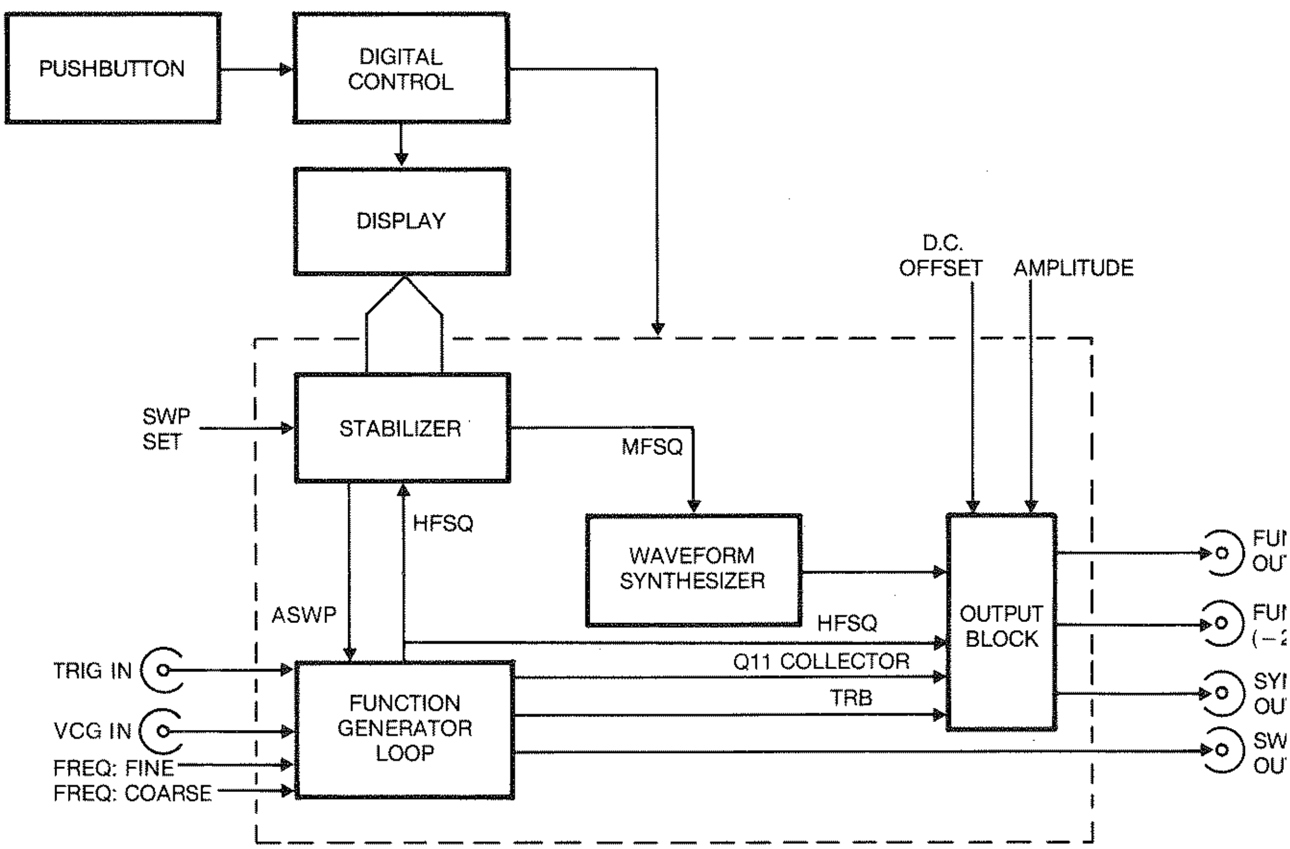


Figure 4-1. Model 22 Block Diagram

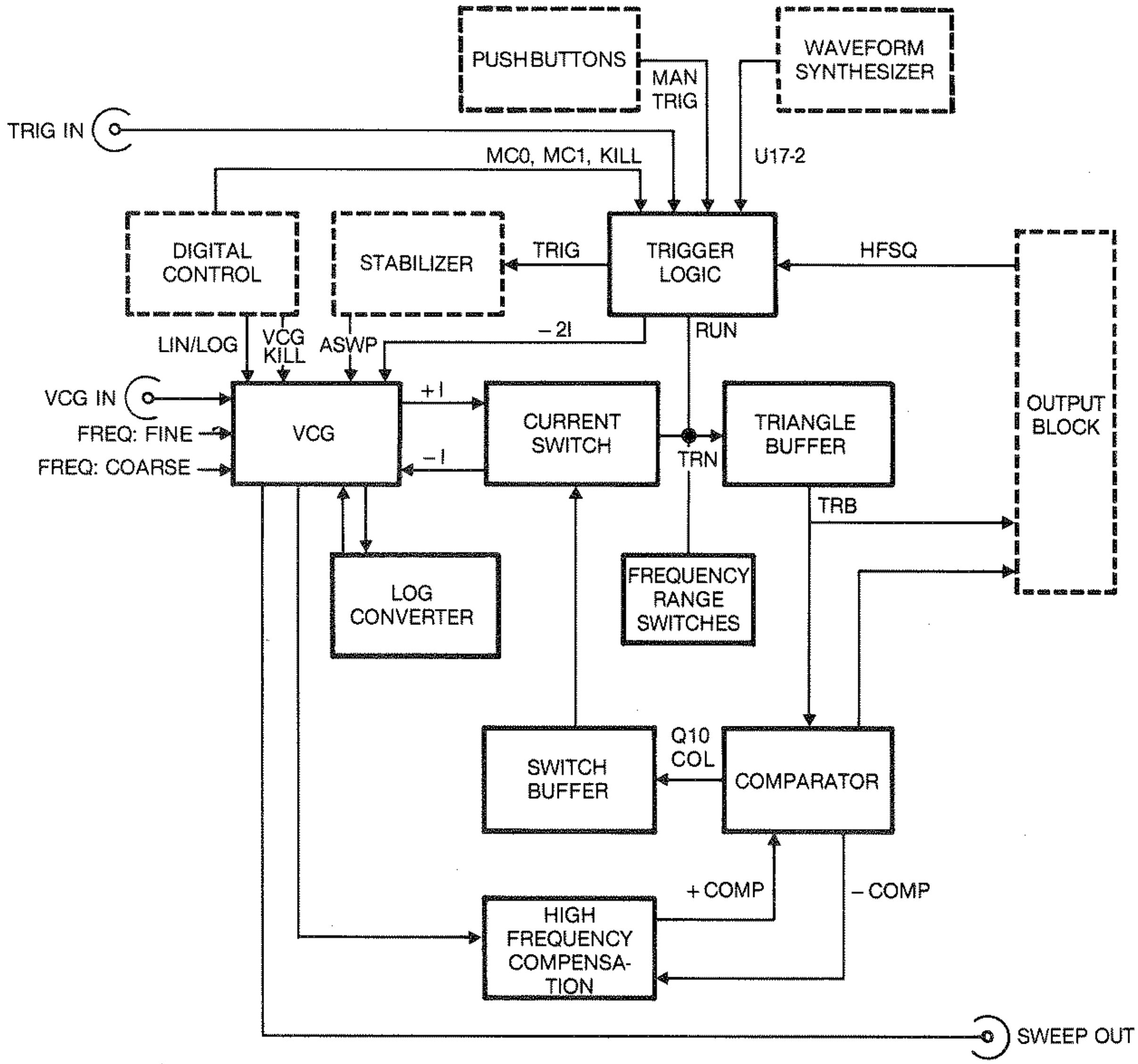


Figure 4-2. Function Generator Loop

Sync Out connectors; the output block is controlled by the digital control, Amplitude and DC Offset controls. The stabilizer, when in Stab mode, monitors the frequency, the same as shown on the display, from the function generator loop and supplies a feedback voltage (ASWP) to the function generator loop; thus the stabilizer keeps the frequency within one least significant count regardless of the frequency range. Also, the stabilizer circuit sweeps the function generator loop by increasing the voltage (ASWP) over a period of time.

The digital control sets the circuits shown in the dotted outline to a default state each time the unit is turned on. The front panel pushbuttons via the pushbutton interface causes the digital control to change parameters in the various control circuits. The digital control along with the stabilizer controls the front panel display's digits and annunciators.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Function Generator Loop

Figure 4-2 shows an expanded diagram of the function generator loop that consists of the VCG (voltage controlled generator), log converter, current switch, frequency range switches, triangle buffer, comparator, switch buffer, high frequency compensation, and trigger logic circuits.

The VCG produces two currents (+ I and − I), alternately switched in and out by the current switch and controlled by the output of the switch buffer, that charge (+ I) or discharge (− I) one of four range capacitors in the frequency range switches to produce a linear triangle. The specific frequency is determined by the magnitude of the + I and − I currents. The triangle buffer amplifies the triangle and drives the comparator. The comparator detects the triangle peaks which causes the comparator to switch output states; the threshold level of the comparator is controlled by the high frequency compensation circuit. The output of the comparator controls the switch buffer output state which, in turn, controls the current switch. The function generator loop only produces the top four frequency ranges, the five lower ranges are produced by using the function generator loop to clock the waveform synthesizer. The log converter supplies the VCG with a current logarithmically proportional to the Frequency knobs' settings and VCG In voltage. The trigger logic circuit enables or disables the function generator loop depending on the selected mode.

4.2.1.1 VCG

The VCG (ref: schematic 0103-00-1116 sheet 1) consists of the VCG amplifier, current sources, current sink, and trigger control current sink. The VCG amplifier (U1 pin 1) converts voltages from the VCG In (except in Stab mode), FRFINE (Frequency Fine), FRCOARSE (Frequency Coarse), and ASWP (stabilizer or sweep) into currents that controls the current source and sinks (U28). The magnitude of the current sets the frequency within the selected range. A gain adjustment (R1) controls the top-of-range frequency, where as R13 sets the 1100:1 (bottom-of-range) frequency. R11 controls the offset of the amplifier and zener diode CR1 limits the voltage swing at U1 pin 1 to within 30% over the maximum allowable swing. CR2 and CR3 prevent excessive voltages at VCG In from damaging the VCG amplifier.

Current Source and Current Sink: The current source and current sink supply the current charging (+ I) and discharging (− I) the frequency range capacitor. The negative signal from the VCG amplifier (U1 pin 1) is converted into a current leaving summing node at U1 pin 9 through R1 and R12. U1 pin 8 controls current sunk by Q1 which, in turn, controls current sourced by Q2 and the two transistors in the upper half of U28.

Operational amplifier (U1 pin 8) holds pin 9 at ground potential. When pin 9 tries to go negative, pin 8 goes positive, which causes Q1 to sink current through R18.

This lowers the voltage at the base of Q2 and th
transistors in U28 which sources sufficient cu
through Q2's collector to hold U1 pin 9 at 0V; incre
current now flows from the current source (U28 pi
CR4 limits the voltage swing at U1 pin 8 to within
of the maximum allowable swing.

An increase in current through R42 pin 16 appear
a positive input to the operational amplifier (U1
driving the output at pin 7 positive. This raises the vc
at U28 pin 1 that causes pin 3 to sink more curren
virtually all the current through R42 pin 16 pa
through U28 pin 3, maintaining a virtual ground
pin 5. Increased current now flows into the curren
(− I) through U28 pin 6 which tracks the current sc
The emitter resistors for Q4 and U28 pins 2 and
all 1kΩ, therefore the collector currents at U28 pin
(pin 6), and Q4 will be equal.

Trigger Control Current Sink: The trigger contrc
rent sink clamps the triangle node (TRN) at ground
tial during the "off" state in the triggered and
modes.

When the generator is gated "off", RUN goe
reverse biasing CR7. As the triangle at TRN rises to
the zero crossing point, a greater proportion of th
current, emitter resistor at U28 is 500Ω, flows th
U3 pin 9. Equilibrium is reached when the trigger h
current is equal to the positive current (+ I) bein
plied to the generator loop, preventing the triangle
voltage from rising any further. The matched dio
U3 have equal currents through them [(− I) + (
(− 2I)] and the anode at pin 4 is grounded, henc
voltage drops across the two diodes are equal a
triangle node is held at ground potential. This sto
triangle waveform on the rising slope and ensure
at least one complete cycle will be generated ever
the generator is triggered. Also, refer to para
4.2.1.9 Trigger Logic.

4.2.1.2 Log Converter

The log converter transforms the linear change
frequency knob to a logarithmic current that contr
current source. The logarithmic converte
schematic 0103-00-1116 sheet 1) consists of trar
Q3 and amplifier U24 that uses the logarithmic
emitter characteristics of the output half of the trar
(Q3) to produce the logarithmic current. Varying t
put transistor's emitter voltage controls the cur

The converter receives its input from the VCG inp
cuit at R31. A constant 3mA through R34 keeps th
transistor's base-emitter voltage at − 0.7V. Wh
Frequency knob is set at minimum frequency (0
emitters are biased at − 0.7V (base of the

transistor is fixed at $-0.3V$ by R36) which places 0.4V between the output transistor's base and emitter and supplies 1μA control current to the current source.

When the frequency knob is set at maximum frequency ($-7.5V$), the base of the input transistor is biased at $-0.3V$, thus biasing the emitters at $-1V$. This places the output transistor's base-emitter bias at 0.7V which supplies 1mA to the current source. Thus, the linear change in base to emitter voltage of the transistor generates an exponential change in collector current.

4.2.1.3 Current Switch

The current switch (ref: schematic 0103-00-1116 sheet 2) consists of the diode switches (CR10, 11, 12, 13), current source buffer (Q7) and current sink buffer (Q17). Controlled by the square buffer, the current switch allows the charging ($+I$), and discharging ($-I$) of the selected frequency range capacitor (see Frequency Range Switches) to produce a triangle waveform.

The current switch sources current buffered by Q7 ($+I$) or sinks current buffered by Q17 ($-I$) at the switch output (junction of CR10 and CR12). The instantaneous polarity of the switch buffer output control line (junction of R59 and R60) determines the direction of current flow.

With the control line at $+2V$ which reverse biases diodes CR11 and CR12, the $+I$ current through CR10 charges the selected timing capacitor. At the same time, current flows from the control line through CR13 into the current sink. With the control line at -2V which reverse biases diodes CR10 and CR13, the timing capacitor discharges through CR12 to the current sink and the $+I$ current is sourced through CR11 into the control line.

4.2.1.4 Frequency Range Switches

The frequency range switches (ref: schematic 0103-00-1116 sheet 2) consist of the four basic range capacitors and their controls. Each range capacitor or set of capacitors covers 10% to 100% of full scale. A logic level signal from the frequency range control circuit switches in the range capacitor. For example, when $\overline{FR6}$ goes low, it turns on Q22 which sources about 30 mA through R108 and diodes CR25 and CR26. With CR26 forward biased, the diodes impedance to ground is less than 2Ω and the range capacitor set (C40, C41 and C42) is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, Q22 is turned off, and R109 pulls the anode of CR25 to $-15V$. The voltage divider (R106, R107) biases the anode of CR26 to $-7.5V$ reverse-biasing CR26 which provides a very high impedance to ground effectively disconnecting the range capacitor. Frequency range control lines ($\overline{FR4}$ or $\overline{FR5}$) operate the same way by connecting matched capacitors of 0.0047 μF (C43) or 0.047 μF (C45) to the triangle node (TRN) line. Capacitance for the highest frequency range (100 pF) consists of all the stray capacitance at TRN and the 11 MHz adjustment capacitor (C39 and C38). Frequency range control line ($\overline{FR6}$) connects an additional 400 pF (C41, C42) and the 1.1 MHz adjustment (C40) to TRN.

4.2.1.5 Triangle Buffer

The triangle buffer (ref: schematic 0103-00-1116 sheet 2), a high speed FET input voltage follower with a low impedance output and unity gain, buffers the current switch and frequency range capacitor from relatively high current circuits in the output block and the comparator.

The triangle buffer consists of Q14, acting as a high input impedance source follower, and Q15, acting as a low output impedance emitter follower. The difference between the input and output voltage of the circuit is controlled by adjusting the current through Q14, such that, the gate-source voltage is equal and opposite to the base-emitter drop of Q15, this causes the two voltages to cancel each other. The baseline adjustment (R103) sets the current through Q14.

4.2.1.6 Comparator

The comparator (ref: schematic 0103-00-1116 sheet 2) detects the peak of the triangle and produces two separate square wave outputs. One square wave output from the comparator (Q10 collector) drives the switch buffer, while a second square wave of opposite polarity (Q11 collector) drives the output block. The comparator's threshold voltage is set by the +COMP and −COMP from the high frequency compensation circuit.

When the triangle voltage at the base of Q19 reaches the positive threshold voltage ($+1V$ at U3 pin 2), Q19 turns on as Q18 turns off. When Q18 and Q19 switch, they cause the second differential pair, Q10 and Q11 to switch. As Q10 switches "off", current through R63 decreases and the collector of Q10 goes low, (about $-1.6V$); the current drain through R90 determines the collector voltage of Q10. CR17 and CR18 increase the transistor switching speed of Q18 and Q19 by limiting the signal swing at their collectors to about 0.7V. Resistors R64 and R71 increase the switching speed of Q10 and Q11 by providing a small current which keeps them from turning completely off, and diodes CR16 and CR19 are switched on and off to further guarantee that Q10 and Q11 do not switch off.

Diode bridge (U3 pins 5, 6, 8) operate identically to the current switch. The switch buffer output (U3 pin 6) state determines the polarity of the comparator threshold voltage (U3 pin 2). The comparator threshold voltage is limited to $\pm 1V$ by the voltage drop across the 332Ω resistor (R92), the +COMP and −COMP currents supply 3mA. The high frequency compensation circuit reduces the +COMP and -COMP currents on the highest frequency range which lowers the comparator threshold voltage at the base of Q18 to compensate for switching delays (see paragraph 4.2.1.8).

Output transistors Q10 and Q11 have different values of collector and emitter resistors to match the input requirements of each buffer.

4.2.1.7 Switch Buffer

The switch buffer (ref: schematic 0103-00-1116 sheet 2) shifts the level of the comparator's square wave to provide a voltage excursion (±2.2V) capable of driving the current switch. The switch buffer is a complementary emitter follower biased on by the voltage drops across CR14 and CR15 and controlled by the comparator output at the collector of Q10. The ±2.2V square wave output controls the current switch and the polarity of the comparator threshold voltage.

4.2.1.8 High Frequency Compensation

High frequency compensation (ref: schematic 0103-00-1116 sheet 2) circuit sets the threshold voltage of the comparator. On the lower frequency ranges (110.0 mHz through 1.100 MHz), the value of the +COMP and −COMP currents set up the comparator threshold voltage at the base of Q18; each current has a fixed value of 3mA through the resistor R92. On the 1.00 to 11.00 MHz range, the threshold voltage is lowered to compensate for switching delays in the function generator loop; this maintains the triangle peaks at the same levels as on lower ranges.

On the lower frequency ranges with HF COMP disconnected, R80 and R81 holds U27 pins 2 and 3 and the emitter of Q5 at 0.0V. This puts 15V across series resistors R83 and R85 and −10V at the base of Q16. The same current that flows through R85 also flows through R52. This puts +10V at the base of Q6. The emitter of Q6 is +10.7V which causes 3mA to flow from the collector of Q6 through U3 and R92 to ground during half of the cycle setting up a threshold voltage at the base of Q18. On the opposite half of the cycle, the base of Q18 switches to −1V because the same amount of current (3mA) flows from ground through R92 and U3 to the collector of Q16.

In the 11.00 MHz frequency range, HF COMP (U2 pin 10 of the VCG) is connected to U27 pin 3. At top of the range, 2.5mA is sinked from ground through R80 and R81 to the collector of Q4 in the VCG lowering the voltage at U27 pin 3 to about −5V. This decreases the voltage at the emitter of Q5, as well as the current through R83, R85, and R52 which places the bases of Q6 and Q16 closer to their respective power supply voltages. The rent through R92, the collectors of Q6 and Q16, an threshold voltage at the base of Q18 are all decrea This new lower threshold voltage causes the trian switch earlier than normal. The threshold voltage o range is inversely proportional to the Frequency Cc and Fine settings.

4.2.1.9 Trigger Logic

The trigger logic circuit (ref: schematic 0103-00- sheet 3) allows the generator to be externally trig or gated. When in trigger or gated modes (deterr by MC0 and MC1), the Trigger Logic circuit preven generator from running by sinking away the curren the triangle node (TRN) that would normally charg frequency range capacitor. Pressing the Trigger b or connecting a signal to the Trig In (TTL) BNC rele TRN to allow the generator to run until HFSQ comp one complete cycle. In addition, when the frequ range is 1.1kHz or lower, the synthesizer output pin 6) must be high to disable the function generator When in DC function, $\overline{\text{KILL}}$ inhibits the generato

The following sections describe the relations various conditions relative to the trigger logic.

Continuous Mode: In Continuous Mode, U12 pin 4 (is low which holds U12 pin 6 low and sets U23 pin 5 $\overline{\text{KILL}}$ (U22 pin 13) is high and U22 pin 11 is low for all tions except DC. This sets U23 pin 9 high enablir function generator loop.

Trig Mode: In Trig Mode, U12 pin 4 (MC0) is helc and U15 pin 4 (MC1) is held low which forces U1 6 and U12 pin 6 high. If the Trigger pushbutton pressed, U15 pin 10 remains high and the signal a pin 8 is in phase with the Trig In signal at U21 pi

With no signal present at Trig In, U23 pin 3 is low. I is low, U22 pin 8 is high, and U23 pin 5 is low. If (U22 pin 13) is high, U22 pin 11 will be high. U20 p (LF) is low for frequency ranges 11.00kHz and a this forces U20 pin 8 high. Since U22 pin 2 is high pin 12 will be low. U23 pin 9 will be low disabling the tion generator loop.

Each time the Trigger pushbutton is pressed U15 goes low or on each positive transition of the T signal, U23 pin 5 is clocked high. With $\overline{\text{KILL}}$ (U22 p high, U22 pin 11 goes low which sets U23 pin 9 (high and enables the function generator loop. A positive transition of HFSQ (U22 pin 9), U23 pin 11 low. On the next negative transition of HFSQ, U2 11 goes high, which clocks the low at pin 12 to pin 9 (and stops the triangle on its rising edge. Only one of generator output is enabled for each trigger applied.

Gate Mode: In Gate Mode, MC1 (U15 pin 4), MC0 (U12 pin 4), U15 pin 6, U12 pin 6, and U15 pin 10 are high while U23 pin 3 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. When LF (U20 pin 10) is low (frequency ranges 11.00 kHz and above), U20 is forced high, and because $\overline{\text{SWPRUN}}$ is high in gate mode, U22 pin 3 will be low which disables the generator.

When Trigger on the front panel is pressed (U15 pin 10 goes low) or a positive transition at Trig In (U21 pin 13 goes high), U15 pin 8 goes high which clocks the Q output (U23 pin 5) high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and enables the generator. As long as the trigger signal at Trig In remains high or the Trigger pushbutton is pressed, U15 pin 6 and U12 pin 6 will remain low, that sets U23 pin 5 high, forces U23 pin 10 (S) low, sets RUN (U23 pin 9) high, and enables the function generator loop by releasing TRN.

When U23 pin 3 goes low, U15 pin 6 and U12 pin 6 go high. The next negative transition of HFSQ shifts U22 pin 8 high, clocks the low at pin 12 to the output at pin 9 (RUN), and disables the triangle at 0V.

Low Frequency: When the Frequency range is 1.1 kHz or lower, the trigger logic works much the same as previously described, except U23 pin 12 must be low to stop the generator. This occurs at either the zero crossing of the rising edge of the triangle (Haver Off), or at the negative peak of the triangle (Haver On). If Haver is Off, U13 pin 6 (waveform synthesizer) functions as a zero crossing detector that controls the trigger logic. If Haver is on, U16 pin 6 (waveform synthesizer) acts as a negative peak detector. U22 pin 6 goes low in either condition. With U22 pin 6 high, the next positive transition at U17 pin 3 forces $\overline{\text{Q}}$ (U17 pin 6) low. For the five lowest frequency ranges, LF (U20 pin 10) is high, this makes pin 8 high and causes U22 pin 3 to go low.

Sweep Mode: For the three sweep modes, the trigger logic functions much the same as for the other modes. For Set and Sweep modes, the trigger logic functions exactly the same as the continuous mode. For triggered sweep mode, the trigger logic allows the function generator loop to run depending upon the condition of the Trig In signal. If $\overline{\text{SWPRUN}}$ is low, the trigger logic's RUN line remains high this allows the generator to keep running. But if $\overline{\text{SWPRUN}}$ goes high the RUN line will go low at the next positive transition at U23 pin 11, this shuts off the function generator loop and always completes the last cycle.

DC Function: If Func is set to DC, U22 pin 13 ($\overline{\text{KILL}}$) will be low. This clears U23 which forces U23 pin 9 low and disables the generator.

4.2.2 Waveform Synthesizer

The waveform synthesizer produces the digitally synthesized waveforms used on the five lower frequency ranges (1.100 kHz and below). It consists of seven circuits: ÷1/÷100 counter, reference selector, ÷1000 up/down counter, waveform EPROM, data selector, latch, and DAC, as shown in figure 4-3 and schematic 0103-00-1116 sheet 3.

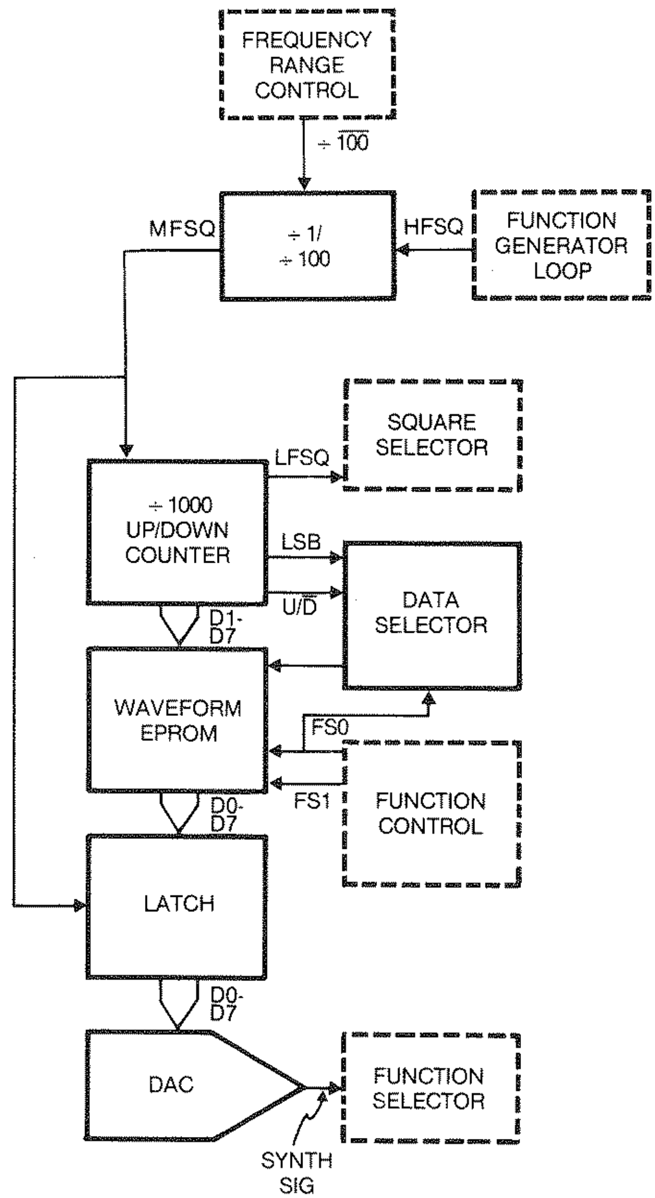


Figure 4-3. Waveform Synthesizer

The synthesizer reference originates at the function generator loop (HFSQ). This signal must pass through the ÷1/÷100 divider (U7B, U8B; ref: schematic a cur-

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0103-00-1115 sheet 3) where the frequency is either divided by 1 or 100, depending upon the selected frequency range, see table 4-1.

Table 4-1. Reference Selection

Frequency Range	Generator Loop Frequency (HFSQ)	÷1/÷100	Medium Frequency Square Wave (MFSQ)
.100 to 1.100 kHz	.100 to 1.100 MHz	÷1	1.100 to 1.100 MHz
10.0 to 110.0 kHz	10.0 to 110.0 kHz	÷1	10.0 to 110.0 kHz
1.00 to 11.00 kHz	1.00 to 11.00 kHz	÷1	1.00 to 11.00 kHz
.100 to 1.100 Hz	10.0 to 110.0 kHz	÷100	.100 to 1.100 kHz
10.0 to 110.0 mHz	10.0 to 11.00 kHz	÷100	10.0 to 110.0 Hz

The 9-bit up/down counter (U6, U10, U11, and U14) counts from 0 to 499, then reverses and counts from 499 to 0. The counter steering circuit (U11, U16, and U18) watches for the top and bottom counts, then reverses the direction of the counter. When the counter increments, U17 pin 12 is low and pin 8 is high. At the top count, U18 pin 1 toggles high disabling the counter for one cycle. Also at the top count, U17 pin 12 goes high and on the next clock pulse from U15 pin 11, U17 pin 8 (the counter up/down control line) goes low, causing the counter to begin to decrement, returning U18 pin 1 to its original low state. At the bottom count, U18 pin 1 again goes high and disables the counter for one cycle. U17 pin 12 goes low, and on the next clock pulse from U15 pin 11, U17 pin 8 goes high, this causes the counter to begin to increment. U18 pin 1 again returns low.

The counter output drives the inputs of EPROM (U9) which contains the data needed to produce the sine, triangle, ramp up, and ramp down waveforms. The status of lines FS0 and FS1 determine the waveform by selecting which block of data as accessed; see table 4-2. For sine and triangle waves, the EPROM produces one half cycle, negative to positive peak, on the up count (0 to 499), then uses the same data in reverse, positive to negative peak, on the down count (499 to 0). The data from the EPROM (U9) is latched through U8 to DAC U7.

Table 4-2. EPROM Control Lines

FS0	FS1	Function
0	0	DC
0	0	Sine wave
0	1	Triangle
1	0	Ramp up
1	1	Ramp down

The DAC converts the data from the EPROM into a
rent, SYNTH SIG, for the function selector.

The synthesizer can also produce ramp up and
down waveforms. These ramps are stored in the EF
(U9), as are the sine and triangle waveforms. To prc
the ramps, the line FS0 goes high; the line FS1 se
either the ramp up (FS1: low) or ramp down (FS1:
In generating the ramps, the up/down counter func
the same as it does for triangles and sine waves; cou
0 to 499 and 499 to 0, except that the least signi
bit to the EPROM is controlled by the data selector
U12). The U/D line (U17 pin 9) is the complement
line, it causes the counter to count up or down.
counting up, U/D is low which holds the least signi
bit low. This allows only even addresses to be acce
When counting down, U/D is high, the least signi
bit is held high and only odd addresses are acce

4.2.3 Stabilizer

The stabilizer serves three functions. First, it mea
the generator's frequency and drives the frequ
display. Second, it compares the displayed frequ
stored in latches, against the actual frequency
generator and makes slight frequency corrections
generator's frequency. And third, it steps the fur
generator loop through the sweep range. Figur
shows a block diagram of the stabilizer block.

4.2.3.1 Timing Generation

This circuit provides the timing control for the stab
As shown in schematic 0103-00-1115 sheet 2, th
MHz oscillator consists of crystal (Y1) and differ
amplifier (U9A). The output of this oscillator is di
to 50 kHz by U8A (at pin 9).

Four divide-by-10 counters (U5A, U6A) together wit
control devices, produce the GATE, MEMCLK, FR
and CLRCNT pulses which control the frequency
parator circuit. Figure 4-5 shows the timing diagra
the counters.

4.2.3.2 Prescalar

The prescalar (ref: schematic 0103-00-1115 sh
selects the clock for the 3½ digit BCD counter. The
frequency, regardless of the selected range, will a
be between 1.00 and 11.00 kHz. The prescalar bloc
sists of the HFSQ divider and selector.

The HFSQ divider (U9C, U8C) divides the HFSQ s
wave from the generator loop by 10, 100, and 1000
of these outputs drive the selector circuit. In ad
the divider includes the ÷1/÷100 counter (U7B) f
synthesizer block.

The selector (U9B), controlled by the frequency
control, determines which HFSQ divider output wil

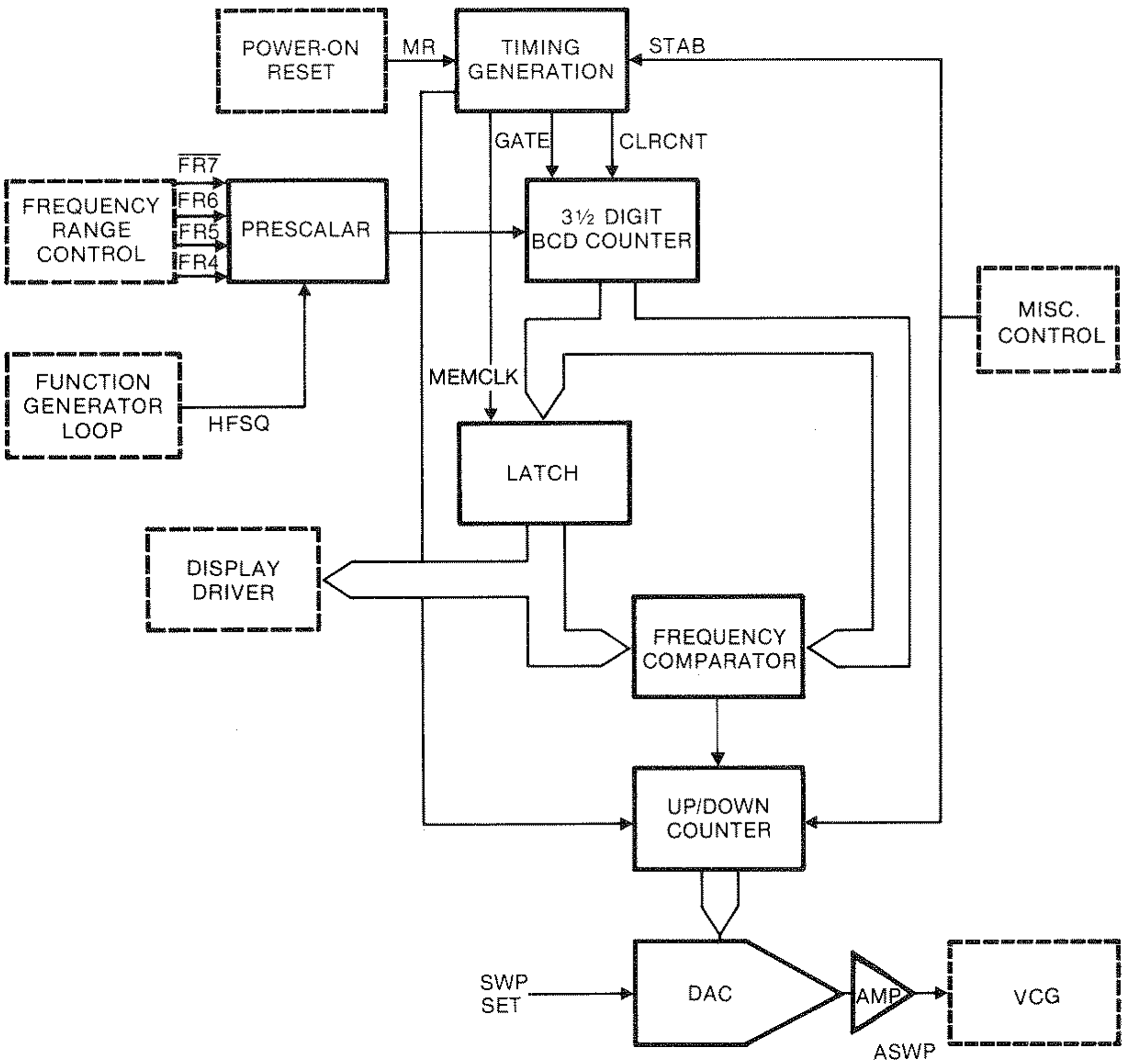

Figure 4-4. Stabilizer

the BCD counter. Table 4-3 shows the relationship between the ranges, generator loop frequency, and division ratio.

4.2.3.3 Frequency Counter

The frequency counter (ref: schematic 0103-00-1115 sheet 3) consists of a control flip flop (U6F) and four cascaded BCD ripple counters (U1A, U2A). This counter tallies the number of cycles from the prescalar over a 100 ms period. The output lines from the counter drive the frequency comparator.

When the GATE line goes high, the control flip flop (U6F) is enabled to allow the counter to count until the GATE

Table 4-3. Prescalar

Selected Freq Range (Hz)	Actual Function Generator Loop (Hz) Frequency	Divider	Counter Clock (Hz)
1.00 – 11.00 M	1 – 11 M (FR7)	÷ 1000	1 – 11 k
.100 – 1.100 M	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0 k	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00 k	1 – 11 k (FR4)	÷ 1	1 – 11 k
.100 – 1.100 k	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00	1 – 11 k (FR6)	÷ 100	1 – 11 k
.100 – 1.100	10 – 110 k (FR5)	÷ 10	1 – 11 k
10.0 – 110.0 m	1 – 11 k (FR4)	÷ 1	1 – 11 k

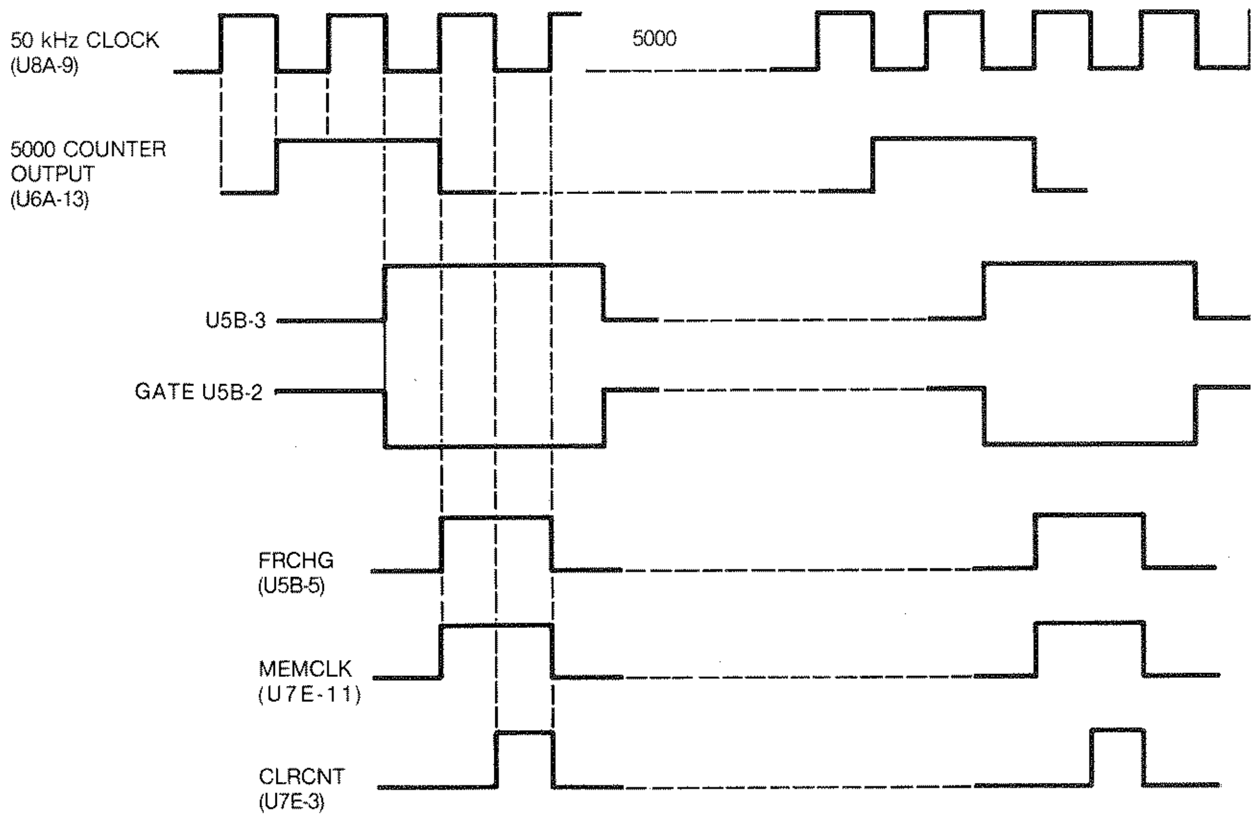

Figure 4-5. Timing Generation

line goes low, which inhibits the control flip flop. Approximately 20 μs after the GATE line inhibits the flip flop, the CLRCNT line clears the flip flop and counter, and when the GATE line returns high, the frequency counter again counts the frequency. For GATE and CLRCNT timing relationships, see figure 4-5.

4.2.3.4 Frequency Comparator

The frequency comparator (ref: schematic 0103-00-1115 sheet 3) serves two functions. First, it is part of the frequency display. Second, stabilizer enabled, it compares the input from the frequency counter with the stored frequency shown on the display. The resulting output at the two latches (U1B, U3B) and two comparators (U2B, U4B) controls the frequency correction or sweep block.

Latches: The latch (U1B, U3B) receives its data directly from the frequency counter. The MEMCLK, when it goes high for 20 μs, clocks the frequency data to the output registers of the latches. Outputs from the latch drive both the display drivers and Q inputs of the frequency comparators (U2B, U4B). The MEMCLK occurs about every 100 ms, see figure 4-5 for timing relation

When the stabilizer is enabled, the MEMCLK line re low holding the frequency data (displayed freq stored in the latches.

Frequency Comparator: The frequency comparatc sists of two individual comparators (U2B, U4B) th daisy chained together via gate U6C. It monitor from the frequency counter and compares the d and Q) with the outputs from the latches. This pro two control lines that control the up/down counte frequency correction or sweep circuit.

When the stabilizer is off, the P and Q lines are a the same (P = Q). When the stabilizer is on, the I can change while the Q data remains unchange comparator detects the change and switches its tv put lines (U4B pins 1 and 19) as shown in table sweep modes, Q6 is forced high and P6 is held low forces the comparator output to P<Q; this caus frequency correction and sweep circuit to always up.

Table 4-4. Comparator — U/D Counter Relationship

Condition	U4B Pin 19	U4B Pin 1	Correction U/D Counter
P=Q[1]	Low	High	Counter Disabled
P<Q[2]	High	High	Counts Up
P>Q	High	Low	Counts Down

NOTE

P Frequency data from the frequency counter.
Q Frequency data from the latches.
1 Also Stabilizer off condition.
2 Also Sweep condition.

4.2.3.5 Frequency Correction or Sweep.

When the stabilizer is on, the frequency correction circuit (ref: schematic 0103-00-1115 sheet 3), controlled by the frequency comparator, makes frequency corrections to the function generator loop. For sweep modes, the correction block steps the generator's frequency from a start frequency up to the stop frequency. This block consists of the 8-bit up/down counter (U9F, U8F) and the DAC (U8G) along with its summing amplifier (U9G).

8-Bit Up/Down Counter: The 8-bit up/down counter (U9F, U8F), controlled by two lines from the frequency comparator, uses its output to increment or decrement the DAC. Table 4-4 illustrates how the comparator controls the up/down counter. The counter preloads (1000 0000) for stabilizer to the center of the counter's range; for sweep modes it load to the bottom of the counter's range. If the stabilizer is on, the FRCHG pulse clocks the counter every 100 ms; see figure 4-5. In sweep modes FRCHG rate varies depending on the sweep time. When the stabilizer is turned on, the STAB line from the misc control logic goes high to enable the counter. For stabilizer off, the STAB line goes low and on the next FRCHG clock transition the outputs all go to a TTL low, except the most significant bit which is held high. The eight data lines from the counter directly drive the inputs of the frequency correction DAC.

Digital to Analog Converter and Summing Amplifier: The digital to analog converter (U8G), DAC, converts the 8 bits of digital data from the 8 bit up/down counter into a proportional analog current. The amplifier (U9G) sums the DAC's current to produce a voltage that, when the stabilizer is on, drives the ASWP input of the function generator loop. The reference voltage for the DAC depends upon the mode of operation. For the stabilizer mode, the reference is set by resistor R29 to the +15V supply. For sweep modes, the reference is set by the Sweep Set control (SWDTH).

4.2.3.6 Trigger Sweep Logic

The trigger sweep logic (ref: Schematic 0103-00-1115 sheet 3) detects the two kinds of sweep trigger that will control the function generator loop. If TRIG remains high at the end of the sweep, the generator returns to and runs at the start frequency. If TRIG returns low before the end of the sweep, the generator returns to its quiescent state (0Vdc).

The following describes the operating cycles for the trigger sweep logic circuit. The TRIG input goes high which clocks flip-flop (U9E pin 5) high thus resetting flip-flops U9D pin 4, U9D pin 10, and U9E pin 10. With U9D's $\overline{Q}$ output low ($\overline{SWPRUN}$), the function generator loop starts operating. Also, U9D pin 9 is preset high forcing U9E pin 7 low which enables the up/down counter.

If TRIG remains high at the end of the sweep time, then SWPRUN remains low but the counter will overflow (U8F pin 15 goes low) which holds the up/down counters. But when TRIG goes low before the end of the sweep, flip-flop U9D pin 6 ($\overline{SWPRUN}$) goes high which shuts off the generator. Also, the up/down counter overflows (U8F pin 15 goes low) which holds the up/down counters.

4.2.4 Output Block

The output block, shown in figure 4-6, consists of the square buffer, square selector, square shaper, sine converter, function select, preamplifier, output amplifier, and attenuator. It also has output protection circuits for both Func Out BNCs. The output block selects the appropriate waveform and connects it to the Func Out BNCs.

4.2.4.1 Square Buffer

The square buffer (ref: schematic 0103-00-1116 sheet 2) amplifies the square wave from the function generator loop (Q11 collector). The output (HFSQ) drives the trigger logic, frequency counter, and square selector. The square buffer is similar to the switch buffer (ref: paragraph 4.2.1.7) except for output phasing and output level: 0 to +5V. A highly differentiated portion of HFSQ is coupled through C24, C25 and C31 to the triangle node (TRN) to counteract switching transients coupled through the current switch.

4.2.4.2 Square Selector

The square selector (ref: schematic 0103-00-1116 sheet 3) picks either HFSQ from the square buffer or the low frequency square wave from the synthesizer. Outputs from the square selector drive the square shaper and Sync Out connector.

Above the 1.1 kHz frequency range, LF (U20 pin 13) is low which enables U20 pin 4 and routes HFSQ to the

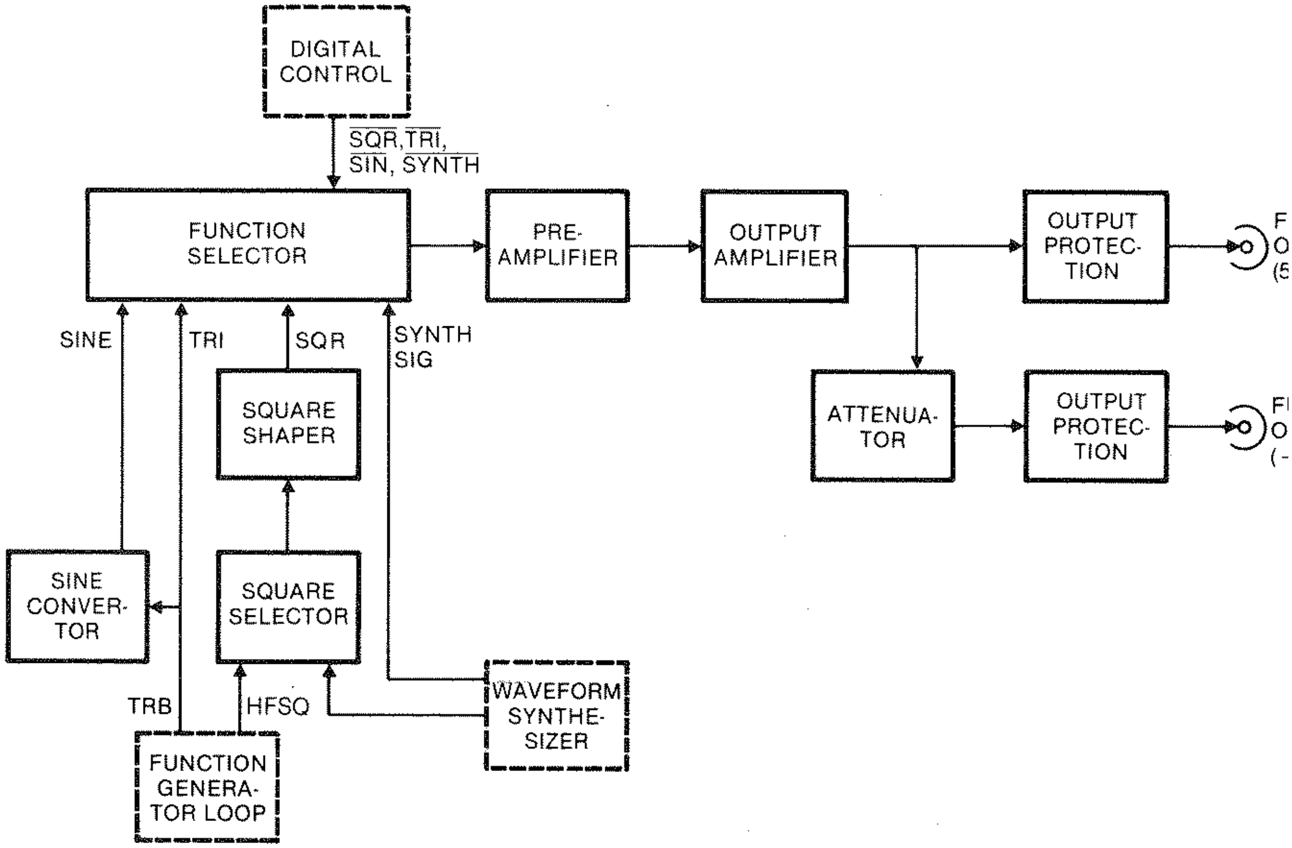

Figure 4-6. Output Block

Sync Out (U21 pin 6) and TTL SQ (U16 pin 12). For frequency ranges 1.1 kHz and below LF (U19 pin 9) is high, this enables U20 pin 3 and routes the square wave from the waveform synthesizer to the Sync Out (U21 pin 6) and TTL SQ (U16 pin 12).

If Func is set to square wave, $\overline{SQR}$ at U19 pin 5 will be low, which puts U16 pin 1 high. The signal at U16 pin 2 will pass in phase to the square shaper via TTL SQ. For all functions other than square wave, $\overline{SQR}$ will be high disabling TTL SQ (U16 pin 12).

4.2.4.3 Square Shaper

The square shaper (ref: schematic 0103-00-1116 sheet 3) takes the TTL square wave (TTL SQ) from the square selector and converts it to a clean, fast square wave current (±1mA) that drives the preamplifier. The square wave is created by alternately sourcing and sinking current through the diode switch (CR36 through 39).

The voltage divider (R141, CR33, CR34, CR35, R144) converts TTL SQR to a bipolar signal that switches the diodes in the square shaper. When TTL SQ is high, the vol at the cathode of CR36 is approximately +1.5V; C sinks current from the TTL SQ signal while CR37 sou 1mA from the +15V supply through U5 pin 6 tc preamplifier. When TTL SQ toggles low, the volta the cathode of CR36 is approximately −1.5V; C sources current to the TTL SQ signal and CR39 sinks from the preamplifier through U5 pin 6 to the −15V ply. The current source and sink for upper and lc levels of square waves are independently adjustab R142 and R147. Resistor R146 sets high frequ square wave peaking.

4.2.4.4 Sine Converter

The sine converter (ref: schematic 0103-00-1116 s 3) transforms the triangle into a sine wave. The sine verter uses the logarithmic response characteristi the six matched diodes (U4) to approximate a sine v current output. Buffered triangle signal (TRB) enter converter at U4 pins 2, 3, and 9. SIN DIST A trim (R121) adjusts the converter input for diode for voltage variation. Two other adjustments, SIN DIST B (R132) and SIN DIST C (R137), balance the positive and negative peaks respectively. The current output is switched through FET switch (U5) when $\overline{SIN}$ is low. Tri Level trim pot (R126) adjusts the triangle waveform current that enters FET switch (U5) which is enabled by a low at $\overline{TRI}$.

4.2.4.5 Function Select

The function select circuit (ref: schematic 0103-00-1116 sheet 3) connects either the synthesizer output signal (SYNTH SIG), the square wave (TTL SQ), the sine converter output, or the buffered triangle (TRB) to the input of the preamplifier. Signal switching is handled by four section CMOS analog switch (U5). For example, when $\overline{SYNTH}$ goes low, U5 pins 14 and 15 short together which connects SYNTH SIG to the preamplifier. C57 and C58 eliminate ringing (switch bounce) on the control line. Except for signal names and component numbers, the remaining three sections are identical.

Both the triangle and sine FET switches (U5), when not selected, are isolated by shorting their inputs to ground through Q27 or Q28. For example, when $\overline{TRI}$ is high (not selected), Q26 is turned off, the collector of Q26 goes low, and Q27 is forward biased which effectively shorts the emitter of Q27 to ground.

4.2.4.6 Preamplifier

The preamplifier (ref: schematic 0103-00-1116 sheet 4) inverts and amplifies the signal current from the function selector to a sufficient voltage level for the output amplifier. The gain of the preamplifier is controlled by R184, which sets the sine wave amplitude; zener diodes CR44 and CR45 bias the preamplifier at ±9.4V.

4.2.4.7 Output Amplifier

The output amplifier (ref: schematic 0103-00-1116 sheet 4) provides the final gain and output drive of the instrument. It consists of an inverted summing amplifier (with a gain of about 10) for high-frequency signals and a differential amplifier for dc and low-frequency signals. The differential amplifier also allows the dc offset of the Func Out waveforms.

AC Signal Path: High-frequency signals couple into the symmetrical emitter followers Q29 and Q32 through capacitors C91 and C92 respectively. These emitter followers drive the symmetrical inverter stage consisting of Q30 and Q33. Diodes CR46 and CR47, along with the 10Ω resistor R175, increase the switching speed of the output stage transistors Q31 and Q34 by biasing them partially on. The output signal (±20V, maximum) feeds back through resistors R176 and R177 to the input. Two 100Ω resistors (R196 and R197) set the output impedance for the Func Out (50Ω) connector.

DC Signal Path: The dc and low-frequency path in the output amplifier is through the differential amplifier transistor array (U26). The output signal (U26 pin 3), inverted relative to the input (U26 pin 5), controls the current through transistor Q30. The signal at the collector of Q30 changes until the fed back signal through R176 and R177 balances with the input signals. The PNP transistors (U26) balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C85 limits the speed of this section at high frequencies.

Offset Circuit: When the D.C. Offset switch is turned on, the voltage on the wiper of R3 is converted to current through R167 and R168. This current is proportional to the voltage and polarity at the wiper of R3 and provides dc control of the input current and, therefore, the output voltage offset.

4.2.4.8 Attenuator

The attenuator (ref: schematic 0103-00-1116 sheet 4), two 498Ω resistors (R198 and R199) and a 54.9Ω resistor (R200), provides 20dB of attenuation at 50Ω output impedance to the Func Out (−20dB) connector.

4.2.4.9 Output Protection

The output protection circuits (ref: schematic 0103-00-1116 sheet 4) guard the output amplifier from excessive external voltages that could be accidentally connected to either of the Func Out BNCs that could damage the instrument.

There are two safeguards to protect the output amplifier.

1. Two in-line fast-blow fuses for each Func Out connector.
2. Four voltage-limiting, high current diodes (CR50 through CR53) that provide additional protection at the Func Out (50Ω) connector.

4.2.5 Pushbutton Interface

When a front panel pushbutton is pressed, an input to the pushbutton interface (ref: figure 4-7 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) is connected to either +5V or ground which switches the logic level of the pushbutton interface output. The MAN TRIG line from the pushbutton interface goes to the trigger logic, while the remaining lines go to the digital control block. Each switch drives a Schmitt trigger gate. RC circuits prevent multiple pulsing at the input of each gate. Outputs drive the appropriate control circuit within the unit.

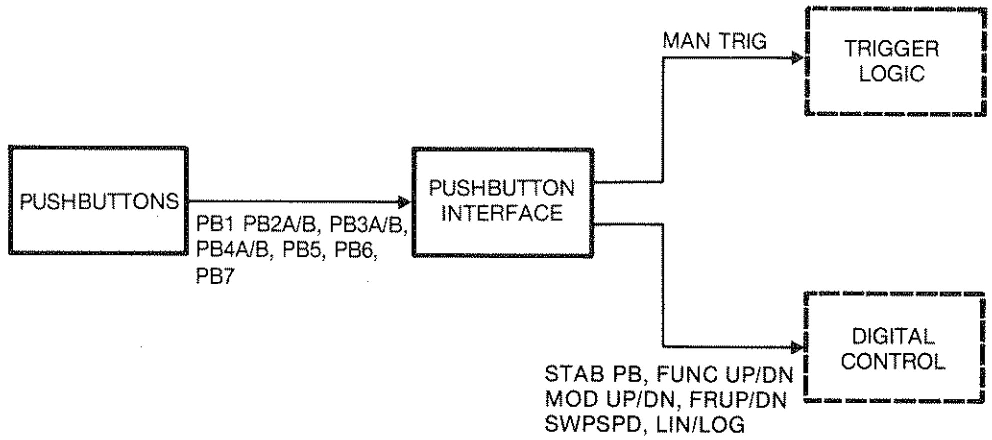

Figure 4-7. Pushbutton Interface

4.2.6 Digital Control

The digital control block (figure 4-8) consists of the power on reset, mode control, misc. control, frequency range control, function control and sweep speed control circuits.

4.2.6.1 Power-On Reset

The power-on reset circuit (ref: schematic 0103-00-1 sheet 3) sets all other digital control circuits to a prede mined state. On initial power up, C57 holds U3G pin low which causes MR (pin 12) to go high and $\overline{\text{MR}}$ (pi

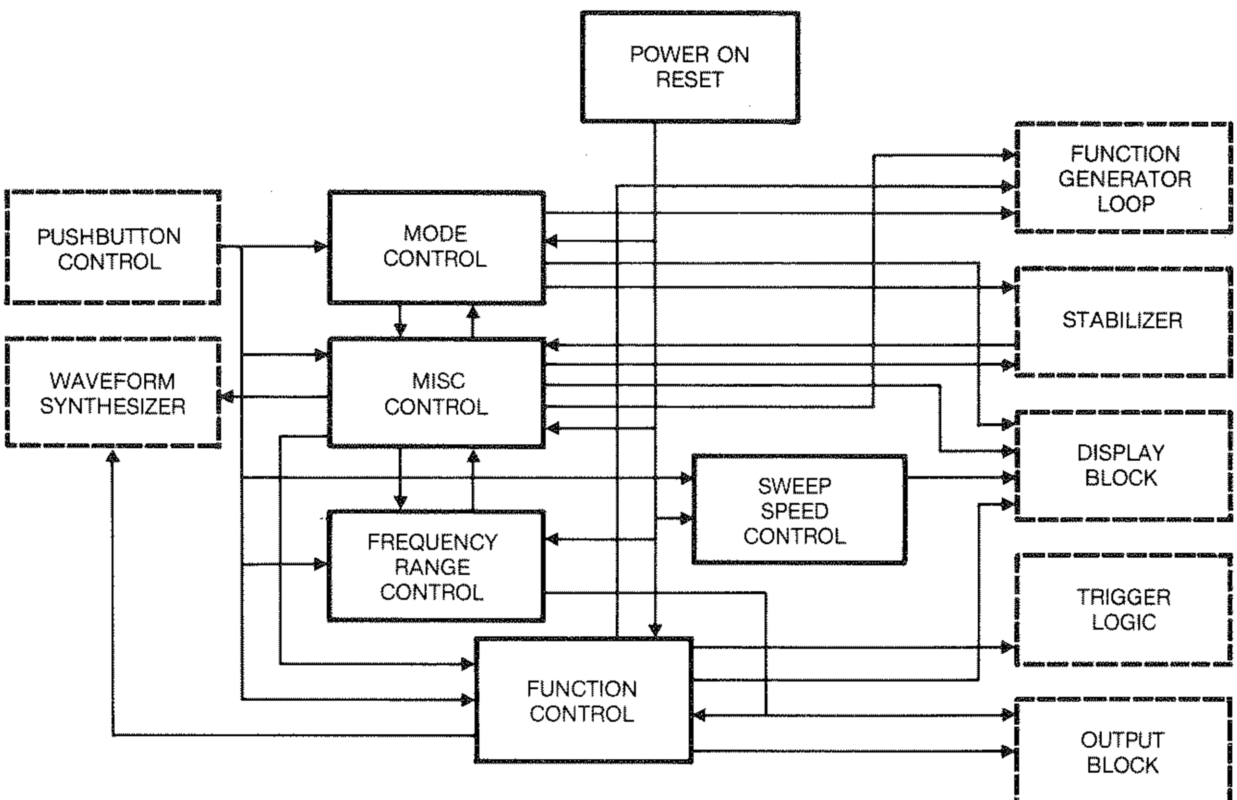

Figure 4-8. Digital Control

to go low. MR and $\overline{MR}$ reset the various digital control circuits. After about ½ second, C57 has charged to approximately 2.5V which causes MR (pin 12) to toggle low and $\overline{MR}$ (pin 4) to toggle high. These levels now remain constant for the remainder of the time the unit is on.

4.2.6.2 Mode Control

As the Mode pushbutton control lines (ref: figure 4-9) are pulsed, the mode control circuit steps through a sequence of modes either up (MODUP) or down (MODDN) from the last selected mode. This switches one of the output mode lines low. These mode lines, in conjunction with additional logic gates, control the trigger logic, stabilizer, display, and misc control; $\overline{CONT}$ combines with $\overline{STOP}$ to produce BL.

The mode control circuit (ref: schematic 0103-00-1115 sheet 2) contains the up/down counter (U4G) with separate count up (MODUP) and count down (MODDN) inputs. The counter's output drives decoder U4F that enables one of the seven modes.

The two NAND gates (U5G) limit up or down counts between gate and sweep. At one extreme (gate mode), U5G pin 8 is low, which causes pin 11 to remain high and

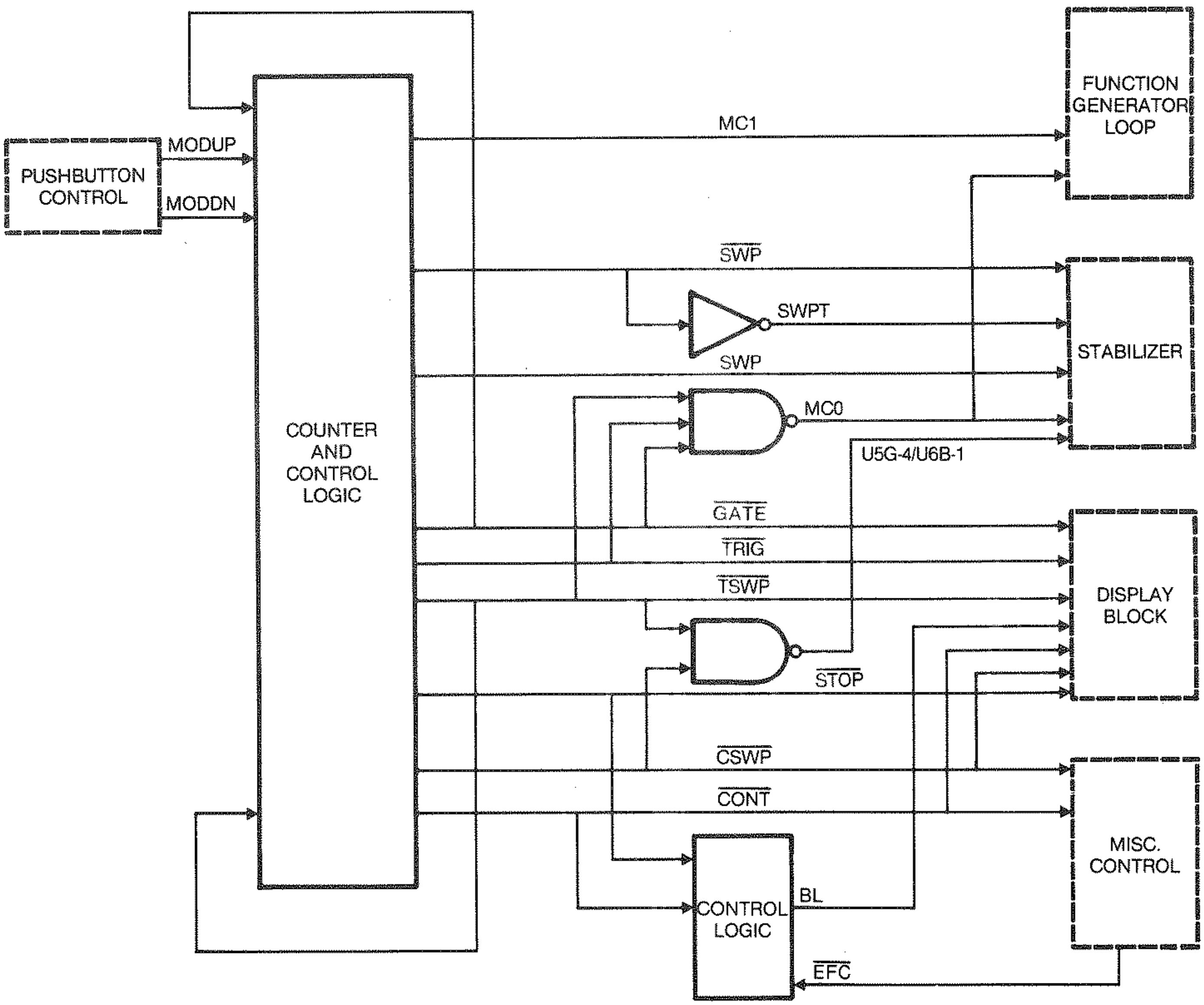

Figure 4-9. Mode Control

inhibits inputs at pin 12. In the other case (triggered sweep mode), U5G pin 8 inhibits pin 9. MC0 and MC1 control the trigger logic. $\overline{\text{CONT}}$ controls the misc. control. $\overline{\text{GATE}}$, $\overline{\text{TRIG}}$, and $\overline{\text{CONT}}$ enable the appropriate segment on the display. In trig or gate modes, BL disables all number segments of the display.

4.2.6.3 Misc Control

The misc control circuit (ref: figure 4-10 and schematic 0103-00-1115 sheet 2) receives control lines (LIN/LOG, STABPB, and EFCPB/SWPSPD) from the pushbutton interface, $\overline{\text{CONT}}$, $\overline{\text{CSWP}}$ and $\overline{\text{TSWP}}$ from the mode control, LF from the frequency frange control, and UNST from the stabilizer circuit. It drives the display, stabili function generator loop, frequency range control, m control, function control, waveform synthesizer, anc converter.

Sweep Speed: The sweep speed counter (U3A) recei a pulse (EFCPB/SWPPD) from the pushbutton interf (U3G pin 10) each time the Swp Time pushbutto pressed. This steps the counter (U3A) through four bir states which supply control lines SPD0 and SPD1. Th two lines are further decoded by U4C whose outp through the display drivers, control the display.

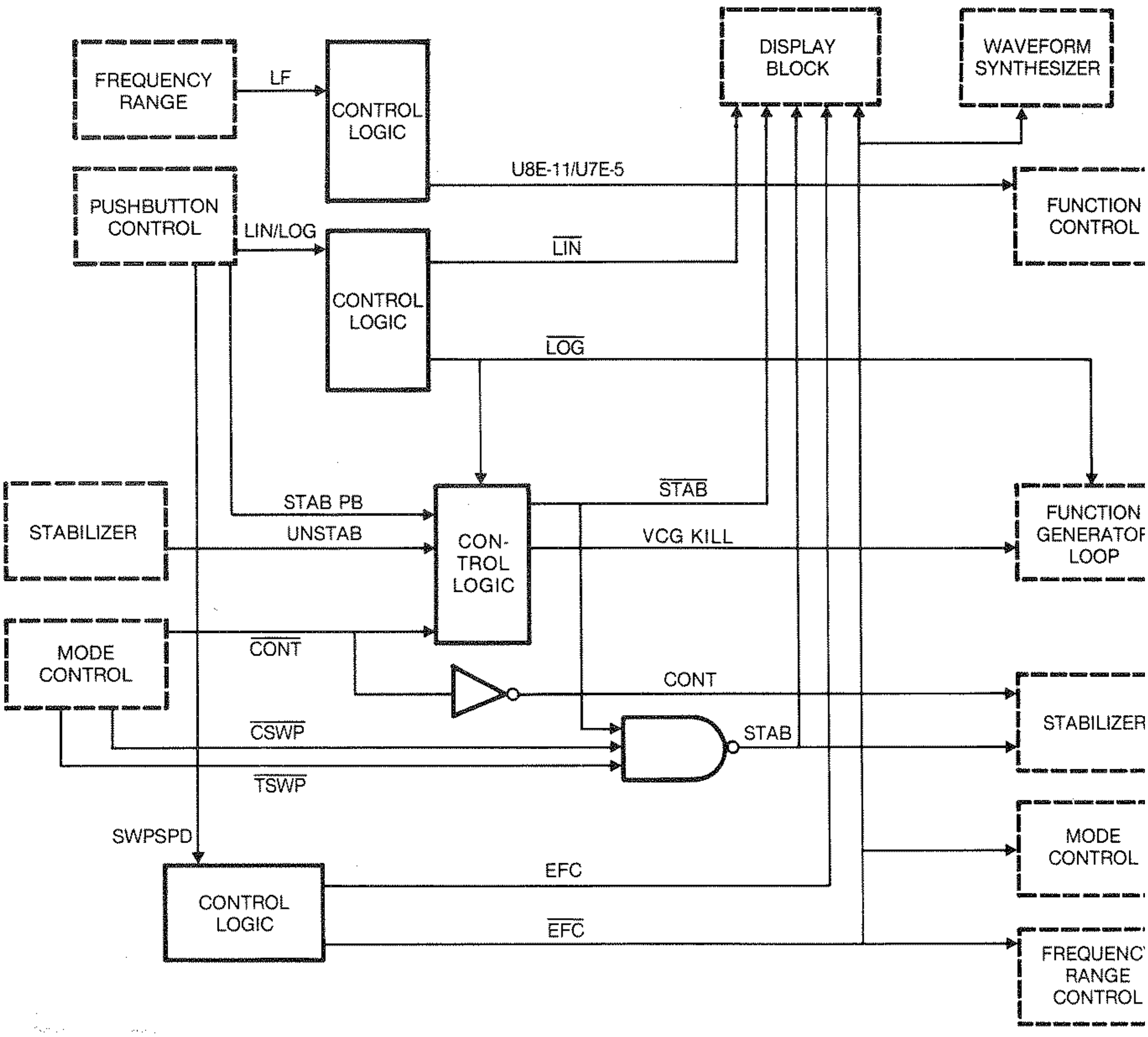

Figure 4-10. Misc Control

Lin/Log: The Lin/Log counter (U7A) receives a pulse from the pushbutton interface (U3G pin 6) each time the Lin/Log pushbutton is pressed. This causes the counter output (U7A pin 3) to change states. When $\overline{\text{LIN}}$ goes low, linear frequency change is selected.

Stabilizer: The stab flip-flop (U6F) receives a pulse (STABPB) from the pushbutton interface (U3G pin 2). Since both J/K inputs to U6F (pins 10 and 11) are always high, the two flip-flop outputs (pins 14 and 15) change state each time the flip-flop receives a STABPB pulse. When the stabilizer is off, $\overline{\text{STAB}}$ is high. U4E inverts $\overline{\text{STAB}}$ to produce STAB which, when low, allows MEMCLK to be pulsed with each transition of U7E pin 13. When the stabilizer is on, $\overline{\text{STAB}}$ is low, making STAB high, which in turn holds MEMCLK low at all times. With $\overline{\text{STAB}}$ low, VCG KILL is high which disconnects the VCG In BNC from the input of the VCG circuit. The stabilizer is disabled by U6G pin 1 if UNSTAB (U6G pin 3) goes low, the frequency exceeds the range, or a mode other than continuous is selected.

4.2.6.4 Frequency Range Control

The frequency range control circuit (ref: figure 4-11 and schematic 0103-00-1115 sheet 2) steps through a sequence of frequency ranges. As the Freq Range pushbutton is pressed, the pushbutton interface detects whether the frequency range should increase (FRUP) or decrease (FRDN). The circuit's output lines control the

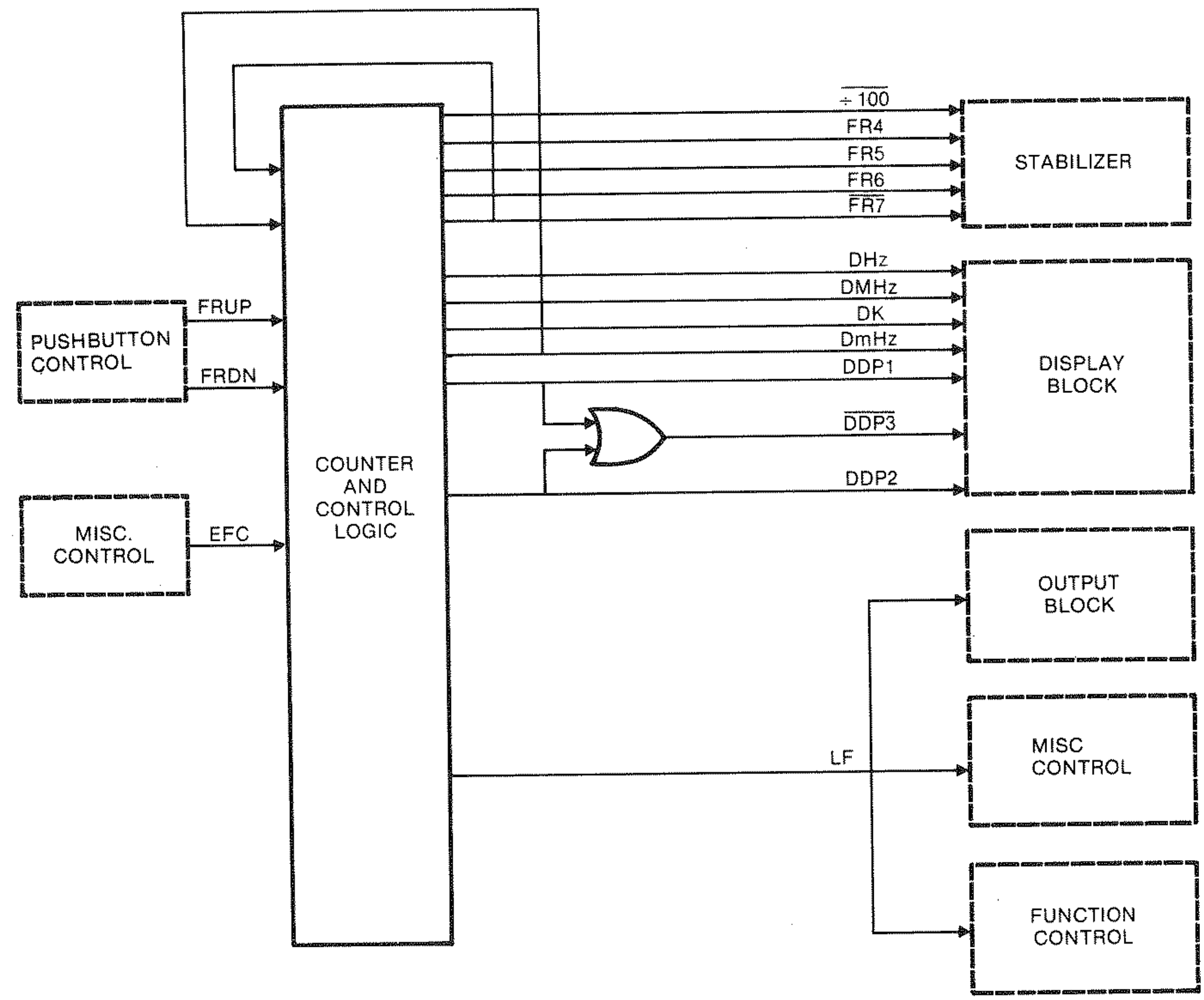

Figure 4-11. Frequency Range Control

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stabilizer, display block, output block, function control, and misc control. External frequency control (EFC) combines with other control lines to produce LF.

Up/down counter (U6E), which has separate "count up" and "count down" inputs, receives pulsed signals from U5F originating from the freq range (FRUP and FRDN) pushbutton buffers. The output of this counter drives decoder (U6D), which selects one of its output lines to be low. $\overline{FR7}$, which controls the HF COMP on the analog board and goes to the frequency counter, is driven directly by one of these lines. From the remaining output lines are decoded the appropriate frequency range control lines (FR4, FR5, and FR6), which are inverted by the frequency counter circuit before going to the analog portion of the generator. The nine output frequency ranges of the generator originate from these four control lines (FR4, FR5, FR6, and $\overline{FR7}$), the low frequency synthesizer, and the $\overline{\div 100}$ control line. In the five lowest ranges, LF is high which, unless square function is selected, enables SYNTH (through the function control). This connects the output of the LF waveform synthesizer to the input of the preamplifier. The output frequency of the synthesizer is 1/1000th of the range selected. For example, if FR5 (110kHz range) is selected, the output frequency range of the synthesizer (and therefore the Func Out connectors), would be 110Hz. In addition, in the 3 lowest ranges, $\overline{\div 100}$ is low, further dividing this signal by 100. Using the same example, the synthesizer output frequency range would now be 110 mHz. Two NAND gates (U5F), serve to prevent any up or down count beyond the capability of the unit. At one extreme (110mHz frequency range), U5F pin 1 is low which causes pin 3 to remain high at all times and disables pin 2. In the other extreme, (11.00 MHz), U5F pins 8, 9, and 10 perform this function.

On the display, DmHz controls the "mHz" emblem, DHz controls "Hz", DK controls "K", and DMHz controls "MHz". The decimal points are controlled by DDP1, DDP2, and $\overline{DDP3}$.

4.2.6.5 Function Control

The function control (ref: figure 4-12 and schematic 0103-00-1115 sheet 2), which selects the instruments six functions (waveforms), consists of the input gates (U5F), up down counter (U5D), decoder (U4D), and control gates (U4E, U5E, U6E).

When the Func pushbutton is pressed, a pulse occurs on either the FUNCUP or FUNCDN lines. These lines, routed through the input gates, step the up/down counter either up or down from the last selected function. The BCD output from the counter is decoded by U4D; a low on the decoder's output represents an enabled line. The control gates (U4E, U5E, and U6C) further decode the circuits output lines. These lines control the d
block, output block, trigger logic and wave
synthesizer.

The two NAND gates (U5F) prevent any up or down
beyond the limits. For dc function, U5F pin 13 i
which disables FUNCDN at U5F pin 12. For ne
going ramp, U5F pin 5 goes low which disables FU
at U5F pin 6. Output lines $\overline{TRI}$, $\overline{SIN}$, and $\overline{SQR}$ in th
synthesized frequency ranges select the waveforr
to the preamplifier. When LF (from the frequency
control) is high and the unit is in sine, triangle, or
ramp function, $\overline{SYNTH}$ is selected (low) connecti
output of the waveform synthesizer to the input
preamplifier. FS0 and FS1 select the waveform
waveform synthesizer output. When the unit is in s
function, $\overline{SQR}$ is selected (low), connecting the
of the square shaper to the input of the preamplifie
⎍ , ⏷ , ◸ , ◿ enable the appropriate segm
the front panel display.

4.2.7 Display

The display block (ref: figure 4-13 and scher
0103-00-1115 sheet 1 and 0103-00-1117) consists
display drivers and the display. Two 30 Hz signa
and its complement $\overline{BP}$ originating from U5C
chronize the LCD and the segment drivers. To e
a segment of the display, 5Vrms is needed betwe
and the segment control line.

The display drivers are exclusive-or gates which
the display's bars, arrows, and decimal points a
function the same. For example, when the unit is i
tinuous mode, U3F pin 9 ($\overline{CONT}$) is low. The $\overline{BP}$
at pin 8 is in phase with the signal at pin 10 (Z3) a
of phase with BP. This results in a 5Vrms volt
between BP and Z3, which enables the segment.
the unit is not in Cont mode, a high at pin 9 caus
output at pin 10 to be in phase with BP which res
0Vrms and disables the segment. Data for these
originate from the various digital control circuits
unit.

Lines D2A through D4D, which originate from t
quency comparator, determine which number seg
are enabled. Each output line (2A through 4G) d
number segment except in Trig or Gate modes whe
are disabled by BL.

4.2.8 Power Supply

Three power supply voltages, +15V, −15V, an
are generated on the power supply circuit boa
schematic 0103-00-1113).

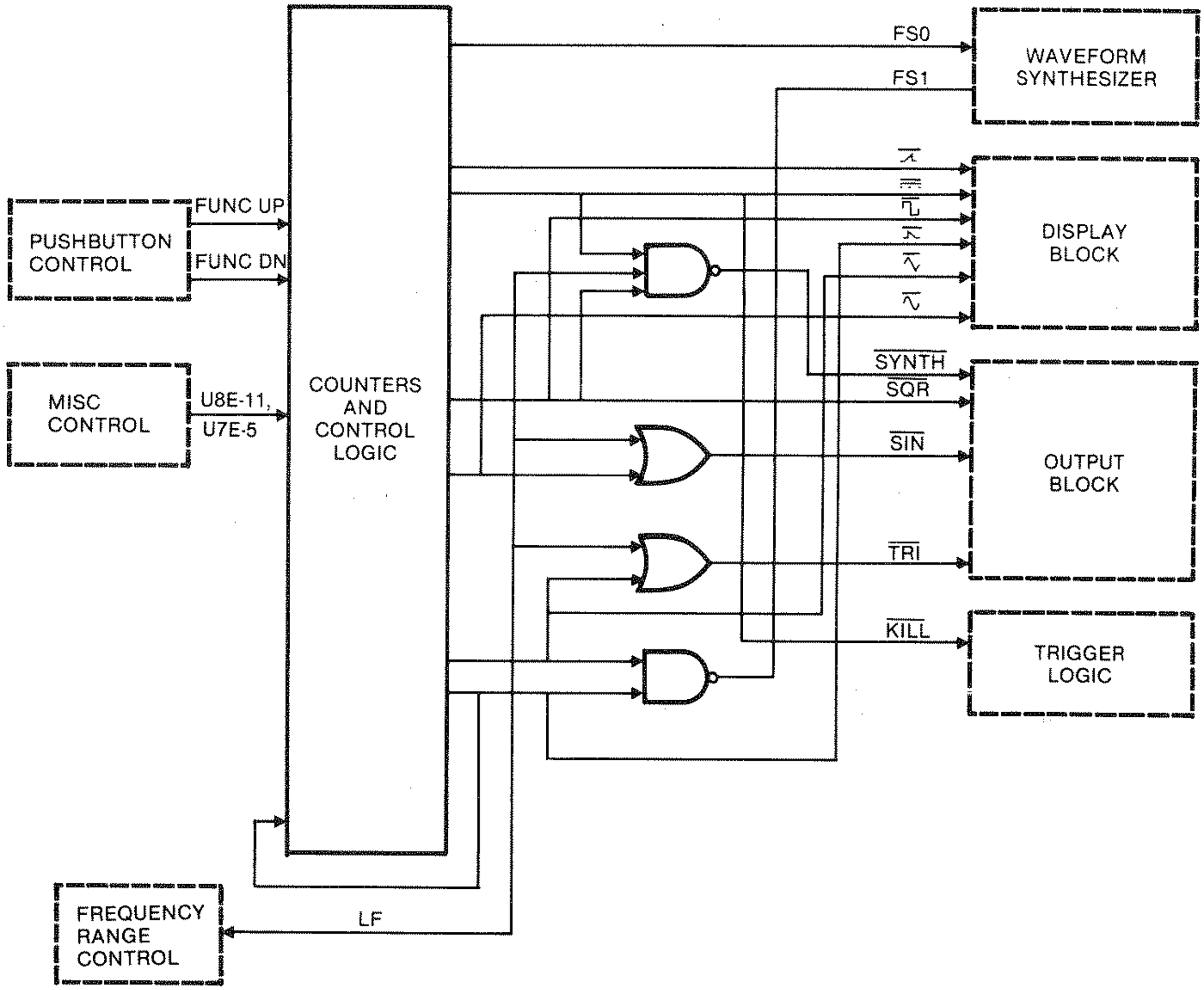

Figure 4-12. Function Control

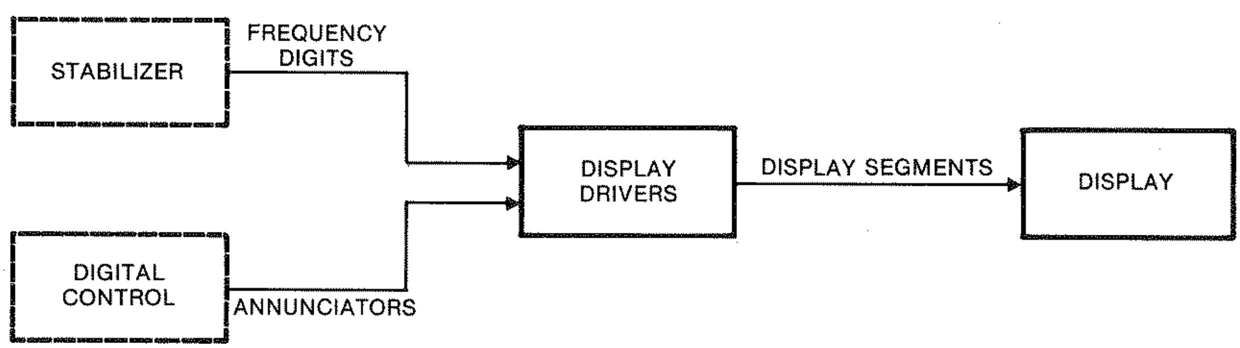

Figure 4-13. Display Block

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4.2.8.1 +5V Supply

In the +5V supply, ac from the transformer T1 (located on the rear panel), is rectified by CR2 and filtered by C9, C10, and C11 to provide unregulated dc for regulator VR2. This three-terminal regulator normally operates with a 1.25V difference between its input and output terminals. C12 provides additional filtering at the output of the regulator.

4.2.8.2 ±15V Power Supplies

The ±15V Power Supplies provide power to the analog sections of the instrument. R2, which is in series the output of the +15V regulator, causes current lin to take place at a lower value than the internal lin provided by the regulator. As the current throug reaches its limiting value, the voltage drop acros reaches 0.4V. Any further current through R2 cause regulator to lower the output voltage until the curren back to the limiting value.

The −15V supply operates similarly to the +15V su however the polarities are reversed.

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SECTION
CALIBRAT

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter	Millivolt dc measurement (0.1% accuracy), true rms
Oscilloscope, Dual Channel	≥100 MHz bandwidth
Counter	20 MHz (0.01% accuracy)
50Ω Feedthru	±0.5% accuracy, 2W
Distortion Analyzer	To 200 kHz
RG58U Coax Cable	3 ft length BNC male contacts
Spectrum Analyzer	To 60 MHz
Pulse Generator	40 Hz, 5 to 15 ms pulse width, TTL level.

5.3 CALIBRATION

NOTE

Before removing the cover, disconnect the instrument from the ac power source. Refer to Section 2 for cover removal, except leave top cover on and remove only bottom cover for calibration. Invert the instrument so generator board adjustments are on top and place the bottom cover on top of the unit to maintain the operating temperture during calibration.

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. Figure 5-1 shows waveform generator board calibration points.

NOTE

The completion of these calibration procedures returns the instrument to correct calibration. All limits and tolerances given in these procedures are calibration guides and should not be interpreted as instrument specifications. Instrument specifications are given in Section 1 of this manual.

1. All measurements made at the FUNC OUT nector must be terminated into a 50Ω (±0 load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing the bottom c connecting the unit to an ac source, and se these front panel switches as follows:

   Frequency
   - Fine . . . .
   - Coarse . . . .

   Amplitude . . . .
   D.C. Offset . . . .
   Swp Set . . . .

3. Allow the unit to warm up at least 30 minutes fo calibration. Keep the instrument covers on to tain heat. Lift bottom cover only to make adjustr or measurements.

Table 5-1. Calibration Procedure

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
1	Power Supply Regulators	dc Voltmeter	J10 Pin 2	Paragraph 5.3 step 2			Black (−) lead ground
2			J10 Pin 5			−15V ± 350 mV	Red (+) lead dc volts
3			J10 Pin 6			+5V ± 250 mV	
4			J10 Pin 7			+15V ± 350 mV	
5	Triangle Amplifier Balance		J10 Pin 3		R103	0V ± 100 mV	Rough adjustment only
6					R86	0V ± 20 mV	
7	Function Out	Scope	Func Out (50Ω)			10Vp-p sine wave (Approximately 2 cycles)	Terminate with 50Ω Scope Settings: 2V/div. 0.2 ms/div.
8				Step Func button to right		Functions match display (correct amplitude and frequency)	
9	Output Amplifier Balance			Func: ⎓ (dc)	R157	0V ± 10 mV	Display shows 00.0 kHz Scope setting: 10 mV/div. (or maximum scope sensitivity if more than 10 mV)
10	Trigger Baseline			Func: /\/ Frequency knobs: fully cw Freq Range: 110.0 kHz Mode: Trig	R103	0Vdc ± 50 mV	Scope setting: 0.1V/div. Verify baseline 0VDC ±100 mV over full range of Coarse Frequency knob (Frequency Fine knob full cw)
11	VCG Zero	DC Voltmeter	VCG In BNC	MODE: Cont Func: ⊓⊔ Frequency knobs: fully ccw	R11	0V ± 0.5 mV	Use coax cable with no termination.
12	1100:1 Frequency	Scope	Func Out (50Ω)		R13	First transition occurs at center vertical grid line, for 50 Hz.	Use coax cable with 50Ω termination. Scope settings: 2V/div. 2ms/div. Trigger slope: − (Neg) Horizontal position: Trace begins at extreme left vertical grid line
13	1100:1 Symmetry				R38	Second transition occurs at extreme right vertical grid (within 2% (1 minor division)	Repeat steps 12 and 13 if necessary. Alternate method: magnify X10 and alternate trigger slope between + and −, set R38 for <2 divisions assymetry.
14	Low Log			Lin/Log: Log	R36	One cycle is 10 division	Scope setting: 2ms/div. 2V/div.

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
15	High Symmetry	Scope	Func Out (50Ω)	Lin/Log: Lin Frequency knobs: fully cw Freq Range: 11.00 kHz	R20	<0.1% (½ minor div.) symmetry	Scope setting: 2V/d 10 μ X10 Magnification. nate trigger slopes adjusting R20 for minimum assymetry
16				Coarse Frequency: 5kHz	Verify only	<0.5% asymmetry (Verify 2½ minor divisions)	Scope setting: 20 μ Magnification: Off
17	Sine Distortion	Distortion Analyzer		Frequency knobs: fully cw Func: ∿	R121, R132, R137, R86	Minimum distortion (typically 0.2 to 0.3%)	Adjust R86 slightly necessary.
18	Full Scale Frequency	Counter		Func: ⊓⊔	R1	11.15 kHz on display	Display reads same counter ± 0.01 kH
19		Display		Switch between Range: 11 kHz and 110 kHz Freq Ranges		11 kHz Freq Range: 11.05 to 11.25 kHz. 110 kHz Freq Range: 110.5 to 112.5 kHz.	Set for best frequer balance between fr ranges. C44 (.001 μ nominal value) trim 11.00 kHZ range.
20	High Log			Freq Range: 11.00 kHz Lin/Log: Log	R31	11.15 kHz	
21	11:1 Frequency			Freq Range: 110 kHz Lin/Log: Lin Frequency Coarse knob: fully ccw	Verify only	10± 2kHz on display	
22	High Frequency Calibration			Frequency knobs: fully cw Freq Range: 1.1 MHz	C40	1.115 ± .005 MHz on display	C41 may be trimme obtain equal adjustn above and below 1.110 MHz
23				Frequency Coarse knob: fully ccw		Note display reading	
24				Freq Range: 11 MHz Frequency Coarse knob: fully ccw	C38	Set for 10 times reading noted in previous step	C39 may be trimm obtain equal adjust above and below g frequency
25				Frequency knobs: fully cw	R80	11.15 ± .05 MHz	
26	Amplitude	True rms Voltmeter		Func: ∿ Freq Range: 11.00 kHz Frequency Coarse fully ccw	R184	3.55 ±0.015 Vac (3.535 to 3.565 Vac)	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
27	Amplitude	True rms Voltmeter	Func Out (50Ω)	Func: ∿	R126	2.90 ±0.015 Vac (2.885 to 2.915 Vac)	
28				Frequency knobs: fully cw Freq Range: 1.1 kHz	R151		
29		dc Voltmeter		Freq Range: 110 mHz Func: ⊓⊔	R142	+5.025 ±0.025 Vdc. (+5.00 to 5.05 Vdc).	Turn frequency coarse knob fully ccw to hold each peak while adjusting
30					R147	−5.025 ±0.025 Vdc. (−5.00 to −5.05 Vdc).	
31	Waveform Quality and Frequency Response	Scope		Frequency knobs: fully cw Freq Range: 1.100 MHz Amplitude: 8Vp-p	R146	Minimum aberations <4% (320 mV)	Scope settings: 2V/div. 0.1 μs/div. (Observe peak-to-peak aberations at 0.5 V/div by adjusting vertical position)
32				Amplitude: fully cw		Rise/Fall <22 ns	Scope settings: X10 Magnification
33				Func: ∿ Frequency knobs: fully cw Freq Range: 11.00 MHz	Verify only	Amplitude between 8.6 and 10V	Scope settings: Magnification Off
34		Spectrum Analyzer		Freq Range: 1.100 MHz		Harmonics less than −40 dBc from 1.1 to 0.1 MHz	Rotate coarse frequency controls through its range and return fully cw
35				Freq Range: 11 MHz		Harmonics less than −28 dBc from 11 to 1 MHz	Rotate the Coarse frequency control through its range and return to full cw.
36	D.C. Offset	Scope or dc voltmeter		Function: ⎓ (dc) D.C. Offset: fully cw		Minimum +5Vdc	The calibration procedure is complete; start functional checkout.
37				D.C. Offset: ccw (not in detent)		−5Vdc or more negative	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
38	– 20 dB Output	Scope	Func Out (50Ω)	D.C. Offset: Off Func: ⊓⊔ Frequency knobs: fully cw Freq Range: 11.00 kHz	Verify only	Approximately 10 Vp-p square wave	Scope settings: 2V 20
39			Func Out (– 20 dB)			Approximately 1Vp-p square wave. Note value.	Scope settings: 0.2
40			Func Out (50Ω)	Amplitude: fully ccw		Verify Vp-p less than value noted in step 39	
41	Sync Out		Sync Out	Amplitude: fully cw		Normal TTL level square wave	Remove 50Ω termi Scope setting: 2V/c
42	Trigger and Gate			Mode: Trig		Display shows Trig (numbers blanked). Scope shows approximately 0Vdc.	
43			Func Out (50Ω)	Func: ∿		Verify triggered sine wave	Connect 1kHz TTL signal from externa source to CH2 and (TTL) BNC. Scope settings: 0.2 Trigger on CH2, Monitor CH1
44				Mode: Gate		Display shows Gate Verify gated sine wave	
45	Manual Trigger					Sine wave when Trigger button pressed	Disconnect externa nal source, scope CH2 and Trig In (TT Trigger on CH1
46	VCG In			Mode: Cont Freq Range: 110.0 kHz Frequency knobs: fully ccw Func: ⊓⊔		Display shows 110 ± 5 kHz	Connect +5VDC t In BNC.
47						Verify one cycle >5 divisions	Remove voltage fr In BNC. Scope setting: 2ms
48	Linear Sweep	Scope	Func Out (50Ω), Swp Out	Frequency knobs: fully cw Freq Range: 110.0 kHz Func: ∿		CH2: > +5 Vdc	Scope — CH1: 2V/div; Func CH2: 2V/div; Swp Time Base: 1ms/di Trigger: – slope, C Vert Mode: Alterna
49				Mode: Swp Set. Frequency knobs: fully ccw.		Display: Set. Scope: CH1 frequency and CH2 voltage varies in the Swp Set control.	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
50	Linear Sweep	Scope	Func Out (50Ω) Swp Out	Mode: Swp Swp Set: cw	Verify only	Display: Swp 0.01s Scope: CH2-0 to ⩾5 V, 10 ms ramp. CH1 Linear swept sine wave.	
51	Log Sweep			Lin/Log: Log		Display: Log. Scope: CH1 Logarithm swept sine wave.	
52	Sweep Time .1s			Swp Time: .1 sec		Display: 0.1 sec. Scope: CH2 0 to ⩾5 V, 100 ms ramp.	Scope: Time base: 10 ms/div. Vert Mode: Chop Sweep Mode: Norm Trig.
53	Sweep Time 1s	Scope and Counter		Swp Time: 1 sec		Display: 1s. Scope: Slow sweep. Counter: 1s period	Scope: Time base: 1ms/div. Trigger: CH1. Connect counter to Swp Out.
54	Sweep Time 10s			Sweep Time: 10s		Display: 10s. Scope: Slow sweep. Counter: 10s period.	
55	Triggered Sweep	Scope		Swp Time: 0.01s Lin/Log: Lin. Freq Range: 1.100 kHz. Mode: Trig Sweep Frequency Coarse: cw Fine: cw		Display: 0.01s. Trig Swp Scope: Sweep starts coincident with rising edge of trigger signal; waveform returns to baseline at end of sweep.	Disconnect counter; Connect pulse generator to CH2 and Trig In. Scope: CH1 and CH2: 2V/div. Time base: 5ms/div. Trigger: CH2; +Slope. Pulse Generator: TTL level. 5ms pulse at 40 Hz (25 ms) rate.
56						Scope: Sweep starts coincident with rising edge of trigger signal; waveform returns to start frequency.	Pulse Generator: 15 ms pulse at 40 Hz rate.

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
57	Stab	Scope		Mode: Cont Stab: Off Frequency Fine: initially centered Frequency Coarse: 500Hz Func: ⊓⊔ Stab: On	Verify only	Quickly turn Frequency Fine knob as indicated and verify the following: 1) Rotate the Fine control cw to move transition from center to 3cm to the left. 2) Transition travels approximately 2 cm toward center of scope display 3) Transition jumps back to 3cm left of center grid line 4) Stab now Off	Disconnect Trig In si Scope settings: CH1: 2V/div. Time base: 0.2 ms Trig: CH1, + Slope X10 Magnification: Adjust horizontal p tion for square wa transition at cente NOTE *Stabilizer automatica disengages when it reaches its electrical limits.*
58				Use Frequency Fine knob to return square wave transition to center vertical grid line Stab: On		Same as step 57 in opposite direction	Repeat as in step 57 except turn Frequenc Fine knob ccw to mo transition from cente 3 cm right
59	Low Frequency Ranges			Frequency knobs: fully cw		Display reads between 1.105 kHz and 1.125 kHz	Scope settings: 50 µ X10 Magnification: C Set horizontal variab 1 cycle on screen
60				Freq Range: 110.0 Hz		Display reads between 110.5 Hz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5 m
61				Freq Range: 11.00 Hz		Display reads between 11.05 Hz and 11.25 Hz. Scope screen shows 1 cycle.	Scope setting: 5ms/ Trigger mode: Norm
62				Freq Range: 1.100 Hz		Display reads between 1.105 Hz and 1.125 Hz. Scope screen shows 1 cycle.	Scope setting: 50 m
63				Freq Range: 110.0 mHz		Display reads between 110.5 mHz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5s/div.

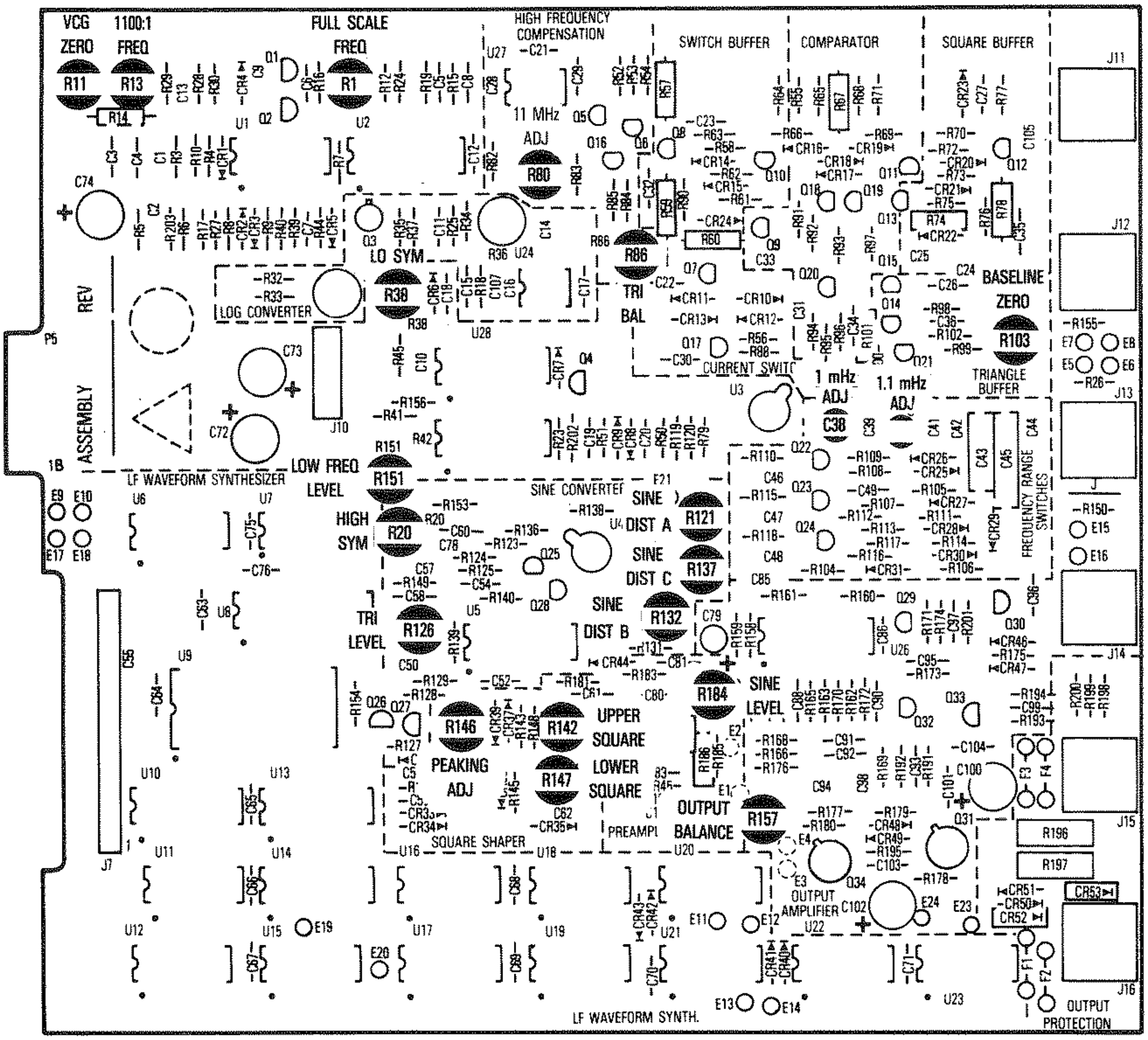

Figure 5-1. Calibration Points